ANALYSIS OF THE MULTIPLICATION AND LINEAR INTEGRATION INPUT TECHNIQUES TO A CCD

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ABSTRACT

The two important signal processing functions of multiplication and linear integration can be realized by operating the input of a CCD in a transient dynamic injection mode. Optimum design of input geometry requires the development of a model capable of predicting the input charge flow. This paper describes such a model, which simulates the flow of charge in an arbitary input structure, and compares the results with direct measurements of the injected charge. The model includes external circuit components and uses a simple calculation of a surface fringing electric field which decays exponentially either side of a gate edge. This avoids the time consuming solution of a two dimensional Poisson's equation and results in a model capable of yielding sufficiently accurate values of injected charge packets for a wide range of input conditions within a reasonable time.

INTRODUCTION

Much effort has been devoted to the development of CCD input structures which produce the optimum linear relationship between an input charge packet and the instantaneously sampled signal voltage.[1,2] All such methods rely upon potential equilibration to cancel distortion resulting from the complex dynamic behaviour of incomplete charge injection and the non-linear variation of surface potential with the charge under a MOS gate. One of the earliest input techniques was dynamic charge injection[3] but, because of factors outlined above, it was superceded by the potential equilibration methods. However, in abandoning this technique two important signal processing functions remained undeveloped. They are, firstly, an integrating input capable of integrating the signal over a defined sampling window. This ensures that the total signal energy is sampled and thus avoids aliasing problems and the possible loss of certain information due to instantaneous sampling[4]. This is of great use in radar systems where the total content of a range cell is often more important than discrete samples taken at the cell boundaries[5]. Secondly, the non-linear charge injection can be used to obtain the product of two input voltage waveforms[6]. The technique has potentially a large bandwidth (100 MHz) while allowing a more compact design and has been incorporated into a recent 20 MHz correlator design[7].

SIMPLE THEORY

Consider a twin gate input scheme, as shown in fig 1, including the first phase gate, ϕ_1 of the CCD. Two signal voltages, V_D and V_C, are applied to the input diode and the second input gate respectively, while ϕ_1 is shown at its high voltage level. Charge is to be collected under ϕ_1, thus it is necessary for this voltage to be considerably greater than V_D and V_C. During the application of a voltage pulse of width τ and height $V_P > V_D$, V_C, within ϕ_1, carriers will flow

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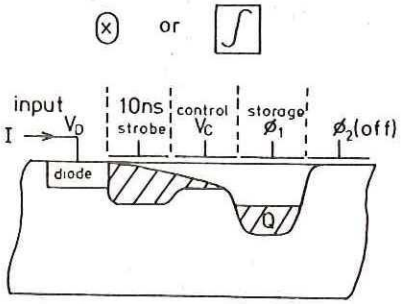

$$I = f(V_D, V_C) = \propto V_D V_C + \ldots$$

$$Q = \int I \, dt$$

Figure 1 *Schematic layout of a CCD configured to operate as a multiplier or linear integrator.*

from the diode such that charge is collected under ϕ_1. To first order, the input circuit may be analysed as a single transistor formed by the input diode as the source at V_D, an effective gate voltage of V_C, and a virtual drain under ϕ_1. Saturated operating conditions apply and the charge collected may be expressed as the integral of the saturated value of the equivalent MOS transistor current from an arbitrary time t:

$$Q = \frac{\beta}{2}\int_0^T \left\{ V_C(t + t') - V_D(t + t') - V_T \right\}^2 dt' \qquad (1)$$

where V_T is the gate threshold voltage. Q clearly contains a term in the integral, within the sampling interval, of the product of V_D and V_C. This term may be isolated by a time multiplexed four-quadrant transformation in which V_D and V_C are alternately referenced to V_D^R and V_C^R. These two charge packets are summed at the output and subtracted from the signal charge packet Q to give an output:

$$V_o = A\int_0^T \left\{ V_D(t + t') - V_C^R \right\}\left\{ V_C(t + t') - V_C^R \right\} dt' + V_{off} \qquad (2)$$

where V_{off} is a dc offset dependent only on V_D^R and V_C^R, and A is the gain. A linear integrator is similarly possible if either V_D or V_C is kept constant. The time penalty of multiplexing may be overcome by designing three inputs in parallel or, as in the case of the integrator, operating in a differentially linear region of input characteristics.

EXPERIMENTAL VERIFICATION

The method has previously been evaluated in a functional mode as a multiplier[6] and as a linear integrator[4]. In the case of the multiplier it has been shown to give a performance with spurious responses 38 db below the principle product terms. In this work a more basic method has been used to

give data against which a physical model may be compared in detail. This involves measuring the injected charge directly at the input as a function of V_D and V_C, thus avoiding any irrelevant effects introduced by charge transfer and non-uniformities in the remainder of the CCD. The charge is readily measured as a voltage drop across a large capacitance C (100pf) on the input diode as the input gates are pulsed in the sequence indicated in fig 2. For small time scales (T < RC) the diode voltage waveform is a

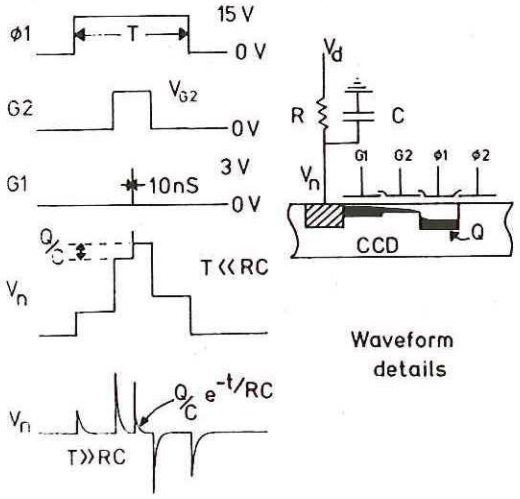

Figure 2 *Pulse sequence used in the measurement of input charge and the form of the diode waveforms observed.*

series of steps due both to stray capacitance and charge injection into the CCD. If the time scale is increased to T > RC, each pick up edge has time to relax to V_d and the injected charge alone may be measured by sampling shortly (< RC) after the end of the strobe pulse on G1. By sweeping the height of the pulse on G2 (V_C) between changing the value of V_d the charge input characteristics, as displayed in fig 3a for example, were obtained.

The curves consist of two regions depending on whether V_C is greater or less than the applied strobe pulse V_P (2V high and 5nS wide). In the upper region charge flow is restricted more by the strobe gate than the control gate, thus the variation of the injected charge Q with V_C is diminished and depends primarily on the increase in Q from that component due to charge storage under the control gate. Its slope is consistent with the capacitance of that gate (~ 0.6pF). The lower region corresponds to $V_C < V_P$ and is the active multiplying region as can be seen by the change in slope of Q with respect to V_C as the diode voltage is varied. The functional performance is highlighted in fig 4, where the results of a four-quadrant transformation on the data of fig 3a are displayed with $V_D^R = -0.2$ V and $V_C^R = 1.8$ V. The prediction of equation 2 is thus confirmed and the results are compatible with the 38db performance of ref 6.

The dashed curve in fig 3a is a typical characteristic given by eqn 1, and is inadequate as a description of the charge injection although eqn 2 does qualitatively predict the behaviour. The simple model fails to account for the presence of charges transiently stored under the strobe and control gates so that a fuller analysis is required.

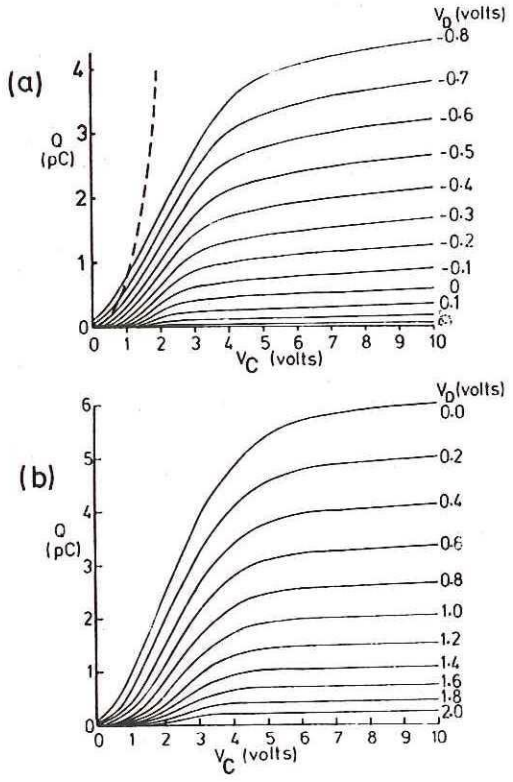

Figure 3 *Input charge characteristics as a function of the voltage on G2, V_C, and the voltage on the input diode, V_D, a) experimental, b) simulated.*

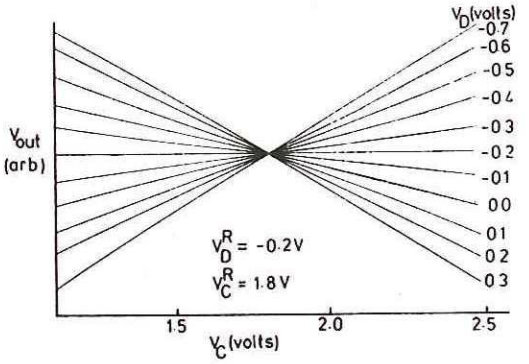

Figure 4 *Multiplier characteristics derived from a four-quadrant transformation of fig3a.*

DYNAMIC ANALYSIS

The dynamic analysis of charge movement within a CCD has been reported in detail by other authors[8,9] and the description here is kept to essential details. The minority carriers only were considered and they were assumed to be constrained to move at the $Si-SiO_2$ interface under the influence of self-induced, diffusion, and fringing electric, fields. The first two fields are simply derived from the charge distribution while the latter is included phenomenologically by assuming the fringing field to decay exponentially either side of a gate edge[9] according to:

$$E_f = \frac{1}{L}(V_1 - V_2)\exp(-x/L) \quad (3)$$

where V_1 and V_2 are the relevant gate voltages, x is the distance from the gate edge and L is 0.25 to 1.0μm depending on the oxide thickness (~ 0.12μm) and the substrate doping density (typically 6 x $10^{20}/m^3$). This simplification was tested through a two-dimensional solution of Poisson's equation for the surface fringing fields. The final accuracy was estimated to be well within the tolerances of processing parameters such as oxide thickness and threshold voltage variations between the different levels of polysilicon used in the construction of the CCD.

The charge flow was determined numerically by using the fringing fields, obtained as above, to calculate the current density[9] at defined mesh points within the input region. Use was then made of the continuity equation to determine the new charge density distribution, initially set to zero, after a small time step (typically 1pS). This charge density then set the new self-induced and diffusion fields which were included with the fringing field to calculate a new current density allowing the analysis to continue thus in a cyclic form. The calculation used the finite element technique as described by Gummel et al[10] to give increased stability and to allow the use of a coarse analytic mesh of 0.5μm, with gate lengths of 7μm. As boundary conditions, the current density was set to zero at the edge of ϕ_1 furthest from the input diode, while the diode itself was assumed to be an ohmic contact with a current density and voltage set by external circuitry such as R and C of fig 2.

The results of a simulation using the experimental conditions of fig 3a (a strobe pulse 2V high and 5nS wide, a voltage pulse on ϕ_1 of 15V, and a substrate bias of -1.1V, using an n-channel device with gates of width 300μm) are displayed in fig 3b. While not yet exact, the overall agreement is substantially better than a simple transfer model. The main cause of disagreement between the theoretical and experimental curves is the presence in the experimental device of a finite V_T of ~ 1.4V. For convenience V_T was assumed to be zero in the calculation but its effect can be included to sufficient accuracy by subtracting it from the values of control gate and diode voltages used in the simulation.

CONCLUSION

A detailed analysis of the charge flow in transient dynamic charge injection into a CCD has been performed, showing that the two functions of integration and multiplication can be obtained. Good agreement with experimental measurement on actual CCD structures has been obtained showing (i) that simple MOS analogies to the input are inadequate, and do not predict the experimental results other than qualitatively and (ii) that the model allows prediction of actual device performance and optimization of the design for good linearity and wide dynamic range. These useful functions can thus be included in actual device designs, with a quantitative prediction of their performance being achievable. An experimental method for the study of transient dynamic injection effects has been developed, and proves to be a useful tool for the study of practical devices. Further developments of these experimental and modelling tools will be extremely useful for advanced signal processing devices.

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