LOW-LOSS CCD CONCEPT

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ABSTRACT

Two closed-loop CCD structures (a 256-stage and 1024-stage) were built to demonstrate a low-loss mode of operation for a very long CCD delay line or a closed-loop CCD structure. The low-loss CCD concept consists of operating a CCD with each signal charge well followed by one or more trailing-bias-charge wells. Two orders of magnitude improvement in the effective transfer losses were demonstrated experimentally by periodically recombining at a signal-regeneration stage the (first-order) signal-charge transfer losses collected by the trailing bias charges with the corresponding signal-charge packets. An effective transfer loss of 2.4×10^{-7} per transfer was demonstrated. The maximum time delay has also been improved by more than two orders of magnitude over that of conventional CCDs by means of a dark-current subtraction technique.

INTRODUCTION

The typical charge transfer loss (charge transfer inefficiency) of a surface-channel CCD is on the order of 10^{-4} per transfer and for a buried channel CCD it is on the order of 10^{-5} per transfer. The low-loss CCD[1] described in this paper** represents a special mode of operation of a CCD structure that can result in about two orders of magnitude reduction in the effective charge transfer losses. This is achieved by operating the CCD structure with each signal charge well followed by one or more trailing-bias charge wells. The function of trailing bias charge is to keep the trapping states in the CCD channel filled. A very low effective transfer loss is achieved by periodically recombining the charge transfer losses collected by the trailing-bias-charge wells with the corresponding signal-charge packets at low-loss signal-regeneration stages. By adjusting the level of the trailing bias charge to be above the signal-charge level, we can guarantee that the effective transfer losses in a low-loss CCD are reduced to the second-order trapping losses encountered by the trailing bias charge tue to the modulation of the trailing-bias-charge level by the first-order trapping losses experienced by the signal-charge packets.

LOW-LOSS CCD TEST ARRAY

To demonstrate experimentally the low-loss CCD concept we have developed a low-loss CCD test chip which includes a 256-stage and a 1024-stage closed-loop low-loss CCD. In addition to low-loss signal regenerators, floating-gate output stages for non-destructive signal sensing, and input and output charge switching circuits, each of the closed-loop CCDs has been constructed with a dark current subtraction stage. The dark current subtraction technique described in this paper can extend the useful delay time of the signal in the closed-loop CCDs by more than two orders of magnitude. A schematic diagram of the 1024-stage closed-loop CCD is shown in Fig. 1.

The low-loss CCD test chip was processed following a two-level polysilicon n-channel buried-channel CCD (BCCD) technology with non-self-aligned n^+ diffusions, p^+ channel stops, 1000-Å-thick channel oxide, and n^+ polysilicon gates processed with phosphorus-doped reflow glass. The

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** A complete description of this work will be published by the authors in the September 1979 Issue of RCA Review.[2,3]

BCCD channels are 25 μm wide. The gate structure has 10-μm polysilicon gates with 5-μm spaces, thus resulting in 30-μm-long CCD stages. The closed-loop CCD structures were designed to operate as a two-phase CCD with a dc offset voltage to be applied between the storage gates and the transfer gates. The charge-corners of both closed loops were designed for a complete charge-transfer operation with the available two-phase CCD clocks.

The construction and operation of a low-loss signal-regeneration stage is illustrated in Figs. 2 and 3. The charge-coupling structure of the signal-regeneration stage is shown schematically in Fig. 2(a) in the forms of a two-phase CCD. The transfer of the charge packets in and out of the signal-regeneration stage is illustrated in Fig. 2(b) at the time instants indicated on the clock waveforms shown in Fig. 3. As shown in Fig. 2(b), the signal regeneration stage first combines the signal charge, S_1, with the contents of the trailing well, which in addition to the trailing bias charge, T_2, also contains the first order losses. Then, one clock cycle later the regenerated signal S_1 is separated from its trailing bias charge T_1. Note, the signal charge, S_1, is always followed by the trailing bias charge T_1 except during two transfers when S_1 and T_1 are together in a single well. Another charge transfer also involving first-order trapping loss that requires special attention is the transfer at time t_4 which separates the trailing bias charge T_1 and the signal charge S_1. This transfer is an incomplete (or bucket-brigade type) charge transfer.[4,5]

DARK CURRENT SUBTRACTION

The dark-current subtraction stage operates by subtracting from the CCD channel a fixed amount of charge. The construction and operation of the dark-current subtraction stage are illustrated in Fig. 4.

One of the possible limitations of the effectiveness of the dark-current subtractor is, that if the dark current is signal-dependent, the operation with a periodic subtraction of a fixed amount of dark current will lead to some form of nonlinear signal degradation of the output. The measured curves of dark current as a function of the signal charge for two different 1024-stage devices in Fig. 5 indicate that in our buried-channel CCDs there is a large range of signal for which the dark current is relatively constant.

EXPERIMENTAL RESULTS

The operation of a 1024-stage closed-loop CCD in the low-loss mode and the effect of bias charge, Q_{SO}, on the transfer losses, ϵ, are illustrated in Fig. 6. The trailing bias charge is designated as Q_{TB}. The general conclusion of the above test is that signal bias charge $Q_{SO} = 0.4\ Q_{TB}$ is sufficient to achieve the minimum transfer losses. Also, the transfer loss for negative signal pulse in the presence of large Q_{SO} is lower but still comparable to the transfer loss for positive signal pulse. The results in Fig. 6 demonstrate the effective transfer inefficiency or transfer loss, ϵ, for low-loss CCD of 2.4×10^{-7} per transfer. We define the effective transfer loss of the low-loss CCD as the transfer loss of the leading edge of an input pulse (the first "one" in a string of "ones"). The effective low-loss CCD transfer loss is

$$\epsilon = \frac{\Delta Q_{S1}(1)}{N(Q_{S1}-Q_{SO})} \qquad (1)$$

where $\Delta Q_{S1}(1)$ is the difference between the initial value of the "one" at the input (i.e., as detected in the first recirculation) and the first "one" after N transfers, Q_{S1} is the amplitude of the signal charge "one," and Q_{S0} is the signal charge "zero."

It is also interesting to note that the signal charge used in this test is $Q_{S1}-Q_{S0}=0.12$ pC, which corresponds to about $0.8\mathrm{x}10^6$ electrons. This means that while in the standard CCD mode the transfer loss of $1.6\mathrm{x}10^{-5}$ per transfer corresponds to an average charge trapping of 13 electrons, in the low-loss CCD mode the transfer loss of $2.5\mathrm{x}10^{-7}$ per transfer corresponds to an effective average charge trapping of 0.2 electrons per transfer.

The comparison of the performance of a closed-loop 256-stage CCD operating a standard clock and in the low-loss mode is shown in Fig. 7. In this figure the device is operated at a low clock frequency of f_c = 4.4KHz to illustrate the performance of the dark-current subtractor. Note, in Fig. 7(b) the signal is stored in the loop for a delay time, τ_D, of 10s, in which time the total dark current generation subtracted from the loop represent 20 full wells of charge. Our experiments also showed that the noise generated by the dark current tends to saturate at a low level maintaining a s/n_{rms} = 54 dB independent of the total delay time.

CONCLUSION

The closed-loop low-loss CCDs provide temporary storage for analog signals with non-destructive read-out. The low-loss CCD combined with the dark current subtraction technique should find applications in new CCD structures requiring a very large number of charge transfers (up to 10^6) and very long time delays (up to 10 minutes). One example of such applications is a synchronous signal correlator which was demonstrated using a 256-stage closed-loop low-loss CCD. With 100 signal recirculations we have obtained an improvement in the signal-to-noise ratio from -5.5 dB to 12 dB.

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REFERENCES

1. W. F. Kosonocky and D. J. Sauer, U.S. Patent No. 4,134,028, "Charge Transfer Circuits with Compensation for Transfer Losses," Jan. 9, 1979.
2. W. F. Kosonocky and D. J. Sauer, "Low-Loss Charge-Coupled Devices," to be published in RCA Review, September 1979.
3. D. J. Sauer, "Analysis of the Effective Transfer Losses in a Low-Loss CCD," to be published in RCA Review, September 1979.
4. W. F. Kosonocky and J. E. Carnes, "Two-Phase Charge-Coupled Devices with Overlapping Polysilicon and Aluminum Gates," RCA Review, 34, 164-202 (1973).
5. W. F. Kosonocky and J. E. Carnes, "Basic Concepts of Charge-Coupled Devices," RCA Review, 36, 566-593 (1975).

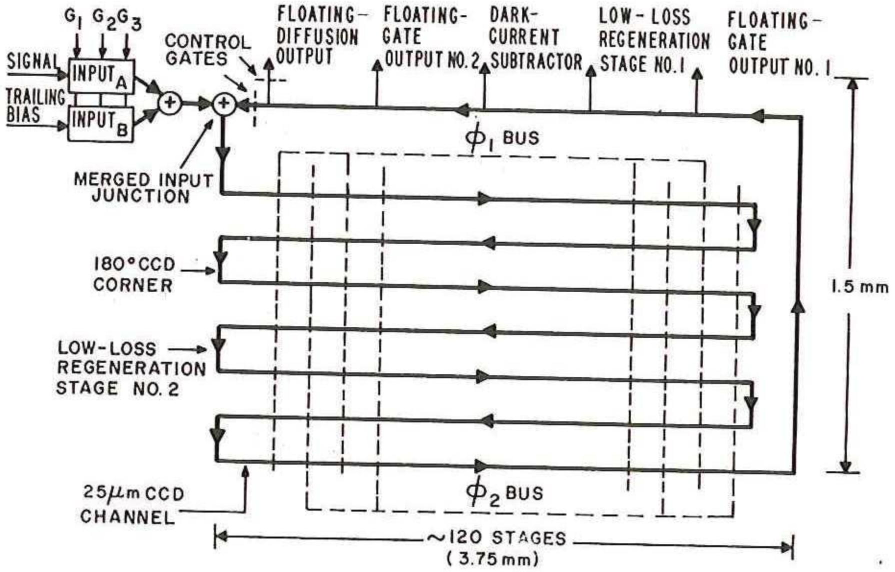


Figure 1. Schematic of the layout of the 1024-stage low-loss CCD loop.

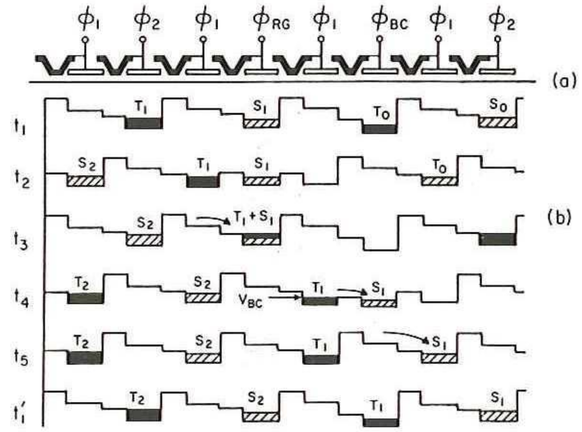


Figure 2. Low-loss CCD.
(a) Charge-coupling structures.
(b) Potential wells illustrating the operation.

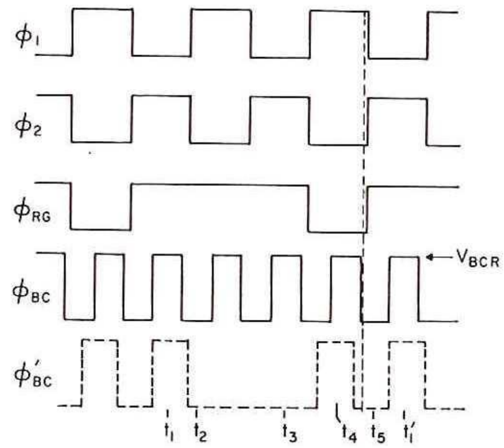


Figure 3. Clock waveforms for operation of the low-loss CCD shown in Fig. 2.

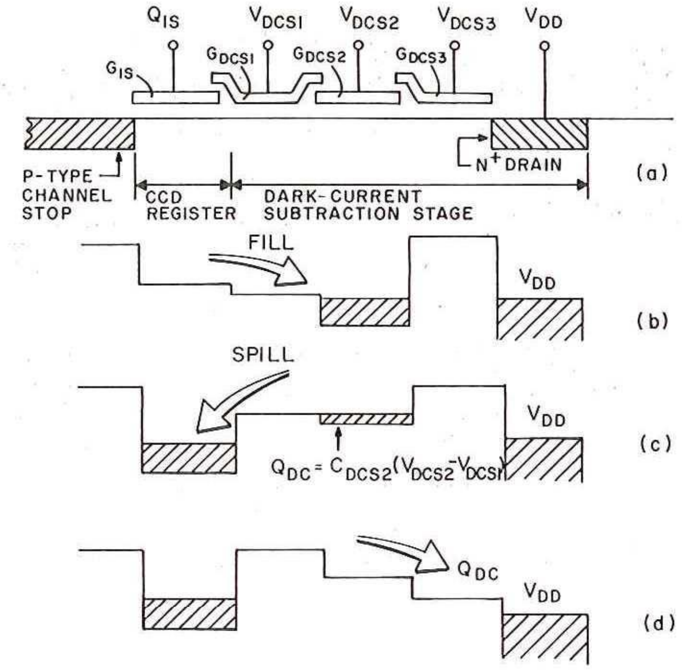


Figure 4. Construction and operation of the dark-current subtraction stage.

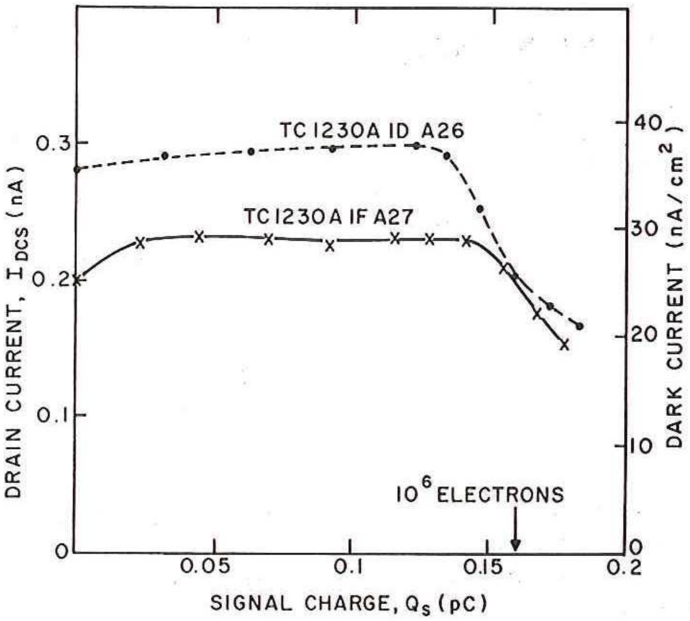
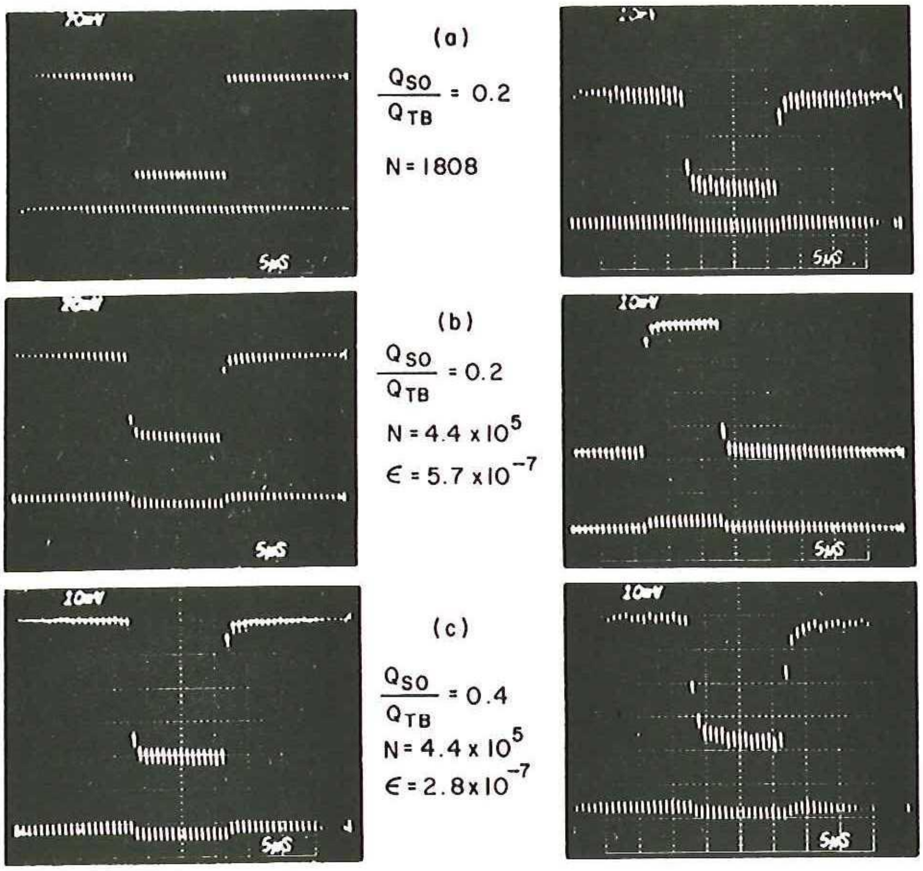


Figure 5. Variation of dark current with signal charge level.



(a) $\frac{Q_{SO}}{Q_{TB}} = 0.2$, $N = 1808$

(b) $\frac{Q_{SO}}{Q_{TB}} = 0.2$, $N = 4.4 \times 10^{5}$, $\epsilon = 5.7 \times 10^{-7}$

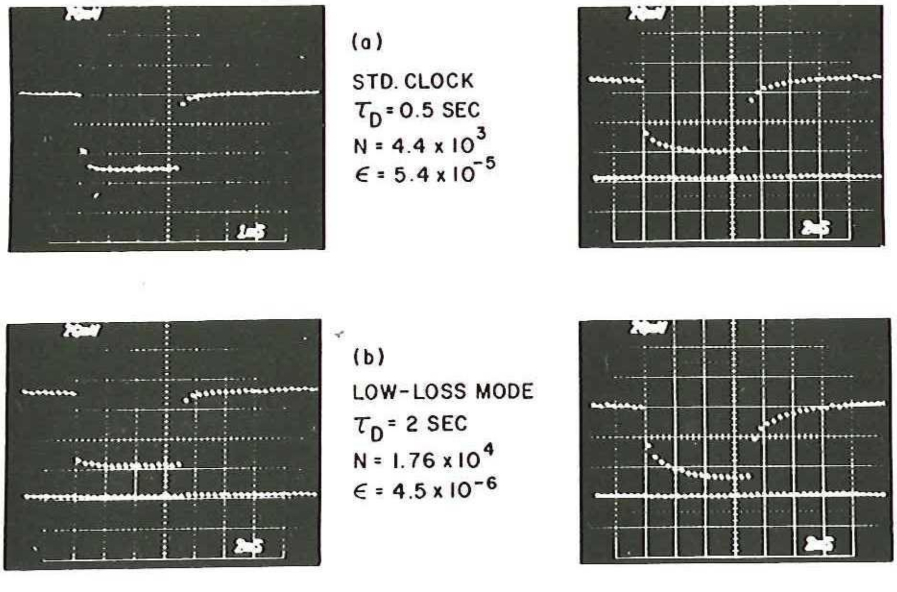
(c) $\frac{Q_{SO}}{Q_{TB}} = 0.4$, $N = 4.4 \times 10^{5}$, $\epsilon = 2.8 \times 10^{-7}$

(d) $\frac{Q_{SO}}{Q_{TB}} = 0.6$, $N = 8.8 \times 10^{5}$, $\epsilon = 2.4 \times 10^{-7}$

(e) $\frac{Q_{SO}}{Q_{TB}} = 0.8$, $\frac{Q_{SI}}{Q_{TB}} = 0.2$, $N = 4.4 \times 10^{5}$, $\epsilon = 2.8 \times 10^{-7}$

(f) $\frac{Q_{SO}}{Q_{TB}} = 0.4$, $N = 2 \times 10^{6}$, $\epsilon = 2.5 \times 10^{-7}$

Figure 6. Comparison of transfer loss, ϵ, of closed-loop low-loss 1024-stage CCD at $f_c = 2.2$ MHz for various "zero" signal charge levels, Q_{SO}, and number of transfers, N.



(a) STD. CLOCK
$\tau_D = 0.5$ SEC
$N = 4.4 \times 10^{3}$
$\epsilon = 5.4 \times 10^{-5}$

(b) LOW-LOSS MODE
$\tau_D = 2$ SEC
$N = 1.76 \times 10^{4}$
$\epsilon = 4.5 \times 10^{-6}$

(c) LOW-LOSS MODE
$\tau_D = 5$ SEC
$N = 4.4 \times 10^{4}$
$\epsilon = 5 \times 10^{-6}$

(d) LOW-LOSS MODE
$\tau_D = 10$ SEC
$N = 8.8 \times 10^{4}$
$\epsilon = 4.7 \times 10^{-6}$

Figure 7. Performance of closed-loop 256-stage CCD at $f_c = 4.4$ kHz: with the dark-current subtractor ON with standard two-phase clock mode in (a), and low-loss mode in (b), (c), and (d).