

CONTROL OF THRESHOLD NON-UNIFORMITIES IN CHARGE-COUPLED DEVICES

N. A. Foss*, W. Larson**, and C. Carrison*

INTRODUCTION

Advanced systems using CCD signal processors call for increased performance levels and reduced system size, weight and power factors. This generally means the development of CCD structures with a greater number of redundant cells and increased packing densities. As the processor packing density becomes larger and the photolithographic tolerances tighter it becomes necessary to develop CCD processor circuits which utilize fewer structural components in order to maximize the CCD readout electronics processing yields. The complexity of the circuit design is highly dependent, however, on several factors with one of the primary factors being the CCD threshold variations, ΔV_T .

The ability to minimize the threshold variations through proper device processing procedures not only results in less complex coupling circuitry, but in the realization of unique processing structures (ref. 1 and 2). This paper first discusses the effect of threshold non-uniformity on various processing functions. Parametric relationships are then developed which show the influence of gate oxide thickness, fixed interface charge, substrate doping, implant doping, and mobile ionic charge on the threshold uniformity.

State-of-the-art threshold non-uniformity levels have been consistently achieved on Honeywell's double-polysilicon gate N-channel CCD's. The results of threshold variation measurements on both linear and 2-dimensional CCD multiplexers will be described for the case of input-to-input variations, variations between chips, between wafers and between processing runs. Effects of operating temperature and channel length effects will also be discussed.

PARAMETRIC EFFECTS ON THRESHOLD UNIFORMITY

The processing parameters which effect the CCD threshold uniformity have been analyzed and will be described for Honeywell's N-channel process.

The general equation for an N-channel enhancement mode MOSFET is given by:

$$V_{TE} = -\phi_{ms} - \frac{Q_{ss} t_{ox}}{\epsilon_{ox}} - \frac{Q_o t_{ox}}{\epsilon_{ox}} + \phi(inv) + Q_B/C_{ox} \quad (1)$$

In this analysis, the work function, ϕ_{ms} is approximated as the difference in Fermi level of the polysilicon gate and channel using non-degenerate (Boltzmann) statistics. The terms $Q_{ss} C_{ox}/\epsilon_{ox}$ and $Q_o C_{ox}/\epsilon_{ox}$ are the voltage shifts due to fixed state interface charge and positively charged mobile ionics. $\phi(inv)$ is the contribution due to bending at strong inversion and by convention, $\phi(inv) = 2\phi_F$. The last term, Q_B/C_{ox} is the charged induced in the silicon with a surface potential $\phi(inv)$. The threshold equation can then be rewritten:

*Honeywell Systems & Research Center, Minneapolis, MN

**Honeywell Solid State Electronic Center, Plymouth, MN

$$V_{TE} = -KT \ln \left[\frac{N_G (N_I + N_B)}{n_i^2} \right] - \frac{Q_{SS} t_{ox}}{\epsilon_{ox}} - \frac{Q_o t_{ox}}{\epsilon_{ox}} + 2KT \ln \left[\frac{N_I + N_B}{n_i} \right] + \left[4KTq \epsilon_{si} (N_I + N_B) \ln \left(\frac{N_I + N_B}{n_i} \right) \right]^{1/2} \frac{t_{ox}}{\epsilon_{ox}} \quad (2)$$

Note that the total doping concentration in the channel is given by the sum of the substrate and implanted concentrations, $(N_I + N_B)$. A definition of terms is: K = Boltzmann's constant, $T = 300$ K, n_i = Intrinsic carrier concentration, $\epsilon_{ox} = \text{SiO}_2$ dielectric constant, ϵ_{si} = Silicon dielectric constant, q = Electronic charge, N_G = Poly Gate doping level, N_I = Implant doping level, and N_B = Substrate doping level.

It can be seen that the control of threshold uniformity is determined by the uniformity of the following process variables:

1. N_G , poly doping level
2. N_I , implant doping level
3. N_B , substrate doping level
4. Q_{SS} , fixed state interface charge
5. t_{ox} , gate oxide thickness
6. Q_o , mobile ionic charge

Using Monte Carlo methods, threshold uniformity may be predicted for given variations of each of the six process parameters. A sensitivity analysis of each process parameter was performed to determine their relative importance. In Figure 1, the one sigma threshold variation is plotted versus the parameter $(1\sigma/\bar{X} \times 100)$ for each process variable with five other parameters having a sigma of zero. From this plot, it can be seen that the relative importance of each variable in decreasing order of importance is oxide thickness, implant doping, Q_{SS} , substrate doping, and finally, ionic charge level.

Measurements of within a wafer, wafer to wafer and run to run variations for each of the six processing parameters was used in conjunction with equation (2) and the computed threshold variations calculated as shown in Table I.

Table I. Calculated Threshold Uniformity for $2\frac{1}{2}$ " wafers (using data on measured parameter variations).

	Across $2\frac{1}{2}$ " Wafer	Between Wafers Within Run	Run-Run
$1\sigma V_T$	23mv	40mv	165 mv

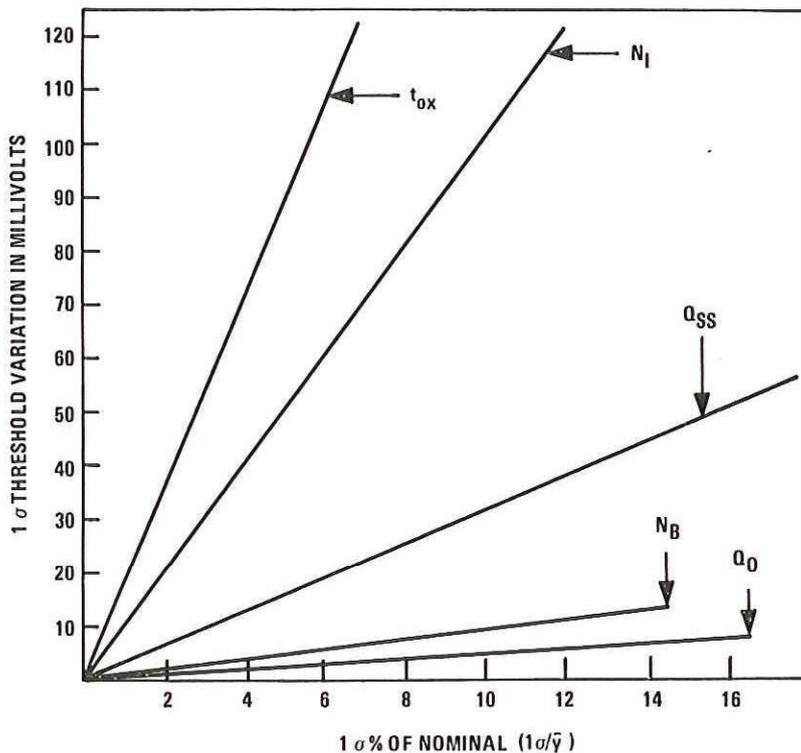


Figure 1. Sensitivity Analysis of Threshold Variations vs. 1σ of nominal value (in %) of parameter characterized.

THRESHOLD UNIFORMITY TEST RESULTS

The CCD threshold uniformity has been measured on a total sample of 56 randomly selected wafers fabricated in nine separate runs over a period of 8 months. These measurements were made on Honeywell's #2181 CCD chip (32 x 32 element MUX) and the #2178 CCD chip which had both 16 stage and 128 stage linear multiplexers. The data will be presented in several forms which include:

- Variations between inputs on the same chip.
- Variations from chip-to-chip on same wafer.
- Variations from wafer-to-wafer from same processing run.
- Variations from run-to-run.

Figure 2 shows the input gates threshold distribution measured on 16 stage CCD multiplexers which span a distance of 25 mils each. The average threshold value for each chip has been adjusted to the "0" position on the abscissa. The 1σ variation is about 2mV for the 512 individual gates tested.

Figure 3 shows the threshold distribution measurements made on 128 stage CCD multiplexers. In this case the active chip width is 210 mils. The 1σ variation for this large chip is about 3mV. The primary difference between the small and large chip measurements is the total peak-to-peak spread in ΔV_T which is only about a factor of 2 larger for the 210 mil chip.

Measurements made over a sample of 56 wafers (both 2181 and 2178 CCD circuits) indicate the degree of repeatability of obtaining a pre-determined threshold voltage. Table II shows the measured uniformity along with the calculated uniformity presented earlier in Table I.

	Across 2-1/2" Wafer	Within Run	Run-Run
$1\sigma V_T$ (measured)	33mV	60mV	117mV
$1\sigma V_T$ (calculated) (from Table I)	23mV	40mV	165mV

Excellent agreement is thus seen between the model presented in equation (2) and the measured ΔV_T values.

EFFECTS OF TEMPERATURE ON ΔV_T

The expression for the threshold variations (equation 2) does not explicitly show how the CCD operating temperature affects the threshold uniformity. Since the main factors influencing the uniformity are the oxide thickness and implant doping density it appears as if the threshold variations should be independent of operating temperature.

Measurements made on 128 stage multiplexers at various operating temperatures ranging from room temperature down to 93K shows the threshold uniformity to be completely independent over the operating temperature (300-93K).

EFFECT OF GATE SIZE ON ΔV_T

As gate length and width are reduced below approximately $4\mu\text{m}$, significant changes in both threshold voltage and threshold voltage uniformity occur. As can be seen in Figure 5, short and narrow channel effects become increasingly important below $4\mu\text{m}$. In Figure 6, the threshold voltage uniformity is plotted as a function of gate length for enhancement mode transistors with a constant l/w ratio of $1/4$. Since the threshold voltage is a strong function of gate length, the threshold voltage uniformity has been normalized by computing the parameter $\sigma/\bar{V}_T \times 100$ where σ is the measured standard deviation across a wafer for a particular gate dimension and \bar{V}_T is the average threshold voltage.

In the previous discussion, it has been shown that the threshold voltage of large geometry devices can be directly attributed to process variations of the parameters in the classical threshold equation given by (1). However, the decrease in threshold uniformity for gate lengths less than $3\mu\text{m}$ can be attributed to factors other than those presented in the previous analysis. Two important factors are:

(1) Variation in dimensional tolerance will cause significant variations in threshold due to short and narrow channel effects. As can be seen from Figure 5 a $\pm 0.25\mu\text{m}$ line width control for $1.5\mu\text{m}$ nominal gate length will result in a $\pm 20\%$ threshold variation due to short channel effects along. It is expected that improved processing such as E-beam lithography and parallel

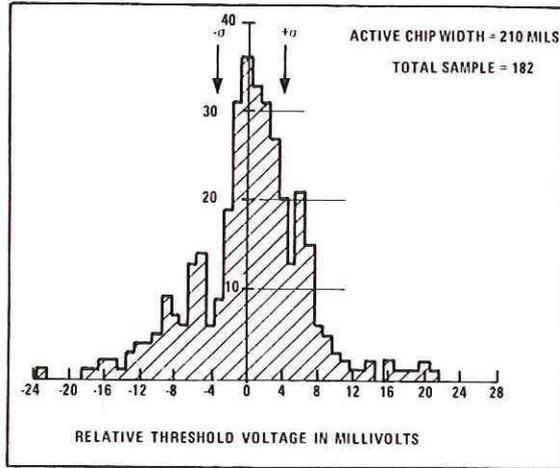
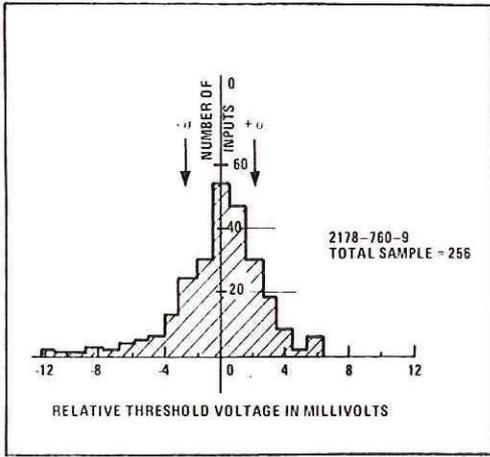


Figure 2. Input Gate Threshold Voltage Distribution Measured On 16 Stage MUX (Chip Width = 25mils).

Figure 3. Threshold Voltage Distribution Measured on 128 Stage MUX (Chip Width = 210mils).

Measurements made on test structures across 2-1/2" wafers resulted in 1 σ variations across the 2-1/2" span of 33mV (total sample measured = 392). We can combine the results from these measurements which span different lengths to determine how ΔV_T varies with chip size. This is shown in Figure 4.

As can be seen from this, outstanding uniformity is achieved on very large CCD chip sizes.

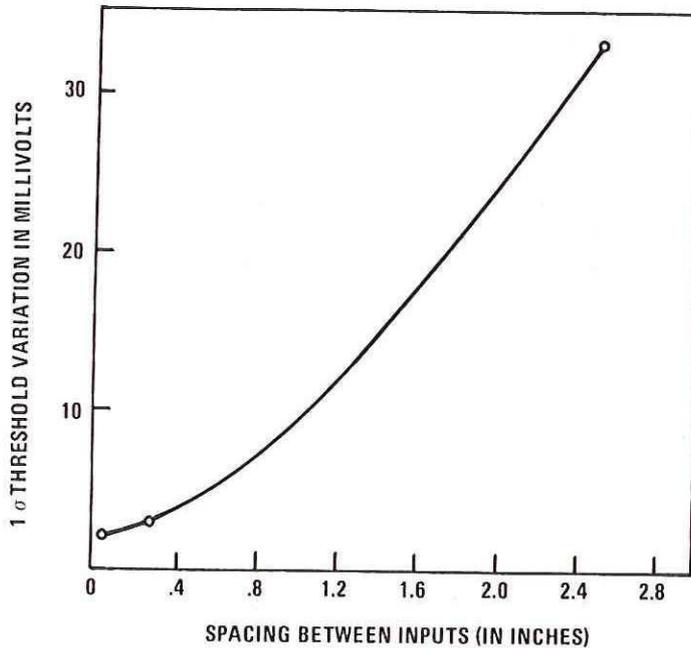


Figure 4. ΔV_T as a Function of Spacing Between Inputs (Cumulative Data Averaged Over 56 Random Wafers).

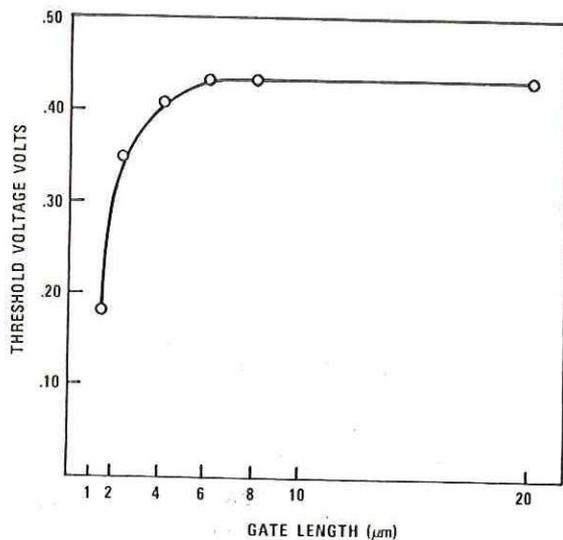


Figure 5. Enhancement Threshold Voltage vs. Gate Length ($w = 20\mu\text{m}$).

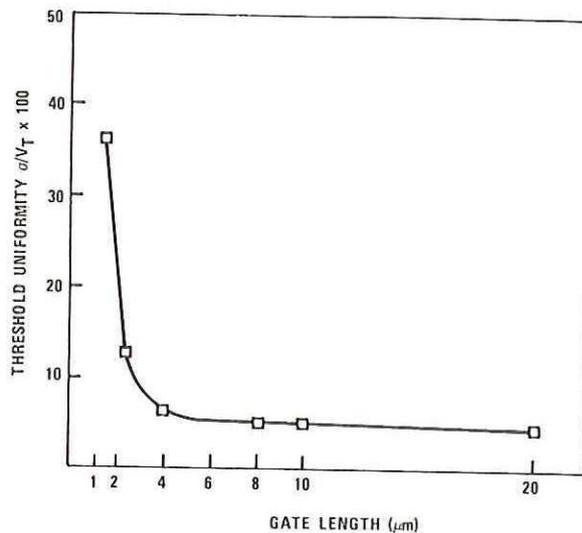


Figure 6. Threshold Uniformity vs. Gate Length ($l/w = 1/4$).

plate plasma etching coupled with improved device structures will improve small geometry threshold control.

(2) As gate dimensions approach $1\mu\text{m}$, statistical fluctuations in both interface changes and dopant atom distribution can be an increasing important factor (3).

CONCLUSIONS

Excellent process control has enabled us to consistently achieve outstanding threshold uniformities in signal processing CCD structures. Threshold variations of 3mV (1σ point) across 210 mil chips allow us to design less complex detector/CCD coupling circuitry, thereby resulting in higher packing density structures. The 1σ threshold variations across a $1''$ chip are below 10mV thereby permitting the design and fabrication of extremely large linear and 2-dimensional CCD processing structures. For very small channel lengths the ΔV_T uniformity control is shown to require special processing care to maintain these low levels.

REFERENCES

- 1: J.D. Joseph, N.A. Foss, C.L. Carrison "A Fully Analog, 128-Stage CCD Correlator", Proceedings, SPIE International Technical Symposium, Aug. 1978.
- 2: C. Carrison, N.A. Foss, "Performance Characteristics of a CCD Analog Memory/Signal Processor". Proceedings, 1979 CCD Conference, Edinburgh.
- 3: Keyes, R.W., IEEE Journal of S.S. Circuits, Aug. 1975, p.245.