50 MHz TIME DELAY AND INTEGRATION CCD

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ABSTRACT

Time delay and integration CCDs are now finding wide application in the fields of IR imaging, sonar beam-forming and transversal filters. This paper reports on the design and performance of a 12 input TDI processed using a two layer polysilicon n-channel buried channel technology.

A major consideration during the design phase was the need for simplified drive requirements. 1½ phase clocking is made possible for the CCD by using barrier implants under the second polysilicon layer, and other necessary clocks (reset and sample) are derived from the input clock by on-chip drive circuitry. All DC bias voltages are also generated on-chip. The only requirements for driving the TDI therefore are a one phase input clock, +15, 0, -5 volt power supplies, and decoupling capacitors for the bias voltages.

The on-chip clock generators allow a clocking frequency which has hithero not been possible. By careful design, 50 MHz clocking was achieved over the full military temperature range (-55°C to +125°C) allowing 13 MHz signal bandwidth to be processed.

PRINCIPLE OF OPERATION

The inputs to the TDI are arranged such that the contributions from the inputs are integrated with a time stagger between each one. In the device reported here, this time stagger represents two clock periods T (see figure 1). Expressed mathematically, the output X(t) is given by

$$X(t) = \sum_{j=1}^{n} I_j \, (t - 2 \, (n + 1 - j)T)$$

where n is the number of inputs, and I_j the jth input.

A linear IR imaging array scanned across an image provides essentially identical signals but with a built in time stagger between its outputs. By passing these signals to a TDI, the coherent signals will be integrated, but incoherent noise from each detector will give only an r.m.s. summation. Hence a processing gain of $\sqrt{n}$ will be realised (ref 1).

In beam-forming applications (ref 2) a sonar echo is received by a linear array of transducer detector elements. Time stagger will be introduced into the outputs from these detectors due to the angle made between them and the return signal. By sweeping the TDI clock through an appropriate frequency range, a peak at the output will occur when coherence is achieved between the input signals.

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CHIP DESIGN

One of the major considerations in the chip design was the requirement for 20 MHz clocking even for devices processed with 'worst case' processing parameters and operation over the full military specification temperature range. Another consideration was to make the device as simple to operate as possible (ref 3). The use of on-chip clock logic and drivers satisfies both these requirements - satisfactory external clock logic and driving circuitry is virtually impossible above 10 MHz.

A buried channel CCD was used in order to make use of its superior transfer characteristics over surface channel CCD, especially at high clocking frequencies. Since the number of transfers is low (48) $N\varepsilon$ effects are only observable at high clock rates, and even then are hardly observable (see fig 8).

In order to set the input DC offset to its optimum level, all the inputs are AC coupled with the offset level derived from on-chip bias circuitry.

Many different possibilities exist for the input circuitry to the CCD and a careful analysis was required in order to minimise harmonic distortion. Fill and spill techniques allow good linear relationships between input voltage and CCD charge but distortion will be introduced at the output of the CCD due to the non-linear characteristics of the depletion capacitance of the output diode. It was therefore felt that the best linearity would be achieved by matching the non-linear components at the output and input to the CCD,and so an input technique setting the surface potential was adopted (fig 2). By resetting the output node to V_{DD} (+15V) and keeping V_{ref} at V_{DD} the harmonic distortion was minimised.

With this diode cut-off type of input, the length of the sample gate is a potential speed limiter. In order for its length not to be dependent on mask misalignment, it is necessary to make the gate in polysilicon 1. At first, it would appear that this is not possible due to the fact that the reference electrode would require to be polysilicon 2 conflicting with the polysilicon 2 clock phase electrode (necessary in order to maintain the directionality barrier). However, this problem was overcome by positioning the start of the buried channel midway between a double width polysilicon 1 clock phase electrode so that a minimum length (5 μm) polysilicon 1 sample gate could be used.

The output buffer consists of a 3 stage source follower with sample/hold transistor between the 1st and 2nd stages (fig 3). Three stages are necessary in order to guarantee 250Ω output impedance and 50 MHz sampling rate. Since the source/drain voltage of the sample transistor can never exceed the maximum signal voltage range (<4v) it was possible to use a transistor with a channel length of 5μm, thus minimising sample clock breakthrough.

Particular attention was paid to optimising the clock generation circuitry (fig 4). Since $\emptyset_R/\emptyset_D$ are essentially in phase with the input clock, it was possible to use a clocked logic gate structure to generate these waveforms, thereby minimising the power consumption. This obviously was not possible for the sample clock ($\emptyset_S$), so that a more standard approach was necessary. It is interesting to note that simulation showed that a higher clocking rate for a given power consumption could be achieved by using a pseudo push-pull buffer rather than using a standard logic gate, despite the extra propagation delay involved. In order to optimise the transistor sizes and their associated input gate capacitances in terms of operating frequency, it was necessary to write a Fortran Computer program to calculate the transistor aspect ratios sizes for a given overall power consumption. As a precaution, an alternative metal mask was made so that the necessary clocks could be driven externally, but in the

event this was not needed.

Several DC bias voltages are required for various parts of the circuit - for the DC phase of the CCD, for the load devices of the source follower stage and for the DC offset of the input signal. These voltages are easily generated by using pairs of transistors acting as voltage dividers. These nodes may be accessed on the chip via pads in the normal manner. In this way the generated voltages can be monitored and external decoupling capacitors added. By this means, the bias voltages may be driven from an external source if necessary.

An SEM photomicrograph of the chip is given in fig 5.

CHARACTERIZATION

The most important feature to arise from these measurements was the ability of the device to operate at a clocking frequency of 50 MHz over the full military specification temperature range. In fact, the device has not been tested beyond 50 MHz due to the limitation of the pulse generator. Frequency response measurements were made for 20 MHz and 50 MHz clocks and the result is shown in fig 6.

Fig 7 illustrates the integrating ability of the TDI when a square wave signal is applied to all inputs simultaneously - in this case the clock rate is 500 KHz. The sample breakthrough can be clearly seen and may be filtered out if necessary. Fig 8 shows the same as fig 7 but for a 50 MHz clock, and Fig 9 shows a 12.5 MHz sine wave applied to alternate inputs.

Without going into further details, Table 1 gives figures for some important performance parameters at 25°C.

TABLE 1

Characteristic	Typical Value	Units
Sample breakthrough	400	mV
Signal bandwidth[1] at 50 MHz	13	MHz
Total insertion gain	-3.1	dB
Dynamic range [2]	68	dB
Harmonic distortion [3]	0.20	%
Output impedance	160	Ω
Power consumption	250	mW

Note 1 -3dB point
Note 2 Input signal V_{pk-pk} increased to give 2% harmonic distortion
Note 3 1 volt 10 KHz signal applied to all inputs

ACKNOWLEDGEMENTS

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REFERENCES

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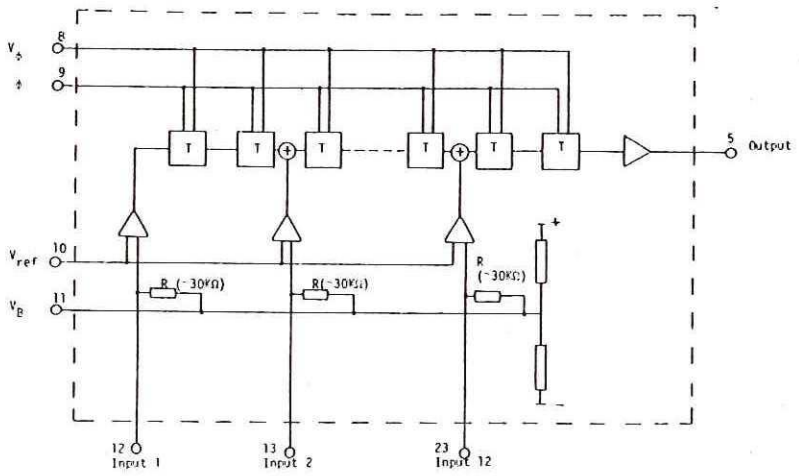


FIGURE 1: Device Schematic

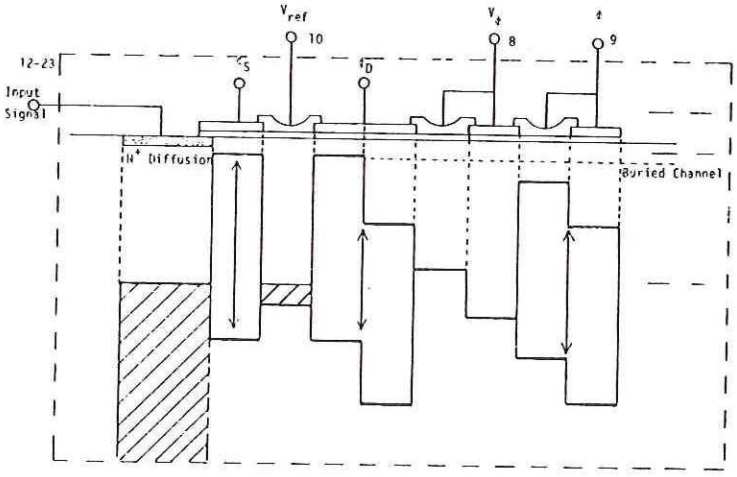


FIGURE 2: Input Circuitry

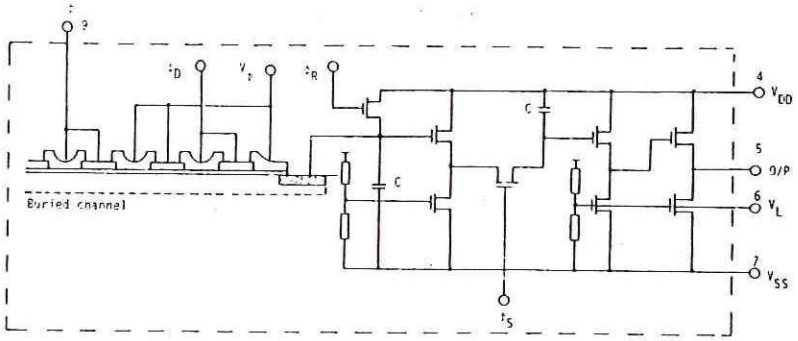


FIGURE 3: Output Circuitry

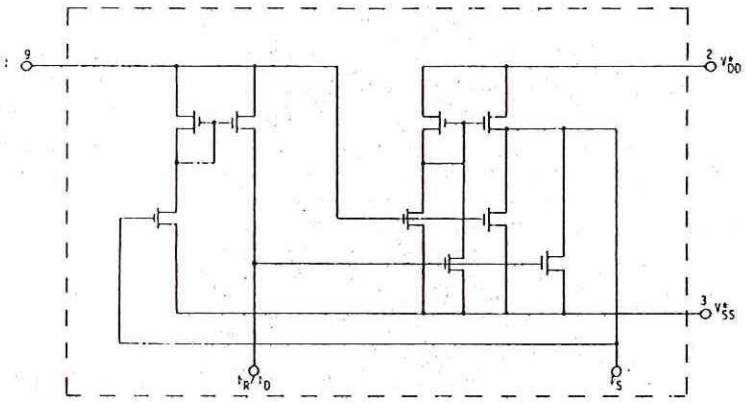


FIGURE 4: On-Chip Clock Logic/Driver Circuit

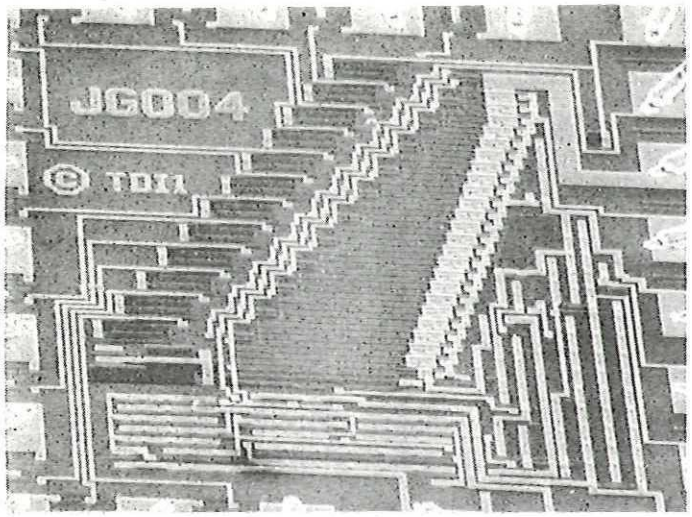


FIGURE 5: SEM Photomicrograph of the TDI.
The CCD and 12 inputs are in the centre, clock logic at the bottom and output buffer to the right of the picture.

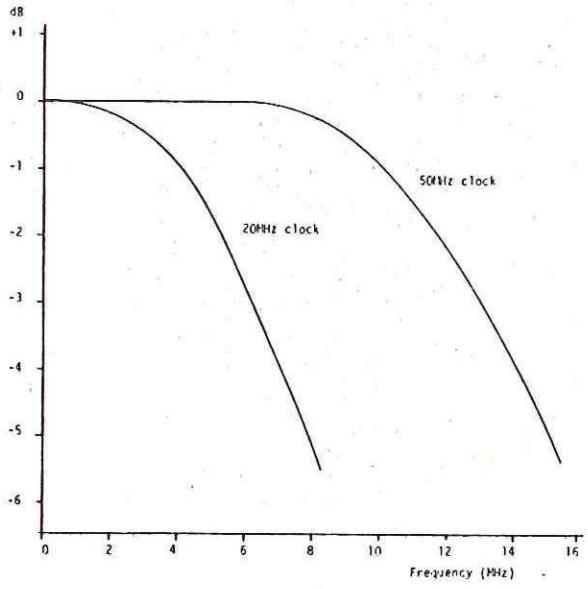
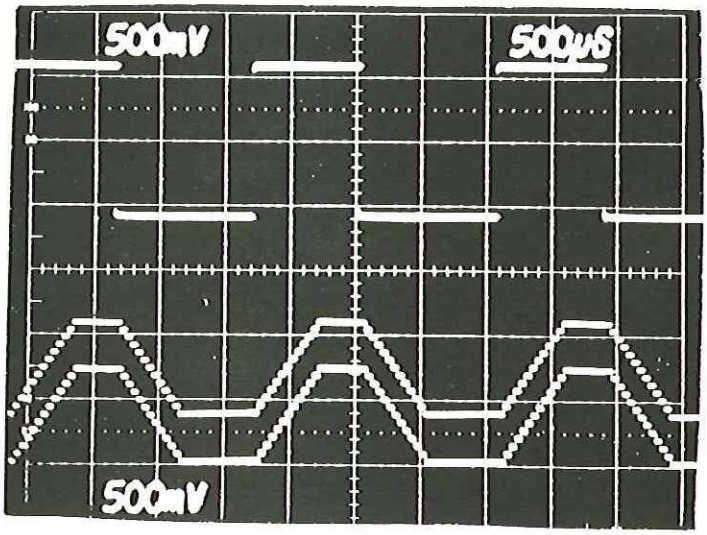


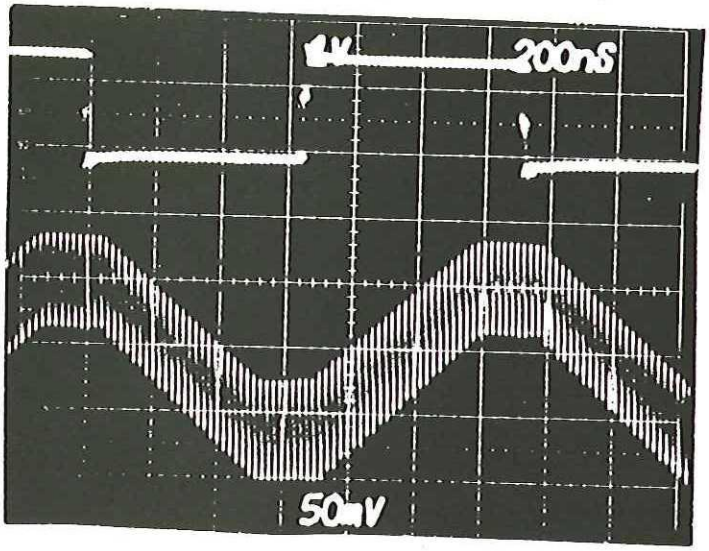
FIGURE 6: Frequency Response of TDI.



INPUT
All inputs connected together

OUTPUT

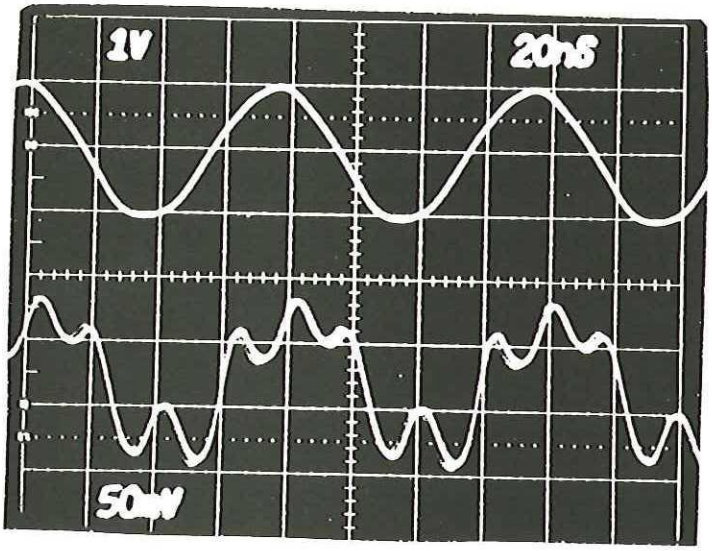
FIGURE 7: TDI Output (500 KHz clock)



INPUT
All inputs connected together

OUTPUT

FIGURE 8: TDI Output (50 MHz clock)
(x10 probe)



INPUT
Alternate inputs connected together
remainder grounded

OUTPUT

FIGURE 9: 12.5 MHz sine wave input
(50 MHz clock)
(x10 probe)