A CCD BANDWIDTH COMPRESSOR FOR AIRBORNE RADAR APPLICATIONS

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Abstract

CCD architectures for capturing high speed transients are reviewed. The relative merits of different structures together with various input techniques suitable for high speed signal input are presented. To illustrate the performance and capability of CCDs for these purposes a 321 cell, 100 MHz, 3 phase CCD bandwidth compressor was constructed and its performance measured. The total system was designed to accept data having an input bandwidth of 50 MHz and subsequently to clock these data out at rates up to 2 MHz for recording on magnetic tape. Since power requirements were at a premium, low overall power consumption and high speed performance were essential design goals.

Introduction

High speed transient recording employing CCDs has been described previously(1,2,3). CCD analogue shift registers are ideal for bandwidth compression (time expansion) or bandwidth expansion (time compression) principally because it is easy to vary the clocking rate. Basically the CCD shift register is first clocked at a high frequency ($\sim$ 100 MHz) for the requisite number of bits thus providing fast sampling of the data until the register is filled with data. The device is then clocked at a lower frequency ($\sim$ 2 MHz). Thus the analogue samples are read out at a more manageable rate, suitable for digitising by a low speed analogue to digital converter.

Previous CCDs for this application have used a single CCD channel and have employed a serial in/serial out architecture. The n^{th} sample of a total of N points is then transferred through n high speed clock cycles and N-n low speed cycles. Since charge transfer is a function of frequency this results in a non-uniform transfer inefficiency across the sampled waveform. The effective transfer inefficiency is in practice limited by the higher clock rate performance, thus its effect may be minimised in a serial/parallel/serial structure. This reduces the total number of high speed transfers by a factor p, the number of parallel channels used, and still maintains the number of stored samples. However a further non-uniformity is introduced through differences in the channels and will appear as fixed pattern noise at the output. The performance is then improved if the number of parallel channels is set to give a pattern noise whose effect is less than that of the equivalent number of high speed transfers in a serial structure.

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Our device uses a parallel channel arrangement but replaces the serial aspect with a multiplexing operation. The data samples are multiplexed at the input into three parallel channels, using the three phase clocks to select automatically the channel into which each data sample is fed. Thus the number of parallel channels corresponds to the number of phases. While in a single channel p-phase device, data is sampled once every p^{th} phase, in our multichannel device, data is sampled on every phase, thus multiplying by p, the number of parallel channels, the effective sampling rate. In addition, for a given total number of samples, the number of transfers is reduced by a factor of p. Thus this architecture minimizes the number of transfers, and reduces the necessary clock rate, thus utilizing the clock generators in an optimum way.

Transfer Efficiency Considerations

The transfer function (in z notation) for a single channel CCD with no multiplexing is given by[4]

$$H(z) = \left(\frac{(1-\bar{e})\ z^{-1}}{1-\bar{e}\ \ z^{-1}}\right)^{n} \qquad \ldots\ldots\ldots\ (1)$$

$$z = \exp\ (j2\pi f/_{fc})$$

where n is the total number of CCD stages, $\bar{e}$ is the transfer inefficiency per stage and fc is the clocking frequency. If $\bar{e}$ is very small (1) reduces to

$$|H(z)| = \exp[\ -n\bar{e}\ (1 - \cos\ 2\pi f/_{fc})\ ] \qquad \ldots\ldots\ldots\ (2)$$

For a p-way multiplexed device the transfer function is:

$$H(z)^{(\text{MULTIPLEXED})} = [\frac{(1-\bar{e})}{1-\bar{e}z^{-p}}]^{n/p}\ z^{-n} \qquad \ldots\ldots\ldots\ (3)$$

which simplifies as before to

$$|H(z)| = \exp[\ -\frac{n\bar{e}}{p}\ (\ 1-\cos\ p\ 2\pi f/_{fc}\ )\ ] \qquad \ldots\ldots\ldots\ (4)$$

Comparing (2) and (4) shows that a multiplexed device exhibits considerably less dispersion than a single CCD delay line. Although less smearing of the signal results, it occurs over a longer time period; the charge now smears not into the next adjacent time slot but into the p^{th} time slot following output demultiplexing.

The transfer function for the two cases is shown in Fig 1. Multiplexing decreases the magnitude of the ripple in the CCD pass band but its periodicity is increased.

Another technique for improving effective transfer efficiency is to employ feedback compensation. The fractional transfer loss $n\bar{e}$ is first measured. The ideal transfer function, ie where $\bar{e} = 0$, can then be more closely approximated by subtracting the true loss, $n\bar{e}Vc_c$ of the i^{th} output sample, Vi, from the next sample, V_{i+1}. Theoretically the transfer function for a first order compensated CCD becomes

$$H(z) = \left(\frac{(1-\bar{e})^{z^{-1}}}{1-\bar{e}\ z^{-1}}\right)^{n} \quad (1-n\bar{e}z^{-1}) \qquad \text{.......... (5)}$$

which simplifies with the same approximations as before to

$$|H(z)| = 1-n\bar{e} + n^{2}\ \bar{e}^{-2}\ (\text{Sin}^{2}\ 2\pi f/_{fc} - \cos^{2}\ 2\pi f/_{fc} + \cos\ 2\pi f/_{fc})$$

$$\text{.......... (6)}$$

The theoretical improvement in frequency response is shown in Fig 2 and is considerably improved since the variation is now only of the order of $(n\bar{e})^2$. Other recursive compensation techniques have been discussed by Dutta Roy and Das[5].

The proposed implementation is shown in Fig 3, where $n\bar{e}$ may be made variable to allow for charge transfer non uniformities across the output waveform.

Multiplexed CCD Implementation - Chip Architecture

A 3-phase - 3-way multiplexed CCD was therefore designed and manufactured at RSRE as an initial investigation into multiplexed structures. The first device shown in Fig 4 has 321 samples, but longer devices (4 phase, 1024 bits, and 3 phase, 1026 bits) have also been designed.

The device shown in Fig 4 is an n channel structure fabricated on a p type substrate and has overall dimensions of 3.1 x 1.3 mm^2 and a cell size of 21 μm x 50 μm. It employs three identical parallel channels 50 μm wide delineated by p+ channel stops. Automatic input and output demultiplexing is provided by staggering the three inputs and outputs such that each input is sampled in turn during each appropriate clock phase. Fig 5 shows the input structure in more detail. The two-gate input structures on each channel have a common reference electrode (IPG) and each of the other input gates (IG1-IG3) are fabricated on the same level of polysilicon. Since each phase electrode uses a different polysilicon level, a small diffusion region separates IG1-3 from the next phase electrode. Threshold voltage variations from one level of polysilicon to the other thus do not produce channel to channel mismatch. There may still be a slight threshold voltage variation (of the order of ten milivolts) from channel to channel, however, even under the same level of polysilicon, due to substrate doping fluctuations, and therefore each input gate is separately addressable to allow fine tuning of the balance between channels.

Various input techniques for high speed CCDs have been discussed by other authors[1,2]. Many have chosen a charge partition or pulsed input gate technique where an input gate is pulsed rapidly off, leaving a charge packet under the adjacent gate, whose amplitude is determined by the gate potential or the input source diffusion potential. This should be appreciably faster than input charge equilibration techniques such as phase referred[6] or fill and spill[7]. However considerable additional high speed circuitry would be necessary for the gating pulse generation. We have instead employed a simple phase referred input method which does not require any additional circuitry. This is an easy technique to implement; the appropriate input diode is connected to the phase immediately following the metering well in each channel, eg phase 1 in the lower channel, phase 2 in the second and so on. At the output a demultiplexing structure similar to the input is employed so that each charge packet will be fed through a common amplifier/reset system.

Results

A number of simple surface channel versions of the device shown in Fig 4 have been tested. Buried channel versions exhibit better transfer efficiency.

The necessary driver circuitry for the system is provided off-chip. A block diagram is shown in Fig 6 together with a photograph of the completed pc board. A start pulse initiates the control logic to read in the input data by switching the 100 MHz oscillator through the multiplexer and drivers to the CCD. A divide by 107 counter stops the high speed clocks when the device is full and data is then read out at the slower 2 MHz rate. In the change over period, from the 100 MHz to the 2 MHz rate, it is essentially that one of the phases is held high with the others off. If this is not the case, and the 2 MHz clock does not start up in a controllable manner then data may be lost. When the data has been read out the control logic is enabled to accept another start pulse and the cycle repeated. The entire board including the CCD occupies an area 22 cm x 12 cm and employs MECL 10K for the high speed logic. Total power dissipation at 100 MHz is 7.5W.

Fig 7 shows results obtained at an input sampling rate of 100 MHz. The output is clocked out at approximately 2 MHz. The photograph of the triangular waveform gives an indication of the linearity and degree of channel to channel matching obtainable with the device. Results for a square wave input signal clearly show the effects on transfer efficiency resulting from multiplexing. More detailed results of the characteristics of this device are given in table 1. Reasonable linearity and dynamic range are obtainable even with a surface channel CCD operating at such high sampling frequencies. A buried channel version will clearly give enhanced transfer efficiency and linearity and should be capable of operating at several hundred Megahertz. More detailed results including an analysis of the charge input and output will be given in a later paper.

Conclusion

Various structures for high speed transient recording have been discussed. A simple surface channel multiplexed CCD has been shown to be capable of sampling data at 100 MHz while buried channel 4 phase versions should bring 200 MHz easily within reach.

Biblography

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TABLE 1

DEVICE CHARACTERISTICS

Size	$3.1 \times 1.3\ mm^2$
Record Length	321
Sampling frequency	100 MHz
Output data rate	2 MHz
Transfer$^{(max)}$ inefficiency	$\sim 3 \times 10^{-3}$
Dynamic range	47 db
Linearity	>30 dB
Channel to channel non-uniformity	1%
PCB Size	220 mm x 120 mm
Power dissipation	7.5 W

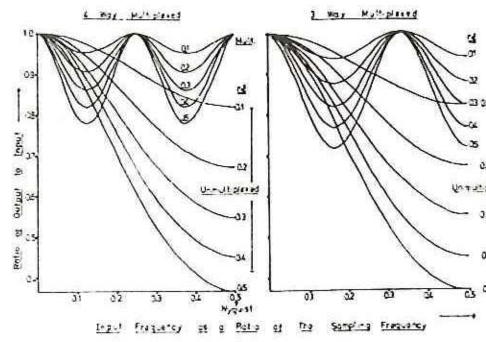


Fig 1 Comparison of Unmultiplexed / Multiplexed CCDs

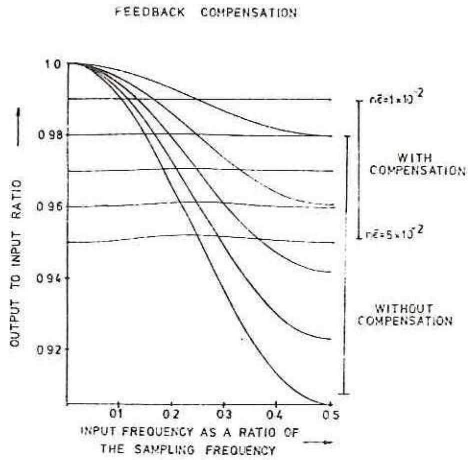


Fig. 2 Transfer Ineffiency Compensation

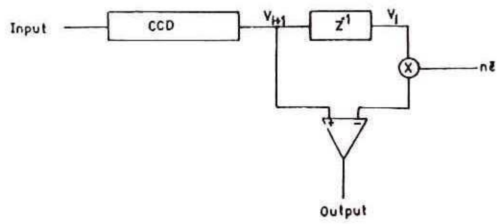


Fig 3 Compensation Circuitry

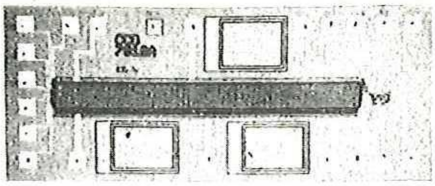


Fig 4 321 Cell Bandwidth Compressor

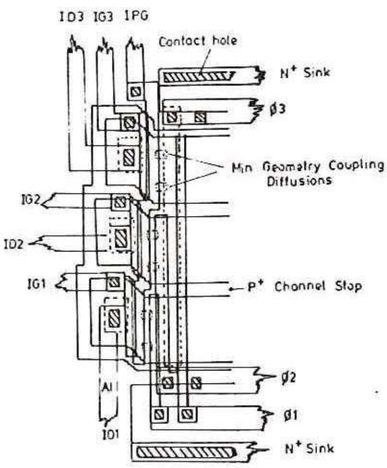


Fig 5 Input Layout

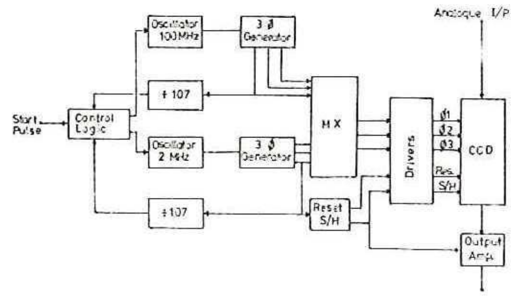
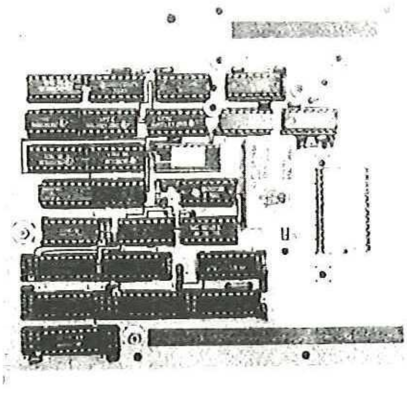
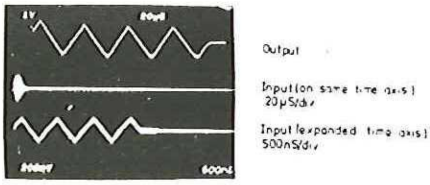


Fig 6 Driver Circuitry: Block Diagram and P. C. Board





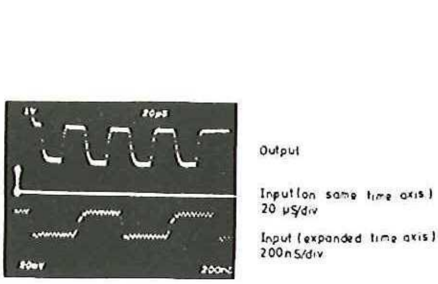


Fig 7 Output Waveforms