CCD ACOUSTIC SIGNAL PROCESSOR

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ABSTRACT

This paper presents a detailed analysis of the operation of a narrow bandwidth (1.0Hz) CCD transversal filter and describes an acoustic signal processing subsystem which incorporates the filter as a basic element.

The analytical design and preliminary measurements of the filter's spectral response have been reported earlier. A more detailed analysis of the dependence of the filter's operational parameters (i.e., bandwidth, stopband suppression, dynamic range, etc.) on the clock frequency f_c is given here. Measurements of device performance based upon current available data are presented.

The acoustic signal processor consists of a multi-channel delay and sum beamformer directly feeding a doubly weighted CCD narrow bandwidth bandpass transversal filter. Thus, the signal information is represented in the charge domain until the filter output signals are formed. Synchronization is required since the filter and beamformer may run at different, and possibly varied, clock frequencies. Clock drivers and control circuitry are implemented with NMOS logic, while a dual-differential charge integrator and sample and hold circuits fabricated with on-chip operational amplifiers form the detected output. Dynamic range of the system is expected to be greater than 50 dB, with a 1% linearity. Experimental data will be discussed if available.

I INTRODUCTION

The work described here is part of an effort to find areas where the use of Charge Coupled Devices (CCD's) results in improved performance of acoustic signal processing systems.

The majority of acoustic signal processors currently operating are implemented digitally. These systems typically mix the output of a digital beamformer with a digitized sinusoidal waveform. Any energy present at the mixing frequency will be transformed to a signal with zero center frequency. CCD's might be used in such systems to implement the (delay & sum) beamformer and/or to match filter the lower sideband signal of the mixed beamformed output, increasing the effective S/N ratio of the detected signal. Section II presents and discusses data demonstrating dark current limitations of a narrow band lowpass CCD transversal filter suitable for the matched filter application.

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As an alternative to the system described above, the beamformed output could be fed directly to a matched bandpass filter, avoiding the complications of mixing introduced to reduce the computational load of the digital processor. Because this is not a factor when using CCD filters within their operating range, by using CCD's it is possible to reconfigure the system architecture to achieve a more efficient signal processing subsystem. Section III describes an architecture for directly implementing a synchronized beamformer-multiple filter subsystem on a single monolithic chip.

II LOW PASS MATCHED FILTER

The CCD transversal filter chip shown in Fig. 1 is the vehicle for this study. The analytical design and some preliminary results for this device have been previously presented[1]. Briefly, the filter consists of a 101 stage four phase split-electrode delay line fabricated with a double layer polysilicon gate process. An auxilliary channel exists to cancel the differential mode clock noise contribution to the filter output. The design value for the passband edge of the filter is $f_p = .01\ f_c$ and $f_s = .03\ f_c$ for the stopband edge. Contamination of the signal charge by dark current can have a significant effect on the performance of the filter when the total delay time of the signal across the chip exceeds 1.0 second, i.e., $f_p = 1.0$ Hz and $f_c = 100$ Hz.

The frequency response of the filter has been measured at $f_c = 200$, 100, and 50 Hz. Three effects detrimental to the filters performance occur as the clock frequency is reduced as shown in Fig. 2. First, the main lobe of the frequency response characteristic is widened. Second, the magnitude of the first sidelobe is increased. Third the stopband noise level of the filter is considerably higher at the lower clock frequency. These results are summarized in Table I.

TABLE I

f_c(Hz)	1st Sidelobe (dB)	Stopband Rejection (dB)
50	17.5	25
100	22.5	33
200	23.33	34

The relative respsonse of the filter Vo(t)/Vi(t) at $f_c = 50.0$ Hz. is increased by the addition of the charge collected from thermally generated carriers (dark current) to the signal charge injected by the sinsoidal input voltage.

For the purpose of this analysis the dark current is a ramp with peak amplitude

$$A_{dc} = J_d N T_c \qquad (1)$$

where J_d is the dark current density, N the number of delay stages, and T_c the clock period. For large N the dark current density can be well approximated by

$$Q_{dc}(n)=A_{dc}nu(n). \tag{2}$$

Assuming the k^{th} signal charge packet $Qs(kT_c)$ injected into the CCD is proportional to the input voltage

$$Q_s(kT_c)=C_{ox}V_s(kT_c); \tag{3}$$

the spectral components of the continuous voltage waveform which if applied to the input of the CCD input would replicate the charge density distribution Q_{DC} are

$$V_{dc}(\omega)=\mathcal{F}(Q_{dc}(nT_c)/C_{ox}) = A_{dc}/C_{ox}\,(\delta'(j\omega)-\omega^{-2}). \tag{4}$$

$\delta'(j\omega)$ is a unit doublet at $\omega=0$. The relative contribution of $Q_{dc}(\omega)$ to the full well charge density capacity of the CCD delay line Q_{MAX} is shown in Fig. 3 for f_c = 100 Hz and 50 Hz. A CCD filter using this delay line and operating close to its full well capacity when maximum input voltages are sampled will not give an accurate response when $Q_{dc}(\omega)/Q_{MAX}$ exceeds the relative response of the filter for a given input frequency.

By assuming the effective filter input signal to be the superpostion of V_s and V_{DC}, the filter outpt is

$$V_o(kT_c) = \sum_{n=0}^{N} W_n \{ V_s(kT_c-nT_c) + V_{dc}(nT_c) \}, \tag{5}$$

Wn is the n^{th} weight of the filter. Note that the dark current contribution to V_o (kTc) is independent of k, and depends only on the device geometry. The spectral components of the filter output waveform are given by its z-transform

$$\sum_{k=0}^{\infty} V_o(kT_c)z^{-k} = \sum_{k=0}^{\infty}\sum_{n=0}^{N} W_n \{ V_s(kT_c-nT_c) + V_{dc}(nT_c) \} z^{-k} \tag{6}$$

If m=k-n,

$$V_o(\omega) = \sum_{n=0}^{N} W_n z^{-n} \left\{ \sum_{m=-n}^{\infty} \{V_s(mT_c)z^{-m} + \sum_{k=0}^{\infty} V_{dc}(nT_c)\, z^{-m} \right\}. \tag{7}$$

Therefore the frequency components present at the filter output are the relative frequency response of the filter multiplied by the input frequency spectrum plus the dark current contribution

$$V_{Odc}(\omega) = \sum_{k=0}^{\infty}\sum_{m=0}^{N} (W_n A_{dc} N/C_{ox})z^{-k} \tag{8}$$

V_{Odc} is proportional to the z transform of the weighted dark current charge density distribution. For an unweighted filter, Eqn (7) has the same dependence upon ω as Eqn. (4). For weighted filters, a numerical analysis is required to estimate the degradation of the filters spectral response caused by the thermally generated carriers. In the case of symetrically weighted filters $W_{N/2+i} = W_{N/2-i}$ for $0 \leq 1 \leq N/2$, and $\sum W_n n = N\bar{W}_{n/2}$. Using this result, with $J_d = 1$ na/cm^2, $C_{ox} = 4.2 \times 10^{-8}$F/cm^2, $NT_c = 2.0$ sec, the analytical result predicting the relative dark current contribution to the filter output is the dashed line plotted in Fig. 2. Thus the experimentally observed main lobe broadening of the filter's frequency spectrum at $f_c = 50$ Hz can be explained analytically by considering the contribution of thermally generated carrier to the input signal.

III ACOUSTIC SIGNAL PROCESSOR

The architecture of the acoustic signal processor is shown in Fig. 4. The signals sensed by an acoustic transducer array are converted to the charge domain and linearly combined in the seven element delay-and-sum beamformer. While still in the charge domain, the combined signal is input to a 128 stage multiply weighted bandpass filter. The relative frequency response of the filter formed by the first set of tap weights is presented in Fig. 5. The second set of tap weights produce a similar characteristics, but with slightly shifted center frequency. The charge on either side of the split-electrode structure is subtracted in the differential integrators, followed by a sample and hold circuit forming the dual outputs of the signal processor. Also required on-chip are individual clock generators for the beamformer and bandpass filter, and the analog charge sensing circuitry. The complexity and sophistication of this device, requiring adequate packing density, is best achieved by a double level NMOS polysilicon gate process capable of producing the CCD's, the analog operational amplifiers and digital control circuitry on a single monolithic chip.

A problem arises in transfering charge from the beamformer output to the transversal filter input since these two devices normally operate at different clock frequencies. Thus a synchronization technique is required to interface these two devices. The basic problem of synchronization is illustrated in Fig. 6. If the sample rate of the beamformer if f_b, and that of the filter is f_f, where $f_b \geq f_f$, one method for synchronization is to simply average the beamformer output sampled for a time $T_A=(f_b/f_f).T_b=T_f$. If we constrain f_b to be an integral multiple of f_f, this averaging could be accomplished as shown in Fig. 8, with an analog integrator gated on for the appropriate interval. To avoid the nonlinearities incurred in converting the signal from the charge to the voltage domain and back, however, a technique is desired which accomplishes the averaging in the charge domain. One such approach is demonstrated in Fig. 7. This diagram represents the signal charge as it progresses from the last stage of the beamformer to the 1st stage of the filter. It is assumed $f_b=2f_f$.

As shown, the charge at the beamformer output will be clocked under a transmission gate during ϕ_{1BF}, and summed with the previous beamformer output sample at ϕ_{2BF}. During $\phi_{4BF} = \phi_{1TF}$, the integrated charge packet is transferred to the filter input and a new sample appears at the beamformer output. The synchronization circuit proceeds in the same manner until the next two samples have been stored, averaged and delivered to the filter input . The use of two transfer gates with applied potential ϕ_{T1} and ϕ_{T2} simplifies the decoding logic required for synchronization since $\phi_{T1} = \phi_{1BF}$; $\phi_{T2} = \phi_{4TF}$, and

$$\phi_s = \overline{(\phi_{4BF} + \phi_{4TF})(\phi_{1BF} + \phi_{1TF})},$$

also this synchronization technique has the additional advantage of reducing the anti-aliasing filter requirement for the system[2].

IV DISCUSSION

Narrowband CCD transversal filters have been operated at clock frequencies as low as $f_c = 50.0$ Hz, where dark current effects become detrimental to the filters performance. Such filters maybe used to streamline the architecture of current digital acoustic signal processors, and permit the implementation of an acoustic signal processor subsystem combining beamforming and matched filtering functions on a single chip.

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2. C. H. Sequin, IEEE J. Solid State Circuits, Vol SC-12, pp. 609-615, Dec 1977.

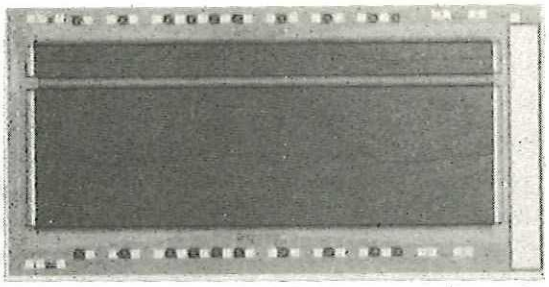

Figure 1. The NOSC-013 Transversal Filter Chip.

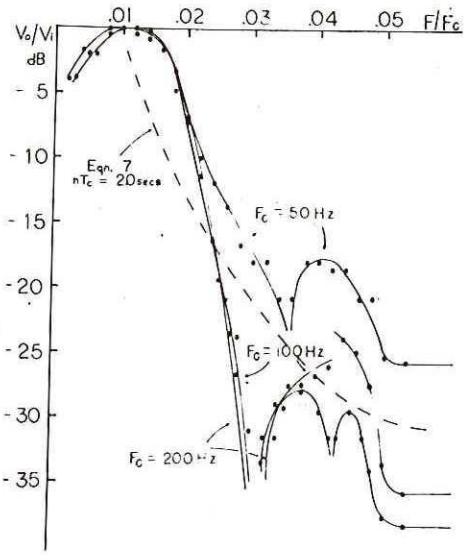

Figure 2. Dark Current Degradation of the Low Pass Filter Relative Frequency Response.

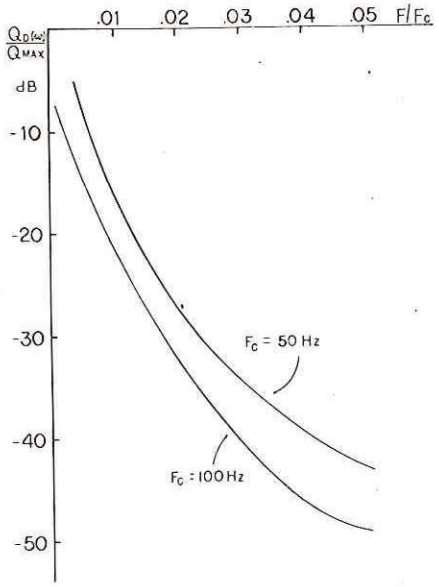

Figure 3. The Dark Current Signal Spectral Contribution.

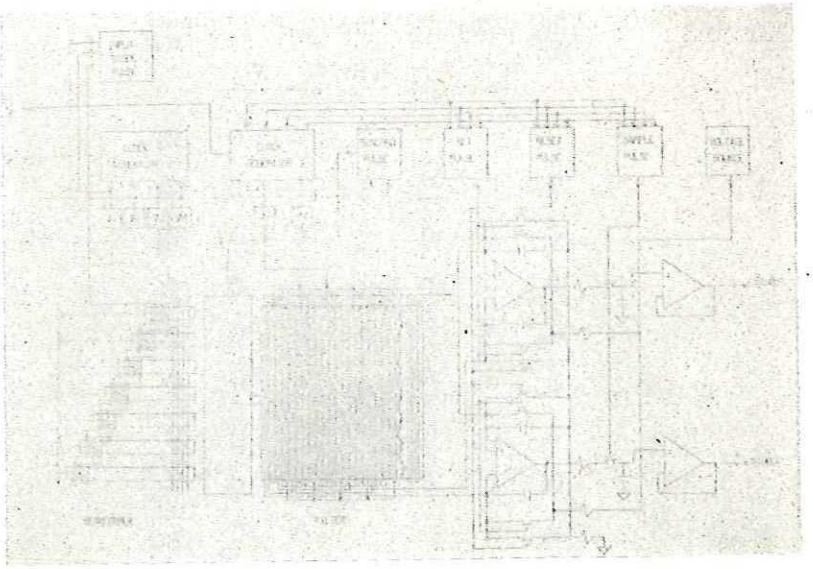

Figure 4. Acoustic Signal Processor Architecture

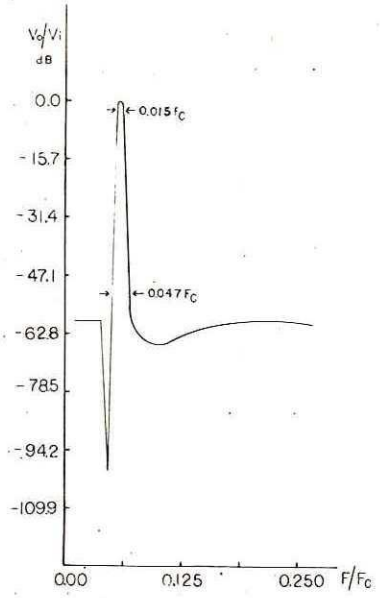

Figure 5. Band Pass Filter Relative Frequency Response

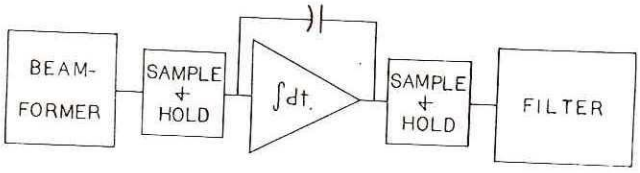

Figure 6. The Beamformer-Filter Synchronization Problem.

BEAM-FORMER PHASE PULSED HIGH	BEAM-FORMER ϕ_4	TRNSFER GATE ϕ_{T_1}	STORAGE GATE ϕ_S	TRNSFER GATE ϕ_{T_2}	FILTER ϕ_1	FILTER PHASE PULSED HIGH
ϕ_4	V_P	0	V_P	0	0	ϕ_2
ϕ_1	0	V_P	V_P	0	0	ϕ_3
ϕ_2	0	0	V_P	0	0	ϕ_3
ϕ_3	0	0	V_P	V_P	0	ϕ_4
ϕ_4	V_P	0	0	V_P	0	ϕ_4
ϕ_1	0	V_P	0	0	V_P	ϕ
ϕ_2	0	0	V_P	0	V_P	ϕ_1
ϕ_3	0	0	V_P	0	0	ϕ_2
ϕ_4	V_P	0	V_P	0	0	ϕ_2

Figure 7. A Three Gate Charge Domain Synchronization Technique.