CCD FILTER FOR THE PCM CODEC

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Abstract

Monolithic integrated filters for the PCM system can be realized with CCD transversal filter. With a cascade of CCD transversal filters with decreasing clock frequency it is possible to fullfill the frequency specifications including line frequency suppression. To minimize the space requirement and power dissipation a parallel-in/serial-out configuration was used for the realization of such a PCM filter.

1. Introduction

CCD devices, which are essentially nothing other than delay circuits, can be used for the simple realization of filter networks. If such a filter network is implemented without any provision for feedback from output to input, the result will be a type of transversal filter which is mainly outstanding for its excellent stability. The realization of transversal filters with CCD devices has been frequently described in the literature /1/.

One highly attractive area of application for this monolithic integrated filter is the PCM system, where it is used in combination with a PCM codec as a transmit and receive filter for bandlimiting the speech signal. In this application CCD transversal filters have in recent years encountered a strong rival in the switched-capacitor filter /2/. The characteristics of switched-capacitor filters make them appear particularly suitable for PCM systems, especially where there is a demand for a transmit filter which provides efficient line frequency suppression.

The present report describes however an implemented CCD transversal filter network which, as will be shown, is also capable of meeting this demand. Its network consists of a cascade of three CCD transversal filters designed with a parallel-in/serial-out configuration rather than the more widely used serial-in/parallel-out solution.

2. CCD Filter Network with Parallel-In/Serial-Out Configuration

The experimental filter network implemented for the PCM system consists of three individual filters with a parallel-in/serial-out configuration. To facilitate an understanding of the overall filter network it would therefore appear practical to describe its structure and properties before going on to discuss the cascading of the unit filters.

2.1 Structure of a Filter Network

There are two different approaches to realizing a transversal filter. One is to apply the signal to the input of a delay line, from which signals delayed by various delay times can be obtained (Figure 1a). These signals are weighted with various different coefficients and applied to an integrating element which then forms the output signal. The most widely known representative of this concept is the split-electrode transversal filter /1/.

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The other approach to realizing the transversal filter is first to weight the signal with a series of coefficients and then apply it parallel to the various elements of a delay line (Figure 1b). If a CCD, for instance, is used as a delay line, the signal can readily be added in the form of a charge packet to the already existing charge. Before describing the weighting principle of this concept with reference to the input stages and its advantageous antialiasing technique, we will first show the basic structure of such a filter network.

A CCD transversal filter network of this type can be realized as a number of CCD registers of different lenght. The weighting with coefficients of different magnitude resides in the various widths of the individual registers. If this filter network is simplified to the point where only a single CCD channel and a single output are left, the resulting structure will be as shown by Figure 2a. The stepped curve along the underside of the channel region is caused by the channel width being reduced there for each element by the vertical distance between two input stages.

Figure 2b shows a realized CCD transversal filter if this type with 25 coefficients. It is implemented in two-level polysilicon gate technology with a minimum structural width of 5 µm. Whereas the circuit length is given by the number of elements and the electrode width, the circuit width has to be realized to within a specified tolerance. We shall describe in the following sections how the circuit width can be substantially reduced through the skilful design of the input stage.

2.2 Signal Weighting in the Input Stages

A transversal filter has to meet the requirement that the signal should be weighted with variously large coefficients having different signs. It was already noted in the foregoing section that the respective magnitudes of the coefficients can be determined by the choice of width of the parallel inputs. We will now show how a positive or negative sign can be realized ad hoc for the input stages of a CCD device.

A potential equilibration input stage with excellent linearity and minimum noise /4/ is used for charge input. This input stage consists of a diode and up to three electrodes (Figure 3). The diode is now driven with a clock pulse $\emptyset_{id}$ such that charge flows from it under the electrodes at an appropriate instant and the superfluous charge is removed again when the clock pulse generator is deactivated. The signal voltage and a reference voltage are applied, say, to the first and third of the three electrodes; the second electrode, with a large voltage V_{DD}, always stores a sufficient amount of charge and serves primarily to assure that the signal voltage and the reference voltage are applied to electrodes of the same kind (Figure 4).

If a reference voltage U_{ref1} smaller than or equal to the minimum signal voltage is now applied to the first electrode and the signal U_{sig} is applied to the second electrode (Figure 3a), the signal charge Q_{sig} generated in the input stage can be defined

$$Q_{sig} = C_y \cdot (U_{sig} - U_{ref1}). \qquad (1)$$

Increasing the signal voltage U_{sig} will also increase the signal charge Q_{sig}, so this input stage is accordingly described as positive-weighting. To realize a negative-weighting input stage the signal voltage U_{sig} must be applied to the first electrode. The reference voltage U_{ref2} applied to the second electrode is larger than or equal to the maximum signal

voltage (Figure 3b). The charge packet Q_{sig} generated at this stage can be defined

$$Q_{sig} = C_v \cdot (U_{ref2} - U_{sig}) \qquad (2)$$

The generated charge packet Q_{sig} decreases as the signal voltage U_{sig} increases. Thus the realized CCD transversal filter is operated such that the zero level of the signal voltage is allocated a certain amount of charge in the CCD. Any change in the signal voltage will now bring about a change in the amount of charge generated at the positive and negative weighted inputs. It is thus possible for positive and negative inputs to be selected using a single signal voltage.

When a transversal filter with the described input stages is realized, two drawbacks are to be noted. One is that the desired interrelationship of the coefficients is liable to be altered by the process. The other is that even the smallest coefficient must be realized with the minimum structural width w_{min} (e.g. 5 µm). This results in the width of the filter being relatively large. We will next describe how these drawbacks can be avoided through skilful design of the input stage.

2.3 Differential Input Stages

In order to make a parameter of an integrated circuit independent of process-induced fluctuations, an attempt is made to define that parameter by the difference between two structures that are both subject to the same fluctuations. This is essentially the case, for instance, with the split-electrode filter, for the value of a coefficient is there formed by the difference between the two components of an electrode. In order to make a CCD transversal filter with parallel inputs similarly independent of process-induced fluctuations, it is again necessary to generate a difference at the input. This is accomplished by realizing each input stage with two parallel inputs, one of which is positive and the other negative weighting. One of these two inputs can be realized with minimum structural width (5 µm), while the width of the other will be the sum of the minimum width and the desired value of the coefficient (Figure 4). The difference between the channel widths in which the weighting resides will then be independent of process-induced fluctuations.

The second advantage offered by this input stage is that it reduces the minimum value for a coefficient. While the minimum coefficient was hitherto given by the minimum structural width w_{min} (5 µm) it is not given by the minimum difference between two structures. This difference will range between 0.1 µm and 1 µm, depending on the chosen technology. This means that it is now possible to realize a set of coefficients with small magnitudes within a small area.

Thus the structure of the realized input stages corresponds to that of the output stages of a double-split electrode filter /5/, for which the difference between the minimum structure and the sum of the minimum structure and the coefficient is likewise formed. In contrast to the split-electrode filters with a serial-in/parallel-out configuration, filter networks with a parallel-in/serial-out configuration offer however an additional advantage with regard to antialiasing which will be shown in the next section.

2.4 Special Antialiasing Technique for Parallel-in/Serial-out Structures

In sampled data systems, which also include the CCD transversal filter network, the sampled values of analog signals are processed. This sampling of the signal in the time domain involves in the frequency domain however the reflection of undesired signals into the baseband. To avoid these undesired effects an attempt is made to choose the sampling values of the CCD filter as high as possible (~200 kHz). A simple integrated lowpass filter with easily realizable conventional elements is in that case sufficient to suppress higher frequency components.

There are two ways of increasing the sampling rate of a CCD filter. One is to choose a higher clock frequency and increase the number of coefficients. Since however the power required by the filter will then increase on a square-law basis, this solution does not appear favorable. It has therefore been proposed that the CCD filter network be provided with an input filter /6/ which operates at a higher sampling rate and suppresses some of the undesired passbands of the filter network.

For CCD transversal filters with a parallel-in/serial-out configuration it is however alternatively possible, after a slight circuit modification, to choose a higher sampling rate with an associated set of coefficients without any significant increase in the power demand. Take, for example, the filter network shown by Figure 5a: the signal is sampled with f_{in}, but this frequency is only required at the input; at the output a lower frequency f_{out} can be used on account of the lowpass character of the filter. This filter network can be advantageously implemented with a parallel-in/serial-out configuration such that two input stages can be provided per CCD element while at the same time halving the number of elements as well as the sampling rate (Figure 5b). The resulting filter network requires only a quarter of the original power demand. If the charge packets are still generated at the input with the frequency f_{in} and every other charge packet at an element is allowed to enter the CCD, the resulting output signal will be identical with every second signal sample of the original circuit. This alternating selection of one of the two charge packets available per element is automatically controlled by the CCD clock pulses.

In the case of a transversal filter with parallel inputs it is naturally possible to go on increasing the sampling rate at the input up to the p-tuple value of the clock frequency, whereby p denotes the number of electrodes per element. For a four-phase system the most favorable solution was however found to be to provide two inputs per element because identical electrodes are then available for charge input.

2.5 Amplification Mechanism of Filter Network

The gain of a CCD filter network with a parallel-in/serial-out configuration is influenced by two different mechanisms. The first is defined by the chosen frequency response and the associated set of coefficients. If we take for instance a lowpass filter and apply to its input a signal with a frequency near to zero Hz, the charge packet appearing at the output will correspond to the sum of all the coefficients. Due to the different signs of the coefficients, this sum is however smaller than the sum of the absolute values of all the coefficients. The output capacitance must however be chosen such that a charge corresponding to the sum of the absolute values of all the coefficients can be stored. Since in the case of a difference input stage there will additionally be compensating component charges, the insertion loss A_{CO} due to the coefficients will be

$$A_{CO} = \sum_{\nu=1}^{n} \cdot C_\nu / \sum_{\nu=1}^{n} |C_\nu| + n \cdot w_{min} \qquad (3)$$

This insertion loss characteristic A_{co} is shown by Figure 6. The maximum charge Q_{max} is composed of the charges of positive, negative and compensating components of the input stages. The charge of the positive inputs here increases with the signal dc voltage, whereas the charge of the negative inputs decreases. The difference between the charges of positive and negative inputs then yields, in a given voltage range, the signal charge packet Q_{sig}. Q_{sig} referred to the maximum charge Q_{max} yields the insertion loss A_{co}.

Besides the insertion loss A_{co} due to the coefficients, CCD transversal filters have a second gain amplification mechanism which is determined by the CCDs. This gain A_{CCD} is given by the ratio of the total input capacitance C_{in} to the output capacitance C_{out}

$$A_{CCD} = \frac{C_{in}}{C_{out}} \tag{4}$$

Since any figure can be chosen for the total input capacitance, the gain of the CCD filter can be realized according to need.

Having treated the structure and characteristics of a unit filter we will now go on to the cascading of three unit filters to form a PCM transmit filter network, and finally we will discuss the results obtained with an experimental PCM transmit filter network of this type.

3. PCM Transmit Filter

3.1 Definition of the Problem

An experimental PCM transmit filter network was realized in order to demonstrate the feasibility of the CCD transversal filters required for a PCM system. Figure 7 shows the chosen tolerance scheme. Frequencies below 60 Hz (powerline frequency) are suppressed by more than 25 dB. Variations of $\pm$ 0.25 dB are allowed within the passband of 300 Hz to 3.4 kHz. The stopband attenuation beginning at 4.6 kHz should be greater than 30 dB. Since all frequencies above 4.6 kHz have to be suppressed, the use of a conventional RC filter network is essential, but the clock frequency of the CCD filter should be chosen as high as possible (above 200 kHz) so that this input filter can be realized in a simple form.

The requirements of the PCM receive filter, which was likewise realized as an experimental unit, are largely the same as those of the transmit filter except that no provision is needed for the suppression of low frequencies, which means that the overall structure is simpler. The additional sin x / x equalization required for the receive filter can be taken into account in a simple manner when calculating the filter coefficients. The following discussion of the filter characteristics will therefore be confined to the transmit filter, which is more difficult to realize.

Any attempt to meet all the requirements of the PCM transmit filter with a single transversal filter will run into the difficulty that for a high clock frequency of, say, 256 kHz, it will be necessary to realize a steep transition band between 60 Hz and 300 Hz. Transversal filters are basically unsuitable for meeting such a requirement because they allow the realization of zeros but no poles in the complex z-plane. To solve this problem it is necessary to have a transversal filter with an estimated figure of 800 coefficients. In this case, however, especially if the 800 coefficients are to be realized with sufficient accuracy, such a large area would be required and, due to the relatively high clock frequency, such a large amount of power would be dissipated, that this solution loses in intereset as compared to others. Thus a new approach was adopted for the realization of the CCD filter network.

3.2 Realization as a Cascade

The design of the PCM transmit filter is based on the concept that the various requirements which it can be met with a cascade of transversal filters operating at different frequencies (Figure 8). The high frequencies are suppressed with a simple lowpass filter (Figure 8b) which samples the input signal at 256 kHz. This lowpass filter has 25 coefficients and suppresses frequencies between 28 kHz und 228 kHz by more than 40 dB. The signal is next applied to a lowpass filter (Figure 8b)with the conventional 4 kHz response. For an input frequency of 32 kHz it has 55 coefficients. These first two lowpass filters were each realized with two input stages per element (ef. Section 2.4). In this way the area for each is reduced by half and the respective clock frequencies are reduced to 128 kHz and 16 kHz. The third filter, with which the steep transition band of 60 Hz to 300 Hz is realized, is run at the lowest possible frequency of 8 kHz. This filter is a bandpass filter (Figure 8b) with 61 coefficients and suppresses frequencies below 60 Hz by more than 25 dB. The three unit filters are realized such that their respective variations within the passband remain collectively below ± 0.25 dB. Since the 8 kHz output frequency of the cascade is identical to the PCM sampling frequency, the filter has to be synchronized with the PCM codec. The unit filters are connected directly from the output of a source follower to the input electrode of the next unit filter. The results obtained with our experimental PCM transmit filter will be described in the next section.

3.3 Measurements Performed on Experimental PCM Transmit Filter

3.3.1 Measurement of Frequency Response

The measured frequency response of the unit filters shows close agreement with the theoretical curves within the scope of the fabrication tolerances. With regard to the gain of the filters, the third unit filter realized as a bandpass filter was found to have an insertion loss of about 10 dB due to the chosen set of coefficients. This undesired insertion loss was offset by the CCD gain V_{CCD} of the filter in a redesign.

Figure 9 shows the frequency response curve of the overall PCM transmit filter network. The attenuation is seen to be more than 25 dB up to 60 Hz with variations of less than ± 0.25 dB within the passband, while the attenuation in the stopband starting at 4.6 kHz is greater than 32 dB. In the representation shown by Figure 9, sin x / x equalization is provided for the output signal.

3.3.2 Measurement of Delay Time

Besides the frequency response, the absolute delay time and delay distortion are of interest. The filter circuits used for the PCM transmit filter network were approximated with a constant group delay as per Chebyshev /7/. Since this constant group delay is too long for the requirements, the filter circuits were converted into minimum-phase systems without changing the number of coefficients /5/. The delay time then obtained for the PCM transmit filter is shown by Figure 10. The distortions between 1 kHz and 2.6 kHz are shorter than 125 µs and conform with the theoretical expectations, whereas the absolute delay time is 390 µs longer than calculated. This additional delay is caused by delays in the unit filters and by cascading; it can be avoided by appropiate circuit design. A fixed delay time of 100 µs and a distortion of 125 µs will remain.

3.3.3 Linearity and Random Noise of PCM Transmit Filter Network

First of all the linearity and random noise of the unit filters were measured so as to be able to determine the alteration due to the cascade. The random noise measured on the first unit filter was -78 dBm. For an input signal of 0 dBm the ratio between the signal and the 1st and 2nd harmonics was about 60 dB. The random noise of the second unit filter was likewise -78 dBm and the ratio between the signal and harmonics for an input signal of 0 dBm was greater than 50 dB. The random noise of the third unit filter was -82 dBm and an input signal of 0 dBm was here reduced to -10 dBm; the ratio of the signal to the 1st and 2nd harmonics was about 50 dB. The maximum linearity of the cascade was found to be 50 dB, but if a minimum variation of about o.5 V is assumed for the working points of the dc voltage of the unit filters it is possible to realize a linearity of 40 dB. With regard to the random noise of the cascade it should be noted that as the sampling frequency is reduced from one unit filter to the next noise components from higher passbands are reflected into the baseband, where they add to the existing noise. For the link between the first and second unit filters the noise increases for example by about 3 dB to -75 dBm. When the third unit filter is included the noise increases to -73 dBm. For the overall PCM transmit filter network this results in a signal-to-noise ratio of 63 dB for a input signal of 0 dBm. This result does not satisfy the PCM requirement of about -80 dBm. Since however the calculated thermal noise of the overall filter network is about -95 dBm, it would appear possible to realize the specified -80 dBm by optimizing the filter through appropriately designing the input and output stages e.g. increasing the gain of the third unit filter.

3.4 Space Requirement and Power Dissipation of the Experimental PCM Filter

In addition to the described PCM transmit filter network a PCM receive filter consisting of two cascaded CCD transversal filters was also implemented. The overall filter network consisting of five CCD transversal filters requires an area of 10 mm² (without clock circuitry).

The power dissipation P of the overall filter network can be calculated from the capacitance C and the respective clock frequencies f of the unit filters in the formula

$$P = f \cdot C \cdot U^2 \qquad (5)$$

For a voltage of U = 10 V the power dissipation calculates at about 20 mW, this being the reactive power used for recharging the capacitors of the CCD devices. The logic and driver stages required for obtaining the clock pulses for operating the CCD elements must likewise be integrated on the chip. Depending on the structure and the chosen technology, between two and five times the power dissipation of the CCD elements will be required. The dissipation of the overall PCM filter network, including the clock pulse generator, can therefore be estimated at about 100 mW. At this figure the dissipation of the PCM filter network consisting of cascaded CCD transversal filters is below that of one recently reported switched-capacitor filter /8/.

4. Conclusion

The present report is intended to show that CCD transversal filters are thoroughly capable of meeting the tight tolerances specified for PCM filters at reasonable cost. Since further improvements, especially reductions in dissipation, are to be expected for switched-capacitor filters,

it does not appear possible at this juncture to make any hard and fast prediction as to which of the two filter concepts will eventually be adopted for PCM filters.

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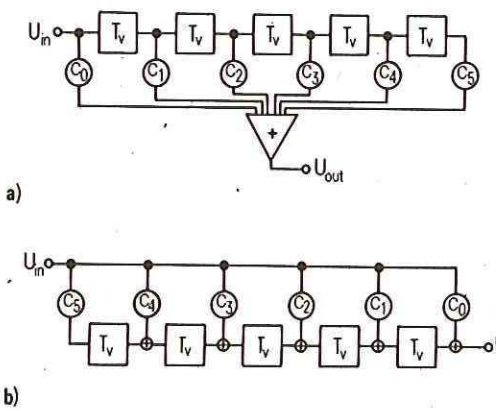

Figure 1 Principles of CCD transversal filters
a) Serial-in/parallel-out
b) Parallel-in/serial-out

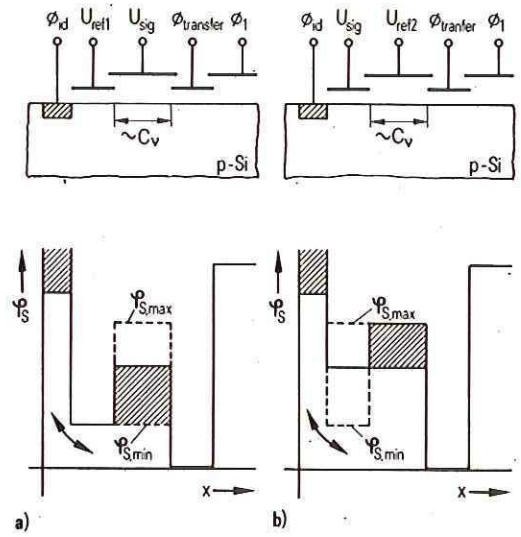

Figure 3 Principle of positive and negative coefficients
a) Positive coefficients: $Q_{sig} = C_v(U_{sig} - U_{ref1})$
b) Negative coefficients: $Q_{sig} = C_v(U_{ref2} - U_{sig})$

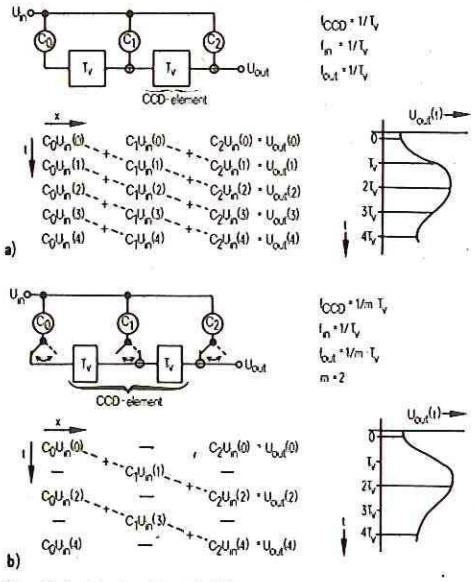

Figure 5 Construction of output data
a) identical input and output sampling rate $f_{in} = f_{out} = 1/T_v$
b) different input and output sampling rate $f_{in} = m \cdot f_{out} = 1/T_v$

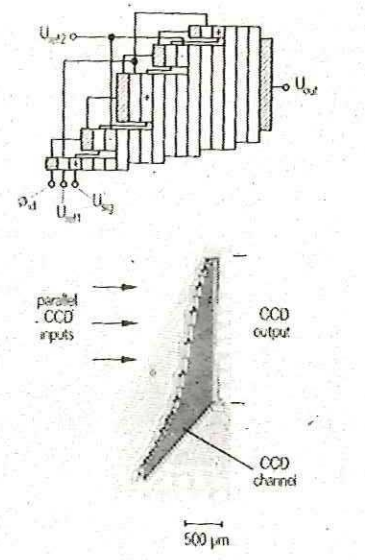

Figure 2 CCD transversal filter with parallel-in/serial-out configuration
a) principle
b) realized filter

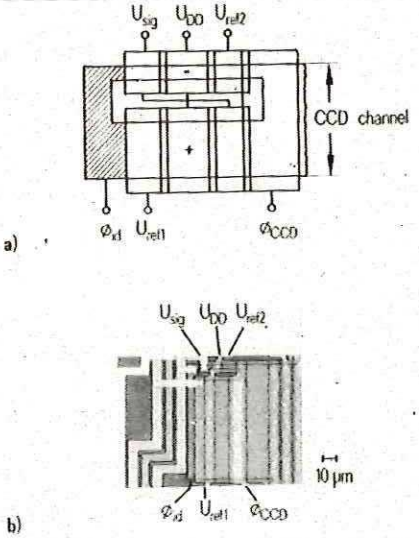

Figure 4 Differential input stage
a) Principle
b) Realized configuration

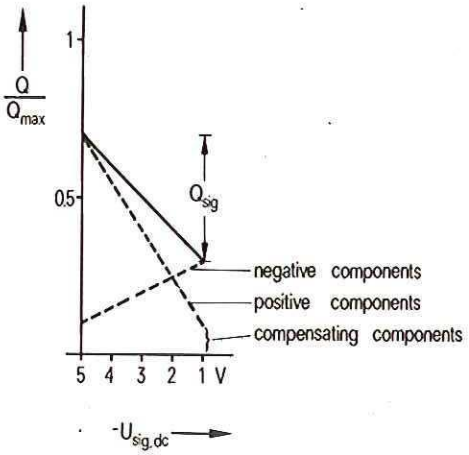

Figure 6 Amplification mechanism of a parallel-in/serial-out CCD transversal filter

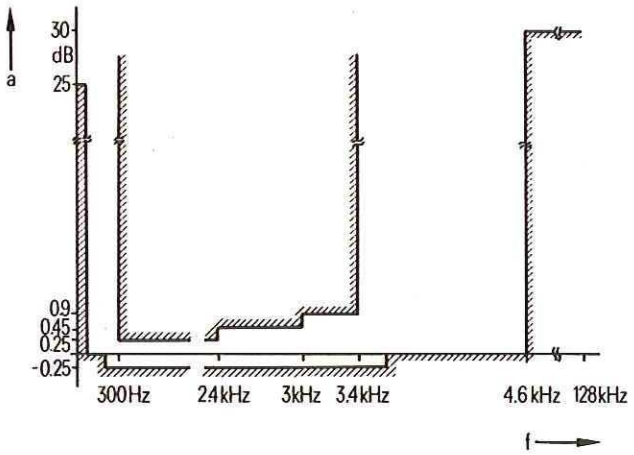

Figure 7 Tolerance scheme with line frequency suppression

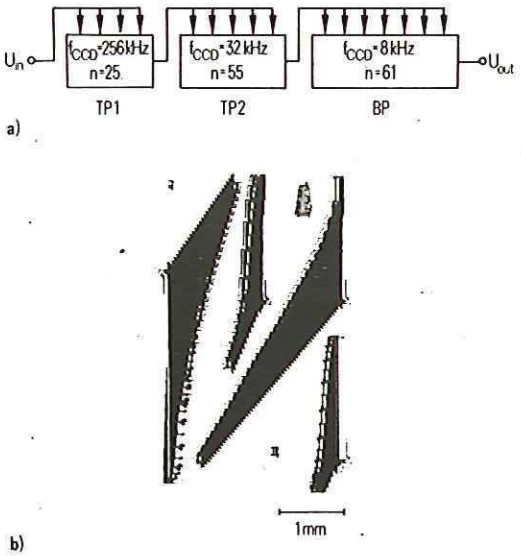

Figure 8 A PCM transmit filter with CCD transversal filters
a) Principle of a cascade of three CCD filters
b) Realized CCD transversal filters

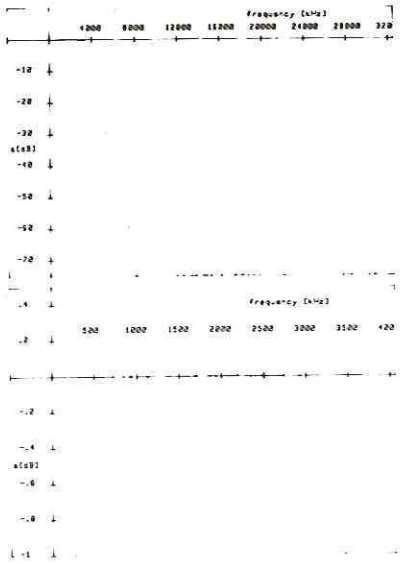

Figure 9 Frequency response of the realized PCM transmit filter

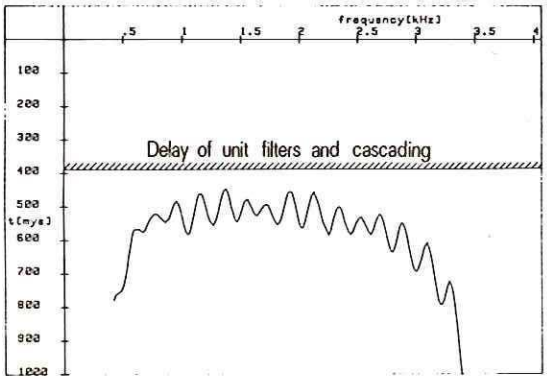

Figure 10 Delay distortion of the realized PCM transmit filter

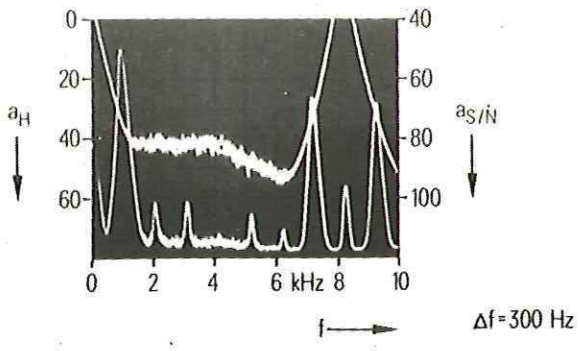

Figure 11 Harmonic attenuation a_H and signal-to-noise ratio $a_{S/N}$ (noise per 300 Hz) of the realized PCM transmit filter