DESIGN OF COMPLEX CCD/MOS INTEGRATED CIRCUITS

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ABSTRACT

Analog signal processing using CCD and MOS switched capacitor devices has matured to the point that large function blocks can be designed as a single integrated circuit. Design techniques and considerations are reviewed and LSI analog systems examples are examined.

INTRODUCTION

Soon after the invention of the charge coupled device, it became apparent that CCDs offered the possibility of a wide variety of signal processing functions including delay, multiplexing, analog memory, and filters.[1,2,3,4] More recently the development of analog switched capacitor filter circuits[5,6,7] has complemented CCDs and provided the MOS circuit designer a variety of building blocks for the design of signal processing functions. There has been a great deal of emphasis devoted to the problem of developing suitable analog and digital peripheral circuits to enable one to fabricate signal processing systems in highly integrated form.

There are several reasons for developing these highly integrated signal processing functions. The potential advantages of lower cost, smaller weight and volume, and reduced power are obvious. If we are to use CCDs and analog MOS there is another reason that it is desirable to achieve a high level of integration. These circuits tend to be best suited to high impedance levels which are incompatible with circuit boards. By integrating a whole function on a single chip it is possible to avoid driving large off chip capacitances and avoid pickup associated with stray capacitances. Better noise, power, and speed performance can be achieved when the sensitive analog signal nodes can be kept isolated from the external circuit boards.

There are a number of important considerations for the designer of these signal processing integrated circuits:

- o The IC designer must start by examining the system design in depth. In many cases the problem to be solved by an analog LSI IC needs to be reconfigured to achieve the optimal overall system. For example, in many cases a filtering function previously performed by passive LC networks might be most efficiently integrated using a CCD transversal filter. In another case, a function previously performed by an active filter might be best replaced by a filter using switched capacitor filters but in a different topology than the discrete designer might choose.
- o The concept of designing an analog system on a chip is relatively new. A general design philosophy and a set of well understood design rules equivalent to what might be used in purely digital designs are yet to be fully developed for analog/digital ICs.
- o Designs of this type are highly customized to particular applications. The combination of high complexity and unique applications for each design makes design costs relatively high.
- o Minimizing design cost through modularity and sacrificing chip area is important.
- o Analog circuits require extensive computer modeling.

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- o Because such IC designs are relatively low volume compared to standard MOS memory or logic products, the designer may be forced to adopt a standard MOS process which might be less than optimal for his design problem.
- o Testing a complex signal processing function in slice form with probes in a production environment presents a serious challenge. As with digital IC designs the circuit designer of analog LSI functions will have to make provision for rapid testing of the IC if production costs are to be practical.

In the following section we will examine several fundamental building blocks for analog signal processing ICs. Although in most cases these circuit elements require modification to optimize them for a particular design, it is desirable to reuse proven basic circuit ideas whenever possible. Examples of analog signal processing ICs are then discussed in the succeeding section.

II. CIRCUIT ELEMENTS FOR ANALOG LSI

CCD Filters

The CCD transversal filter[8] illustrated in Figure 1 offers perhaps the most powerful device in the analog MOS signal processing technology. Because the CCD can perform the fixed coefficient multiplies and adds in parallel and in the charge domain, very high computational power is available in the CCD transversal filter. With practical lengths up to 1000 coefficients and with clock rates above 1 MHz the CCD transversal filter can perform over 10^9 operations per second. CCD filters can be fabricated using two, three, or four phase CCD structures and a variety of different clocking and charge sensing schemes.

The circuit shown in Figure 2 illustrates one general approach to the charge sensing output circuit for a CCD filter. In the split electrode CCD filter, as signal charge packets are transferred along the CCD, an image charge appears on the clocking electrodes. One of these electrodes in each cell of the CCD is split into two separate portions and each piece is tied to a separate bus line as shown. The difference in the image charge sensed by the two portions of the split electrode is proportional to the signal charge in that particular well of the CCD and proportional to the difference in area between the two portions of the split electrode. The operational amplifier with the associated feedback capacitors serves to difference the total charge sensed by the two bus lines and provides the output voltage signal given by

$$V_{out}(n) = \frac{C_{in}}{C_f} \sum_{k=0}^{n-1} V_{in}\,(n-k)\,h_k \qquad (1)$$

where C_{in} is the capacitance of the input metering well of the CCD and C_f is the capacitance of the feedback capacitor, and h_k are the filter weighting coefficients. The split electrode phase of the CCD is maintained at a fixed DC potential by the two "switched capacitor" resistors represented by the minimum size capacitor C_3 and the two MOSFET switches gated on by two non-overlapping clock signals R_1 and R_2. The use of the switched capacitor resistors avoids the reset noise which would be introduced if the resistors were replaced by simple switches. In addition, the operational amplifier used does not have to be compensated for unity gain internally because it is not reset. Much higher bandwidth is possible in this mode of operation. A second amplifier can be added to this circuit which senses and feeds back the common mode signal via capacitive

coupling. Variations of this basic scheme have been used in several IC designs.

Operational Amplifiers

A key circuit for analog signal processing is the operational amplifier. Its performance requirements always challenge the limit of our technological ability in one or more characteristics, i.e., speed, power, size, dynamic range, etc. To date we have not fabricated the universal operational amplifier which satisfies all our applications, but the design shown in Figure 3 has proven quite useful in several IC designs. It emphasizes low power, its budget being 4 mW using a 15V supply. The other specifications are more modest: gain of 2000, gain bandwidth of 2 MHz, and a slew rate of 2 V/μsec. The same general approach has been utilized for higher bandwidth designs.

We employed a traditional two-stage amplifier topology. The first stage consists of transistors M10 through M14. Depletion loads (M10 and M11) provide more gain than would enhancement loads. The quiescent operation conditions of this stage were set to provide the desired high output impedance and to maximize the common mode range. This stage has a differential gain of 30 and consumes .14 mW. The second stage (M19 through M22) is a single-ended inverting amplifier. The driver (M22) sinks the quiescent currents of both the cascode transistor (M20) and the current source (M21). The purpose of the current source is to provide a large fraction of the current through the driver. Thus the load (M19) conducts a much smaller quiescent current than the driver. Since device transconductance is proportional to current, this circuit provides more voltage gain than a circuit with equal load and driver quiescent currents. The output stage (M23 and M24) is a simple source follower scheme.

Because we used NMOS technology, level translation circuits (M15 through M18) are required. Transistors M16 and M17 act as diodes, dropping voltage to the desired quiescent level for M22. The similar circuit, consisting of transistors M6 through M9, provides a differential to a single-ended conversion. The differential signal seen at M10 is level-shifted and fed back to the current source (M14) which acts as an inverting amplifier with loads M10 and M11. The result is that M10 voltage is stabilized, and the signal at M11 is doubled. Capacitors C_1 and C_2 are used to balance the low and high frequency gains of the level shifters, i.e., no signal phase shift occurs in the level shifters.

This amplifier is unity gain compensated by creating a low frequency dominant pole. This pole is formed by the output impedance of the first stage and the integrating capacitor of the second stage, C_3, multiplied by the Miller effect of the second stage. All other poles in the circuit are designed to have frequencies large compared to the unity gain frequency of the overall amplifier. This insures stable operation in the unity gain mode.

Switched Capacitor Filters

Transversal filters, which have only zeros of transmission in their transfer function, are relatively inefficient in their use of silicon area for certain types of frequency responses such as narrow bandpass filters. For these cases a recursive filter (i.e., one which has feedback) that implements poles would be more appropriate. However, CCD recursive filters have several disadvantages. First, in order to implement a stable, accurate recursive filter using CCDs, it is necessary to perform charge-to-voltage and voltage-to-charge conversions with high precision and accuracy. Second, the recursive filter most compatible with CCD implemen-

tation is the so-called direct form filter, but the direct form architecture is known to have very high sensitivity to coefficient accuracy. Thus, it is difficult to achieve sufficient accuracy in recursive CCD filters especially for filters with high Q poles. Another approach to the realization of recursive filters is the use of switched capacitor filters.[5,6,7]

Switched capacitor filters rely on the use of switches, precision ratioed capacitors and operational amplifiers used as integrators. The basic building block of such filters is the sampled data integrator shown in Figure 4. One advantage of using switched capacitor recursive filters is that they are compatible with architectures such as the ladder filter which have very low coefficient sensitivities.

In order to understand the switched capacitor filter operation we examine first a conventional integrator, then a sampled data integrator and its z-transform, and finally a second order section will be described. In Figure 4a, a conventional analog integrator is shown, and in Figure 4b the MOS circuit time integrator is shown. The resistor R_1 has been replaced with a double throw switch and capacitor C_1. This circuit operates in a sampled data mode with the switch alternating at a clock period T_c between the left-hand position shown in Figure 4b to the right-hand position. The z-transform for this circuit can be written in the form

$$H(z) = -\frac{(C_1/C_2)\, z^{-1}}{1-z^{-1}} \qquad (2)$$

which can be recognized as the equivalent of a digital integrator.

This integrator forms the basis for a second order filter as shown in Figure 5. Two integrators can be seen in the figure. One is formed with the capacitors $\alpha_L C_L$ and C_L and the other by $\alpha_c C_c$ and C_c. A sign inversion is accomplished by adding a second switch to the bottom plate of the capacitor so that the polarity can be reversed when discharging this capacitor into its corresponding integrator. The z-transform of this circuit can be written as

$$\frac{V_{out}(z)}{V_{in}(z)} = \frac{-\alpha_i \alpha_c\, (z-1)}{z^2 - (2-\alpha_c\alpha_T - \alpha_c\alpha_L)z + (1-\alpha_c\alpha_T)} \qquad (3)$$

We can see from the z-transform that the frequency response is independent of the absolute values of either C_L or C_c, but depends only on the capacitor ratios α_c, α_L, and α_T. MOS fabrication techniques allow the control of such capacitor ratios to a precision on the order of 0.1% which is adequate for many filtering problems.

Multiplying D/A Converters

Many signal processing functions require the uses of a programmable multiplier. A multiplying digital to analog converter (MDAC) is a convenient tool for these applications. Based on the charge redistribution technique, the MDAC provides an analog output signal which is the product of a sampled analog input multiplied by a set of digital coefficients which can be programmable. The schematic shown in Figure 6 is one implementation of this device which we have used on several ICs. The differential analog signal labeled V_{in} is first sampled onto two holding capacitors. The sampled signals are buffered by two amplifiers capable of driving the capacitor arrays. Pairs of switches controlled by latches

one set for each bit of the digital word, are used to control the input to the bottom plate of each of the capacitors in an array of binary weighted capacitors.[9] In the first step of the cycle each of the capacitor plates is switched to the V_{in}^{-} signal except for the MSB which is switched to the V_{in}^{+} signal. Meanwhile, the top plate of the capacitor array which is a common node for all the capacitors is switched to a reference voltage. In the second half of the cycle, the switches are thrown to the opposite positions for those bits in the digital work corresponding to zero's. The resulting change in the output signal voltage between the first half and the second half of the clock cycle is proportional to the product of the analog voltage V_{in} and the two's compliment coded digital words. The arrays of this type can be built with 10-bit accuracy and can be made to operate at at least 1-2 MHz sample rates.

CCD Clock Drivers and Digital Logic

The control functions in the clocking requirements of CCDs and switched capacitor circuits involve considerable amount of digital logic. The logic functions can, of course, be obtained by standard NMOS techniques and will not be further discussed here. However, one particular clock driver circuit which we found to be very useful is shown in Figure 7. An input signal applied at node A is used to turn the clock driver on and a non-overlapping pulse applied to node B is used to turn off the driver. Transistor M5 is used to charge the bootstrap capacitor formed by transistor M8 whose source and drain are tied together to form a capacitor. Transistor M7 pulls up the bottom plate of the bootstrap capacitor which provides a large gate overdrive on transistor M10 allowing the clock driver to pull the output node to V_{DD}. Delay of the input pulse applied to node A is provided by transistors M1, M3 before it reaches the gate of M7 and M11. This delay causes M7 and M11 to remain on during the initial part of the rise of the driver output, thus achieving a larger charge on the bootstrap capacitor and ultimately a faster transition. The clock driver turn off pulse applied to node B discharges the bootstrap capacitor through M6 and after a small delay pulls up the gates of M7 and M11 causing the output to be pulled low.

A typical LSI analog IC may involve from 10 to 20 such clock circuits which all drive different load capacitances. We have found it convenient to design two or three different sizes of the drivers, each optimized to a different range of load capacitance. Most of the clocks have small capacitive loads and identical small driver circuits are used to drive these loads even though they are not exactly optimized. The same circuit with larger transistors is used to drive large capacitances in the order of 100-200 pF as typically might be found in CCD clock electrodes. The pulses for inputting at node A or at node B can be derived from standard MOS logic circuitry without the need for drivers because the input transistors to the clock driver are typically very small gates.

III. LSI ANALOG SIGNAL PROCESSOR DESIGN EXAMPLES

One example of an IC combining the elements which were discussed above is that of a monolithic analog 512-point chirp z-transform (CZT) processor.[10] The chip calculates the discrete Fourier transform (DFT) using the chirp z-transform algorithm as illustrated in Figure 8. The 6.1 x 5.5 millimeter CCD/NMOS chip includes the premultiply, convolution, and post multiply operations required to perform the CZT. A dynamic range of 63 dB has been obtained at sampling frequencies ranging from

1 KHz to 1.5 MHz. Significant improvement in performance of the CZT over previous implementations[11,12] was made possible by the high level of integration on this IC. Key elements were the CCD charge sensing scheme discussed above along with a common mode stabilizing circuit and a three level CCD clocking scheme for better offset control.

A block diagram of the processor chip is shown in Figure 9. In operation, the input signal is premultiplied by a chirp in the multiplying D/A converters (MDAC) before being convolved with another chirp in 4 512-stage transversal filters. Two CCD sense amps can be used for the four devices to produce the real and imaginary outputs of the convolution. These two output siganls can be post multiplied using the same MDACs that are used for the premultiplier since the transform operates on a 50% duty cycle and the output and input signals are out of phase in this cycle.

The system is partitioned as illustrated in Figure 9. A 9-bit address counter for the 512 chirp coefficients and the chirp ROM are left off the main processor chip. These functions can be performed with conventional digital technology and are too costly in area to include with the chirp z-transform. What is integrated on the IC are the CCD filters, multiplying S/A converters, control logic, clocks, CCD sense amplifiers and buffer amplifiers to buffer the analog signals.

The layout of the IC can be seen in the photomicrograph of the integrated circuit in Figure 10. Here the multiplying D/A converters and the digital signals are on the left-hand side of the bar layout. The bus structure in the center of the bar is used to distribute clock pulses to the main clock drivers for the CCDs just to the right of the center and to the clock circuits required by the MDACs on the left-hand side of the core buff structure. The CCDs can be seen on the right-hand side of the bar. Each of the four CCDs is comprised of four folded channels. At the bottom of the bar are the two input amplifier buffers and at the top of the bar are the two CCD sense amplifiers and the common mode feedback amplifiers which are used to stabilize the common mode operating point of the CCD sense electrodes.

The modular layout shown in Figure 10 provides effective isolation of the digital and analog portions of the circuit. Another precaution taken to avoid analog/digital interactions via substrate coupling was to use differential analog signal paths in most parts of the analog signal path.

Each device was built with a two phase charge coupled device structure using an implanted well technology which was developed for the TI 64 kbit CCD memory. In this process, the second half of each polysilicon gate level has a self aligned implant which provides the charge storage well for the CCD. In order to provide better dc offset control a new clocking scheme was devised which is illustrated in a simplified timing diagram in Figure 11. The clocking scheme maintains the split electrodes of the CCD filter at a fixed potential halfway between ground and positive power supply. The other CCD phase is clocked at three levels in the sequence, zero volts, 7.5 volts, 15 volts and 7.5 volts. The clocked electrode thus is at 7.5 volts twice during the cycle, once when the charge packet is stored under the sense electrodes and again when the signal charge is stored under the clocked electrodes. Conditions seen by the sense amplifier are the same at both times in the cycle except for the presence of the signal charge under the split electrodes during the first period. The output of the differential sense amplifier is sampled at both times and the two output samples are differenced. Thus, we have a means of measuring the signal minus all the feedthrough offsets. The scheme has worked very well at minimizing the which pose a serious problem for the chirp z-transform.

Two more examples of analog LSI circuits are provided by two integra-

ted circuits developed for a CCD/NMOS channel vocoder. The vocoder system is shown in the block diagram in Figure 12. One CCD/NMOS IC shown in the upper dashed line is used to analyze spectral content of voice signals and produces a compact digital code. A second IC shown in the lower dashed line is used to synthesize voice signal from this digital code.

The purpose of the vocoder is to reduce the data rate of speech transmission to 2.4 kbits per second while maintaining high quality and intelligibility in the reconstructed speech signal at the receiver. The basic operation of the channel vocoder is to determine periodically (every 20 msec) the spectral envelope of the speech using the filter bank. The nature of the excitation of this speaker's voice (either a periodic pulse trained for voice sounds or a random noise source for unvoiced sounds) is determined by a pitch tracker. These parameters are encoded into a compact digital code at 2.4 kbits per second and transmitted to the receiver which then synthesizes a signal having approximately the same spectral envelope. The synthesizer uses a filter bank excited by either a periodic pulse strain or a random noise source where the gain parameters of the filter bank, the selection of the excitation, and pulse period are controlled by the information from the transmitted signal.

The voice analysis IC consists of a bank of 19 channels. Each of the channels has a bandpass filter followed by a half wave rectifier and a lowpass filter. The 19 bandpass filters span the audio frequency spectrum from 180 Hz to 4.1 KHz in such a way that the composite filter is approximately flat throughout this range. Each channel output is thus a measure of the energy in its corresponding spectral range. The 19 channels are sampled every 20 msecs and sequentially multiplexed into an A/D converter having a logarithmic response. A five bit digital code representing 1.5 dB steps is generated for each of the 19 segments of the spectrum.

The bandpass filters of the channel bank are implemented with 100 tap CCD transversal filters. The use of switched capacitor bandpass filters was also investigated. However, because the desired filter characteristics would have required two complex pole pairs, the switched capacitor filters would have been larger in silicon area and would have required four times the power used in the CCD filters. The rectifier circuit was implemented using the nonlinear characteristics of a MOSFET, and a feedback amplifier to achieve a sharp rectifier characteristic. The lowpass filters following the rectifier are 3-pole Butterworth switched capacitor filters with a 35 Hz bandwidth. These lowpass filters are implemented using simple source followers rather than operational amplifiers. After the lowpass filters MOS storage capacitors and switches are used to multiplex the signals before they are fed to an A/D converter. The A/D circuit uses a binary weighted capacitor array similar to the MDAC discussed previously to implement the logarithmic A/D conversion.

The clock system on this chip was relatively complex requiring 40 KHz, 10 KHz, 1 KHz, and 50 Hz. A total of 32 different clock waveforms were used in the design. The need for most of these clocks resulted from the decision to use double correlated sampling techniques to eliminate offsets associated with the MOS circuitry. Although the clock system is complex, the MOS circuits to realize the various clock phases are relatively straightforward and require a relatively small amount of silicon area.

In Figure 13 the bar photo of the vocoder analyzer is shown. The modular layout is obvious in the photograph. Each of the 19 channels is identical except for the tap weights of the filters and feedback capacitors associated with the charge sensing circuit of the filters. The feedback capacitors are individually adjusted to normalize the gains of

the filter bank. A common module was used for all the 19 channels with only those adjustable parts being coded separately. The clocking system was laid out as a single module consisting of a number of clock drivers which were designed to stack together conveniently. Most of the clock buses were laid out as a regular array and then the clock generation module was simply connected to it. This approach is far from optimum in the use of silicon area, but it was much faster in the design cycle than other approaches might have been.

The synthesizer for the vocoder is shown in the block diagram in Figure 14. The input to this chip is a sequence of 20 8-bit digital words at the rate of 1 per msec. One of these words controls the selection of the voiced or unvoiced excitation on the chip which is either a random sequence or a pulse generator whose period is controlled by the data in the excitation word. The remaining 19 words of input data are directed to a D/A converter which is demultiplexed to 19 sample and hold circuits, one for each of the synthesis channels. Each of the synthesis channels contains a three pole lowpass filter, a modulator and a bandpass filter. The lowpass filters provide interpolation between the 20 msec speech frames and each lowpass output is used to modulate the amplitude of the excitation pulses which are applied to the corresponding bandpass filter. The outputs of the 19 bandpass channels are summed together to produce the speech output signals.

The lowpass filters are implemented as they were in the analyzer described above. The bandpass filters needed for the synthesizer are simple complex pole pairs which were implemented with less power and silicon area using the switched capacitor filters. The second order filters are like those shown in Figure 8. The modulators are simple switches and capacitors which gate the lowpass output to the bandpass filters during either a noise or pitch pulse.

A photograph of the synthesizer IC shown in Figure 15 and again the modular layout can be seen. Each of the synthesizer channels is layed out in a basic cell identical to all of the other 18 channels. The capacitor arrays for the filters in each channel were customized for that particular frequency response using an overlay cell containing only the capacitors. We sacrifice silicon area for the relative design ease of having the modular layout. The clocking system on this IC as seen in the lower left-hand corner is similar to that used in the analyzer. The D/A converter is seen in the lower middle section of the IC, and the excitation section, the pitch counter, and the noise generator are seen in the lower right-hand corner.

The process used to fabricate these two ICs is similar to the one used described for the 512 point chirp z-transform. However, in this case in order to simplify the design, fabrication, and packing density of peripheral circuits the implanted wells of the two-phase process were eliminated. The resulting process uses four-phase CCD structures which are less dense than the two-phase structure, but this loss is recovered by denser design rules in the peripheral circuit areas.

Testing presents an interesting challenge for these ICs because of the complex nature the signals applied to the devices and their outputs. During the development phase we have included a large number of test points for probes in order to analyze specific parts of the circuit. Although it is yet to be demonstrated, a functioning analyzer can probably be used as the measurement tool to verify synthesizer ICs at probe while specific test inputs are applied to the device under test. The analyzer can be tested by using it as a spectrum analyzer with simple chirp input waveforms applied during probe tests.

CONCLUSIONS

As illustrated by the above examples it is possible to integrate complex analog signal processing functions. The chip designer now has a variety of "tools" available for this task. Although the ICs mentioned above are in the early phase of development several observations can be made.

- o Combining analog and digital MOS and CCD circuits can be done successfully without uncontrollable interaction between analog and digital functions.
- o Modular design ideas can be applied successfully to reduce designer time and costs.
- o We have found that requirements for analog modelling and layout exceed those of digital logic functions.
- o Standard MOS processing techniques can be used to fabricate these analog LSI circuits.
- o The design of automatic testing procedures for such ICs is a formidable problem which may delay generalized solutions. A great deal of attention must be devoted to this problem to realize a cost effective IC design.

For those applications which have sufficient volume to justify the costs associated with custom designs, the LSI analog technology provides a very attractive approach which can lower costs, power, size, and weight. The commercial impact of analog LSI is just beginning to be felt, as this technology is starting to move from the laboratory to production environments.

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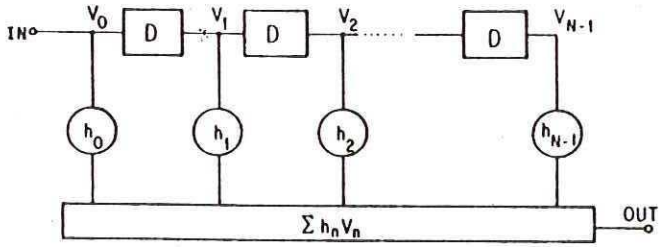


Fig. 1. Block diagram of a transversal filter showing delay stages D and weighting coefficients h_n, n = o, N - 1.

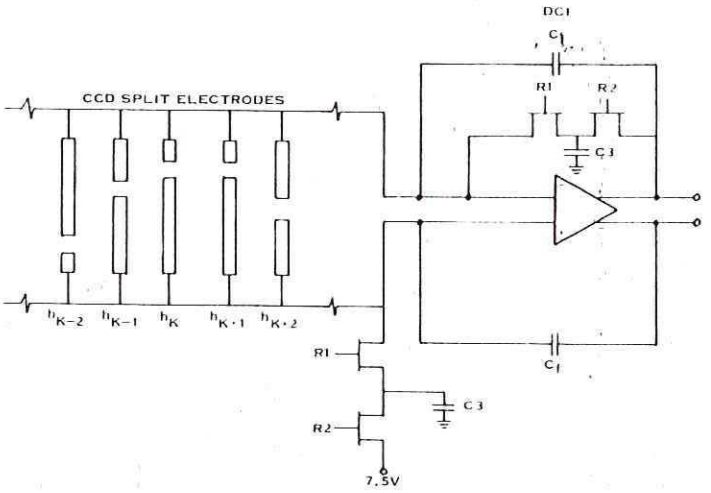


Fig. 2. CCD transversal filter output sensing circuit.

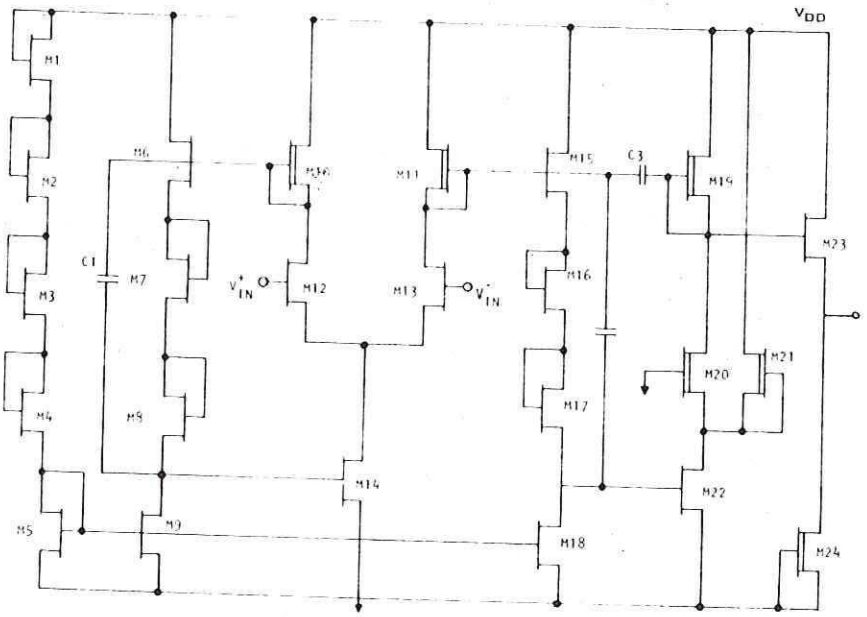


Fig.3. MOS operational amplifier circuit.

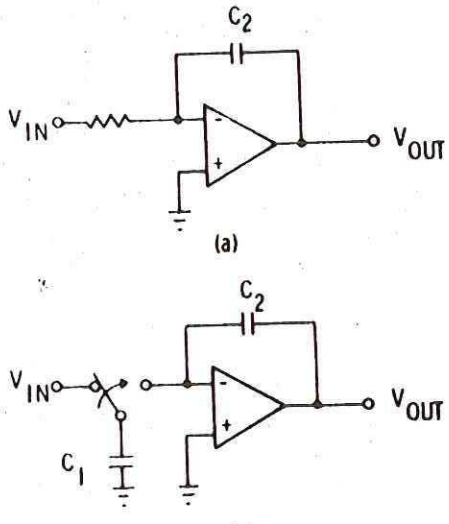


Fig. 4. a) Conventional RC integrator, b) Sampled data integrator, c) Z-transform of integrator in (b).

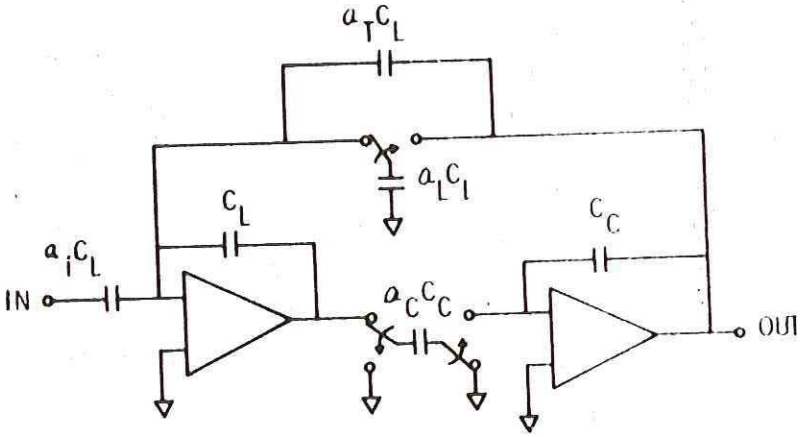


Fig. 5. Two pole bandpass filter using switched capacitor integrators.

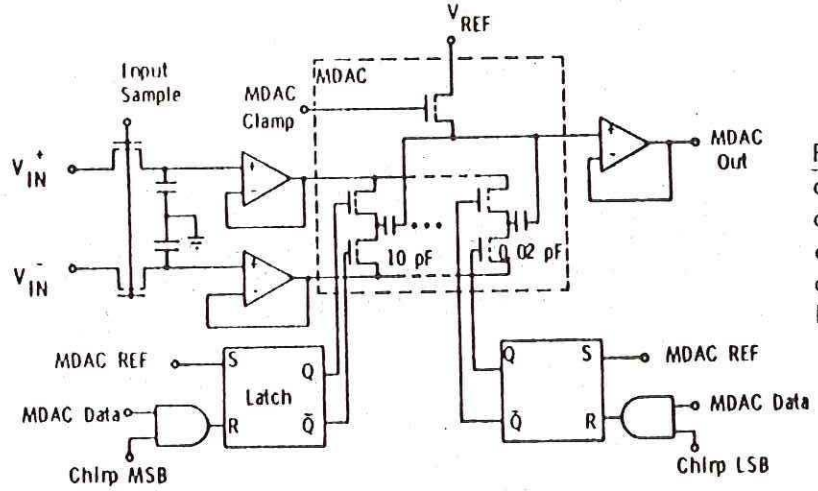


Fig. 6. Multiplying D/A converter using an array of capacitors. The MSB capacitor is 10 pF and the other capacitors are given by $C_i = 10x2^{-i}$ for $0 \le i \le 9$.

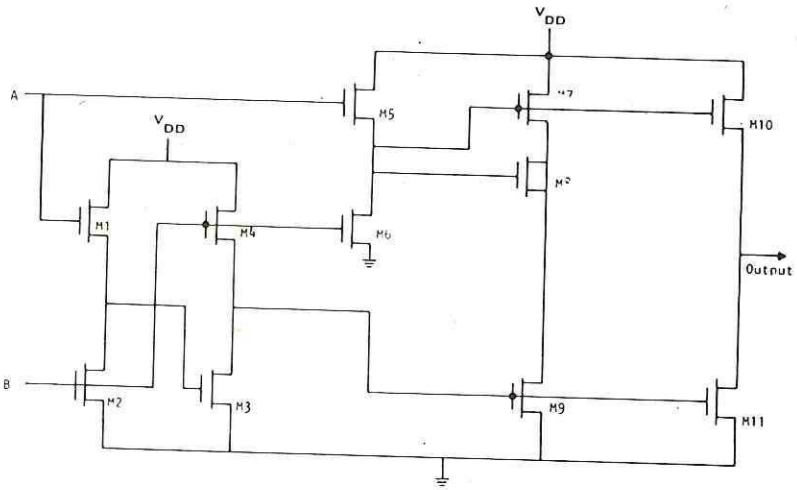
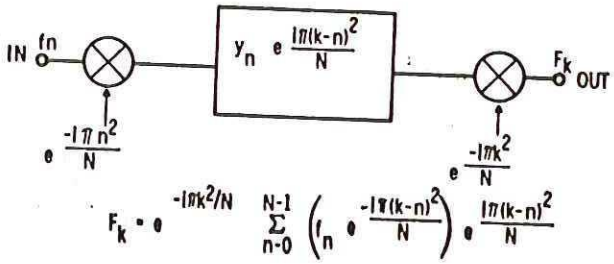


Fig. 7. Clock driver circuit.

Fig. 8. Block diagrams of the chirp z-transform (CZT) algorithm for computing a discrete Fourier transform (DFT).



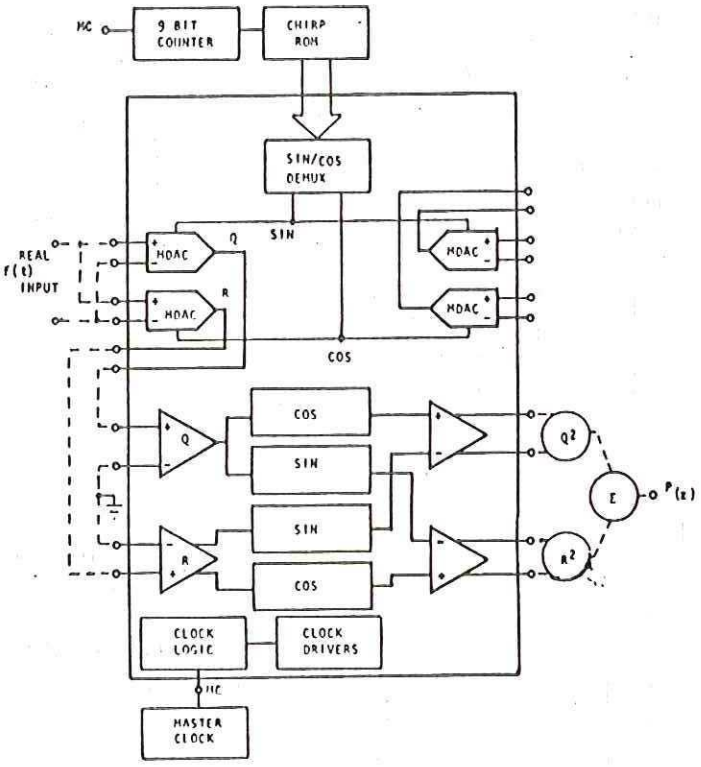


Fig. 9. Block diagram of a 512 point CZT integrated circuit.

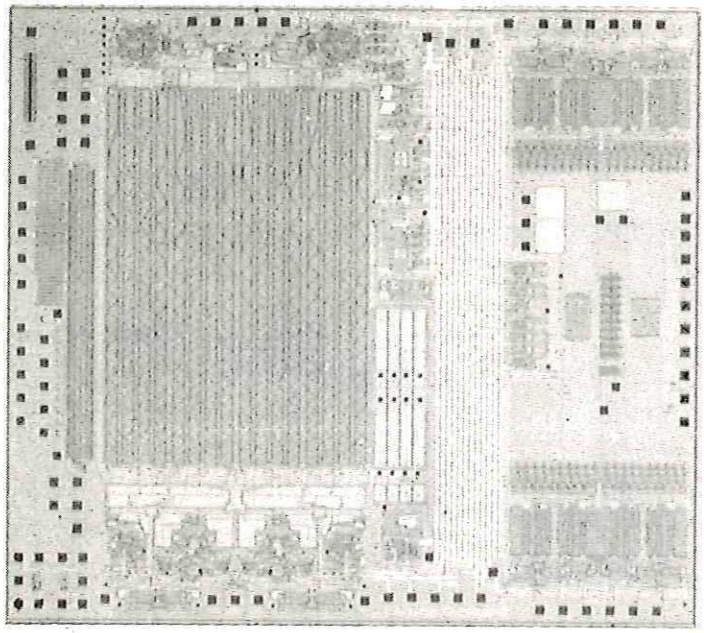


Fig. 10. Photomicrograph of a 512 point CZT integrated circuit.

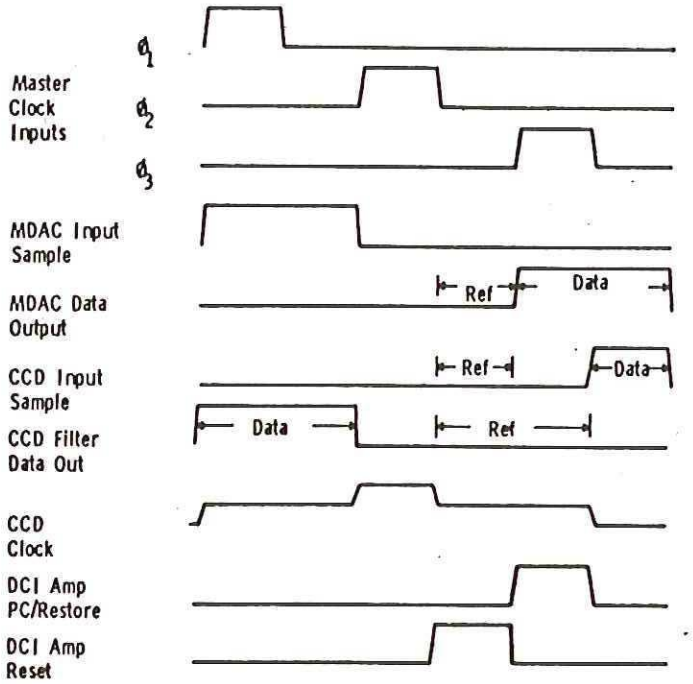


Fig. 11. Simplified timing diagram of a CZT IC.

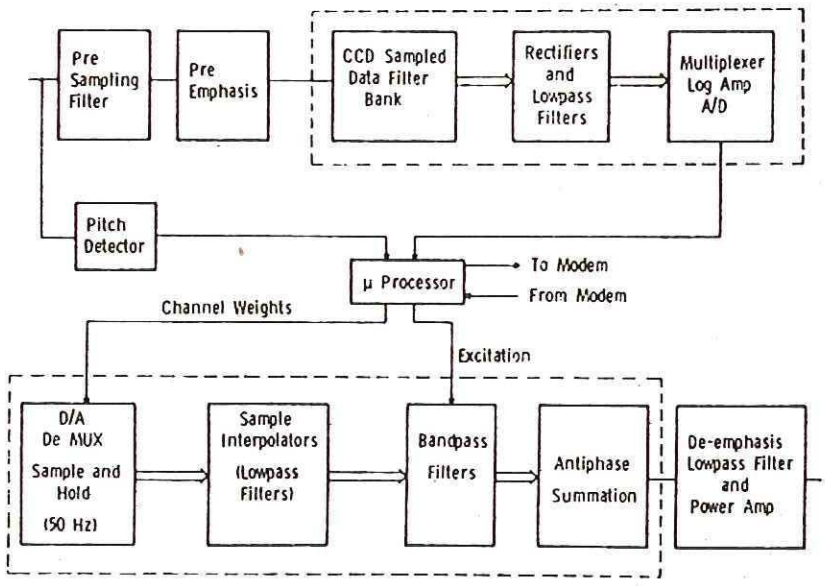


Fig. 12. Block diagram of a channel vocoder based on two custom IC functions enclosed in dashed lines.

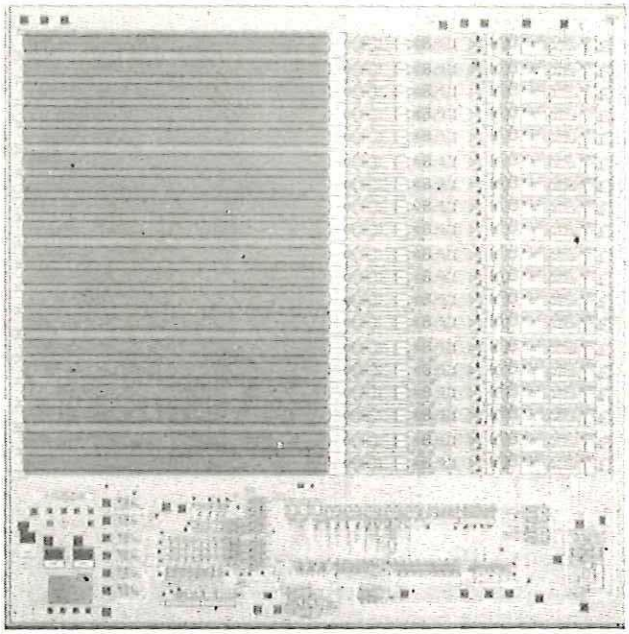


Fig. 13. Photomicrograph of a CCD/NMOS voice analysis IC for a channel vocoder. The IC measures 6.4 x 6.4 mm.

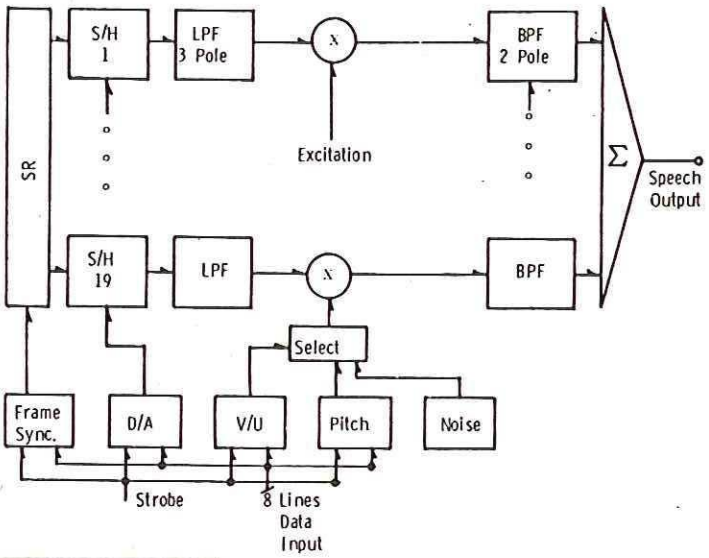


Fig. 14. Block diagram of a voice synthesis IC for a channel vocoder.

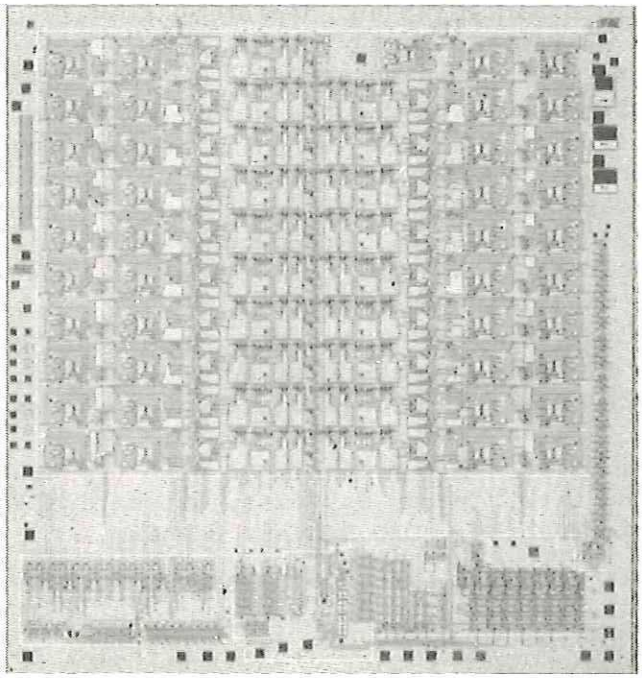


Fig. 15. Photomicrograph of an analog MOS voice synthesis IC for a channel vocoder. The IC measures 6 x 5.6 mm.