PERFORMANCE CHARACTERISTICS OF A CCD ANALOG MEMORY/SIGNAL PROCESSOR

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INTRODUCTION

A device has been fabricated to produce linear, low noise copies of analog waveforms for such applications as scan conversion, signal averaging, and sliding window functions. This Replicating Memory uses a floating gate sensor combined with a fill and spill input to perform replication of charge packets in a CCD serial shift register. Device measurements have demonstrated the feasibility of using this type of charge replication techniques for a wide range of signal processing functions.

DEVICE DESCRIPTION

The Replicating Memory is a device which combines the analog data storage capability of CCDs, with the ability to read them non-destructively. The device consists of two independently clocked 128 stage registers which are interconnected by a charge replicator circuit as shown in figure 1. During device operation, analog data is clocked into the A register and stored there for regeneration into the B register. This non-destructive readout can be repeated as long as the data in the A register remains valid. The output of the B register is the contents of the A register concatenated upon itself at the clock frequency of the B register.

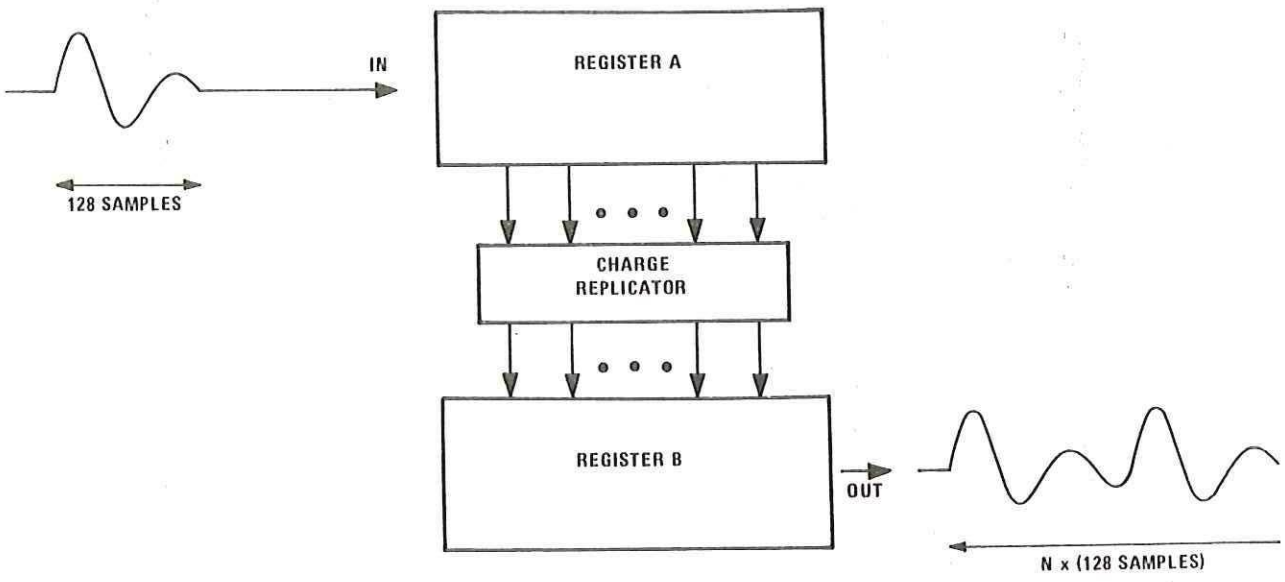

FIGURE 1: CCD SIGNAL REPLICATOR BLOCK DIAGRAM

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The device is designed with a conventional fill and spill input structure on both the A and B registers. The B input is used for test and fat zero injection. Both registers have a floating diffusion output structure with two DC screens for clock isolation. One stage of the charge replicator circuit is shown in figure 2. The A register operates much the same as a floating gate transversal filter, with $\emptyset_C$ used to reset the floating gate to the quiescent value V_C. This condition is shown at T1 in figures 3 and 4. The $\emptyset_S$ diffusion is also pulsed negative at this time to fill the fill and spill structure of the charge replicator. On the falling edge of $\emptyset_{2A}$ signal electrons are clocked to the floating gate in the A register and the resulting voltage change causes electrons to spill out of the fill and spill circuit. The charge replication process is therefore inverting. Although a non-inverting structure could be built by floating the first gate in the fill and spill structure instead of the third, this would result in considerably more clock feed-through.

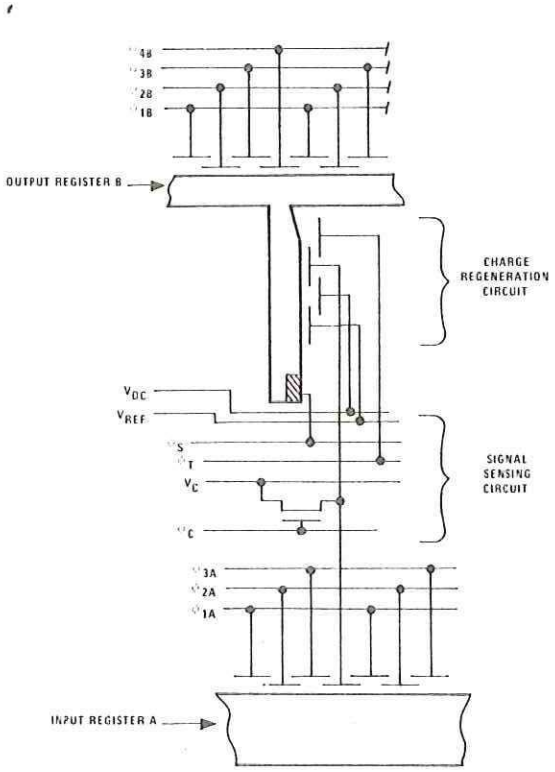

FIGURE 2: CIRCUIT SCHEMATIC DIAGRAM

The fill and spill circuit in the replicator has been designed with three gates rather than two so the reference and input (floating) gates are on the same poly level. This technique minimizes the fixed pattern noise generation due to threshold variations since the thresholds on a single level of poly can be very well controlled. The gate between the two poly 1 gates is biased at a high postive potential so it acts only as a storage well.

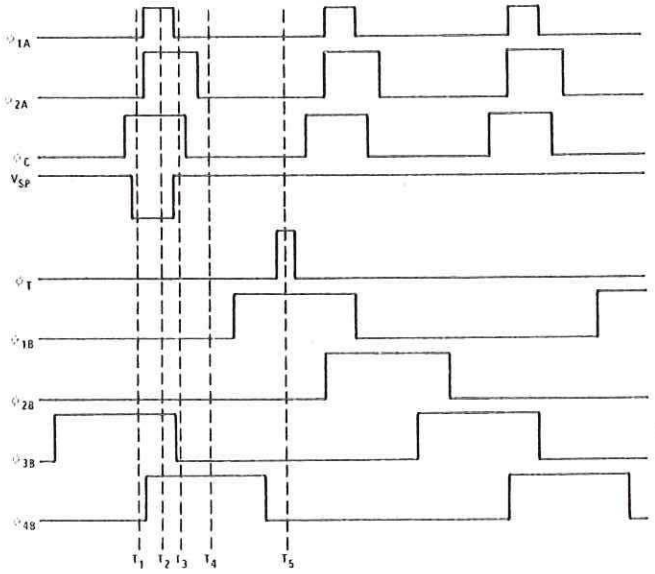

FIGURE 3: PROCESSOR TIMING DIAGRAM

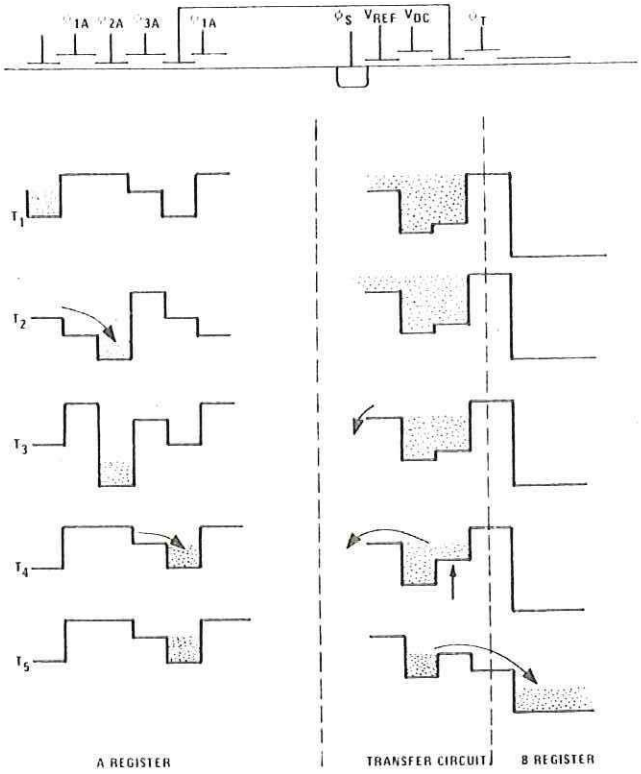

FIGURE 4: CHARGE TRANSFER SEQUENCE

EXPERIMENTAL RESULTS

The Replicating Memory was fabricated at the Honeywell Solid State Electronics Center using a double poly NMOS process. A photograph of the device is shown in figure 5.

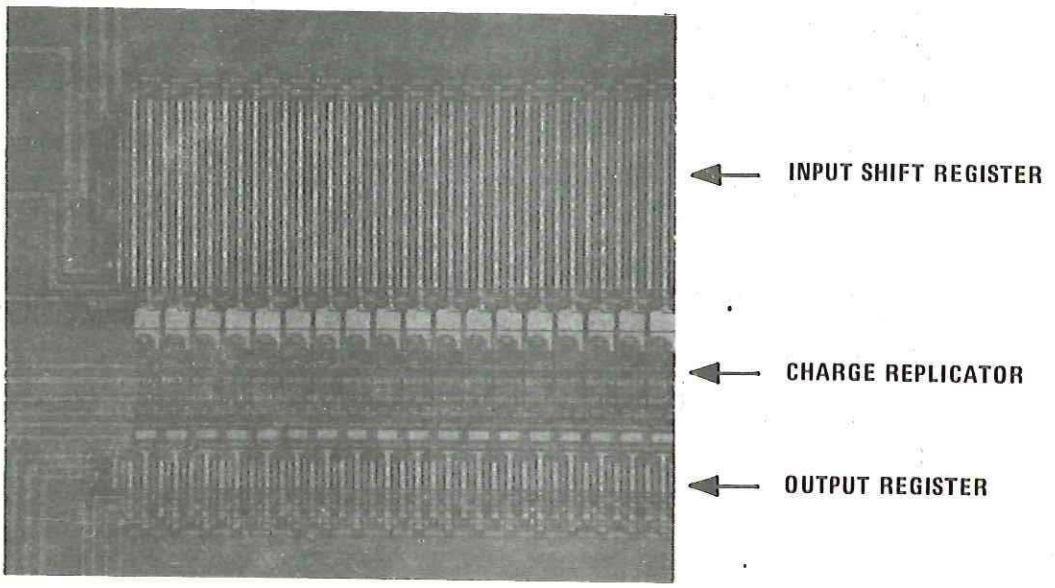

FIGURE 5: PHOTOMICROGRAPH OF CHARGE REPLICATOR

To test the device a fixture was fabricated which would clock the B register continuously while clocking the A register in at intervals which were synchronized to the B register. The output circuits on each register were observed and the resulting waveforms are shown in figure 6. The input waveform was regenerated 16 times in this case with no significant degradation with time. A blow up of one of the edges of the triangle waveform out of the B register is shown in figure 7. The linearity of this curve is better than 1% but is difficult to measure because of the fixed pattern noise created by the replication process.

One of the prime measures of the utility of the Replicating Memory is the uniformity of the replication process. Figure 8 is an expanded view of the output of the B register of the device with a DC input to the A register being replicated. It was expected that the main cause of this nonuniformity would be threshold variation on the parallel fill and spill inputs. From figure 8, we see that the fixed pattern noise consists of a random distribution of offsets along with a larger offset appearing at the first 7 output bits. A relatively good correlation exists between the random distribution and the CCD threshold variations, but it is felt that the larger offsets from the first 7 output bits is design related since the same characteristics appeared on all the devices tested.

At the present time, the Replicating Memory dynamic range (limited by the fixed pattern noise) is 43db. The device, however, can be operated in a self-compensating mode by initially injecting a uniform array charge packet into the A register input and combining the inverted fixed

pattern noise with the input signal thus increasing the dynamic range of the device to greater than 60db.

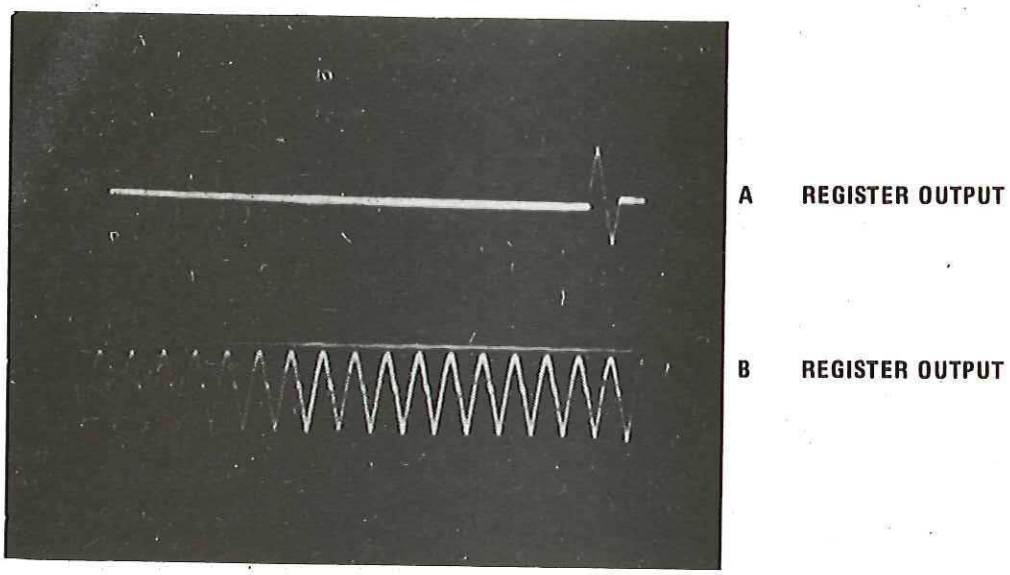

FIGURE 6: CHARGE REPLICATOR PERFORMANCE CHARACTERISTICS

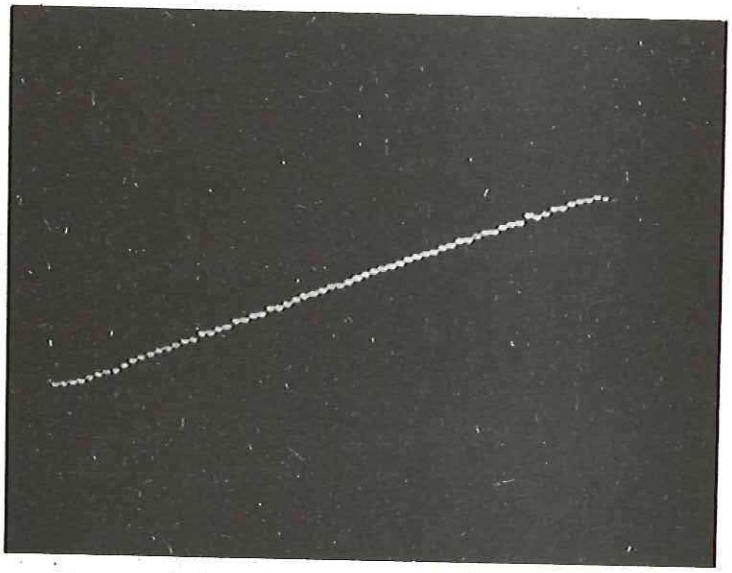

FIGURE 7: DETAIL OF A TRIANGLE WAVE OUTPUT FROM THE B OUTPUT REGISTER

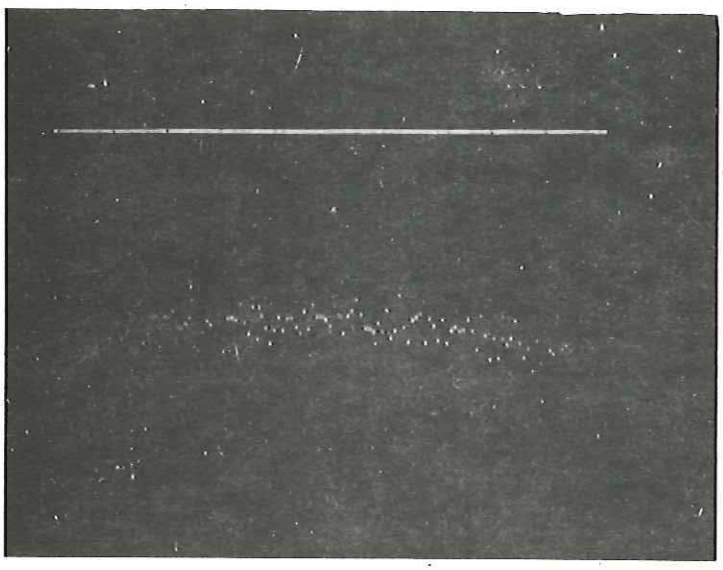

FIGURE 8: DETAIL OF DEVICE NONUNIFORMITIES FOR A UNIFORM INPUT SIGNAL

CONCLUSIONS

A CCD device which will accurately and nondestructively reproduce segments of analog waveforms has been fabricated and characterized. The measured performance characteristics of this device demonstrates the feasibility of the use of this unique structure for a large number of signal processing applications.