# A CCD VIDEO INTEGRATOR

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## ABSTRACT

In situations where noisy, repetitive signals are encountered a video integrator provides a convenient method for averaging over several batches of data to improve the signal-to-noise ratio (SNR). A comparison of different architectures to provide such a video integrator for a system requiring an input data rate of 100 MHz and and output rate of 5 MHz with a signal utilisation efficiency of at least 50% will be outlined. It is shown that a low-power, compact, CCD implementation has distinct advantages. The inherent limitations of dynamic range and linearity are not a major drawback, particularly for noisy signals. The implementation of such a CCD video integrator comprising an anti-aliasing input filter, 384 delay elements and summation in each element of up to 10 input data batches is described. The performance of such a device is illustrated. Finally, possible implementation of the video integrator as a means of recovering information from the output of surface-acoustic wave filters will be discussed.

## INTRODUCTION

In many situations averaging over several batches of noisy repetitive signals is required to improve the SNR. Obviously such averaging is only of value for synchronous signals which are, of course, commonly encountered in radar-like applications. If it is required that this video integrator should accept continuous data at the maximum rate then it is not possible to use conventional bandwidth compressors whose low output clock rate reduces the signal-utilisation efficiency. What is required, therefore, is a video integrator capable of accepting input rates of 100 MHz with an output rate of 5 MHz and with a signal utilisation efficiency of at least 50%. This specification implies that the integrator must be capable of performing at least 10 integrations on successive batches without consequential reduction in linearity or dynamic range. In addition we shall seek to obtain a small-scale, low power method of achieving this performance.

## VIDEO INTEGRATOR ARCHITECTURE

Three particular structures will be considered for such a video integrator as illustrated in Figure 1:

(i) digital system based on high-speed random-access memory (RAM).

(ii) digital system based on high-speed shift registers.

(iii) a CCD implementation.

Initially there are two particular points that can be made about digital methods. Firstly, the analogue input will require digitising in

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an ADC at the 100 MHz rate to whatever number of levels is appropriate. While such ADC's are available they are, at present, somewhat bulky with rather high power consumption. The CCD structure on the other hand accepts analog high-speed data and only requires an ADC at the low-speed output stage with consequent miniaturisation and power reduction. Secondly, in order to achieve 100 MHz operation, digital implementation would probably be based on ECL technology, which is inherently high-current and therefore not capable of large scale integration. CCD's are inherently low-current devices with consequent possibilities for circuit complexity with low power consumption.

Comparing the three architectures individually:

(i) In the system based on high-speed RAM shown in figure 1(a) it is necessary for three operations to take place within the basic clock interval (T): (a) read memory at given address, (b) add to data, (c) write to memory. Since three operations are required this structure is likely to require a high degree of multiplexing to achieve the desired input data rate.

(ii) The shift register architecture shown in figure 1(b) is inherently faster than the previous method since only one operation is required in any clock interval. However all the data must be clocked simultaneously at the high rate. Thus it is likely to require high power.

(iii) Both the digital methods would be expected to consume more power than the CCD structure shown in figure 1(c). Most of the processing is on-chip in this case so that little power is consumed in driver circuits compared with that required in both digital structures. Most of the power consumption in this method takes place in the phase clock generation and driver circuits. Thus the CCD implementation has definite size and power consumption advantages. However the CCD does exhibit the disadvantage of restricted dynamic range and linearity. Typically the output dynamic range would be limited to 50-60 db in which case the input dynamic range before integration over 10 batches would be 30-40 dbs. This essentially restricts the input SNR to less than 30-40 dbs in order for the CCD not to introduce distortion. In applications where SNR's are lower than this value, therefore, this CCD architecture offers significant advantages over its digital equivalents.

## ANTI-ALIASING INPUT FILTER

It is frequently necessary to sample signals at some interval T in the presence of noise whose bandwidth, $B_n$, greatly exceeds the sampling bandwidth, $B = 1/T$. Instantaneous sampling would alias these out-of-band noise components into the sampled signal, reducing the available SNR. Prior passage of the data through a filter of bandwidth B would, however, give an SNR improvement of $B_n/B$. Such a filter can be realised in CCD by utilising the transient dynamic properties of its input. It has already been demonstrated that multiplication can be achieved at the input (ref 1) and that, by multiplying the signal by a constant, integration of the signal over the sampling interval T is possible (ref 2). A technique using integration on MOS capacitors has been suggested which is essentially the same (ref 3). In principle, this type of filter using transient dynamic injection to the CCD, offers the desired filter characteristics ie

(1) The output is band limited so that $B \sim 1/T$; thus out-of-band components are rejected. Changing the sample time automatically adjusts the filter bandwidth.

(2) This form of filter introduces no correlation between samples, unlike other filter profiles.

Detailed measurements (ref 2) on such a CCD having two input gates (an essential requirement) has shown that acceptable linearity and dynamic range can be achieved. Some of these results are illustrated in figures 2 and 3. Figure 2 shows the dependence of the output on time which demonstrates adequate linearity over an integration time of 60 ns for such a device, as has also been demonstrated in refs 2 and 4. The relationship between the output ($\delta V_{out}$) and input ($\delta V_{in}$) signals is shown in figure 3(a) demonstrating reasonable voltage linearity. A more sensitive measure of distortion is to study the total harmonic content in the output compared with the fundamental. This is illustrated in figure 3(b) for a range of integration times and input signals. It is preferable (ref 2) to apply the signal to gate 2 (full line) rather than the input diode (dashed line), in which case for a sample time of 10 ns a total harmonic content of about -50 db would be obtained for $\delta V_{in} = 0.15V$. The input giving an output in the fundamental equal to the noise was $\delta V_{in} = 0.3$ mV so that the dynamic range under these conditions is 54 dbs. Thus dynamic range and linearity for such an anti-aliasing input filter are certainly compatible with normal CCD performance. Accordingly the CCD video integrator described here includes this input option.

## VIDEO INTEGRATOR IMPLEMENTATION

The artwork for a 3-phase CCD based on the architecture of figure 1(c) is shown in figure 4. The input register and integrating section can be clearly seen. It is apparent that the device does not correspond to figure 1(c) in that no separate buffer register was provided. This device gives 128 delay elements and is capable of operating in excess of 30 MHz. Thus, multiplexed three ways, such a device should provide 384 delay elements with an input rate approaching 100 MHz. Results demonstrating integration of a single cycle of sine wave with an input rate of 75 MHz and an output rate of 5 MHz are shown in figure 5. This includes all the required multiplexing and demultiplexing. Some problems associated with this device are readily apparent:

(1) Clock breakthrough: Mosy of the "noise" visible is due to clock breakthrough spikes. With suitable choice of sampling window on the subsequent ADC this problem is largely alleviated.

(2) Gain and offset mismatch: Different CCD chips were used in the multiplexed system each requiring output amplifiers with adjustable gain and offset before demultiplexing. By incorporating the three multiplexed devices on the same chip matching should be improved.

(3) Excess field dark-current: Since the integration time is about 2 ms dark current should not present a problem. However in the current device charge-pumping occurs over the whole chip area. This problem should be removed by the inclusion of a field dark-current drain; such a technique has been demonstrated on other devices (ref 5).

A redesign is in progress to rectify these inadequacies. In addition by suitably varying the devices on each chip, it is intended to avoid the problem of the many different phase clock waveforms presently required. This should enable the power consumption in the clock devices to be minimised. The redsigned CCD will provide 765 delay elements (multiplexed 3 x 255) on each chip.

## USE OF THE VIDEO INTEGRATOR WITH SURFACE ACOUSTIC WAVE (SAW) FILTERS

A video integrator such as that described here lends itself particularly well to handling the output of SAW filters. Typically these will have signal-utilisation efficiencies of 50% and may well require sampling rates of ~100 MHz for the wideband cases. There is an increasing interest in these for the analysis of noisy signals such as are encountered in optical radar or spectrum analysis. Here SNR's of only -40 db per data batch are not uncommon and it is essential to use video integration of a great number of data batches to achieve an acceptable output SNR. Since the CCD dynamic range and linearity of 40-50 db are closely compatible with the SAW filter output it is appropriate to consider performing the integration over the first 10 batches in the CCD video integrator followed by subsequent integration in low-speed digital LSI. For such noisy signals the limited dynamic range of both devices is unimportant. The most significant limitation is the linearity of the SAW filter which determines the final integrated linearity. Typical SAW responses show linearity to about 10% whereas the CCD linearity is about 1%. Thus the CCD video integrator appears to offer a convenient low-power interface between SAW and low-speed digital technologies without introducing any significant distortion.

## REFERENCES


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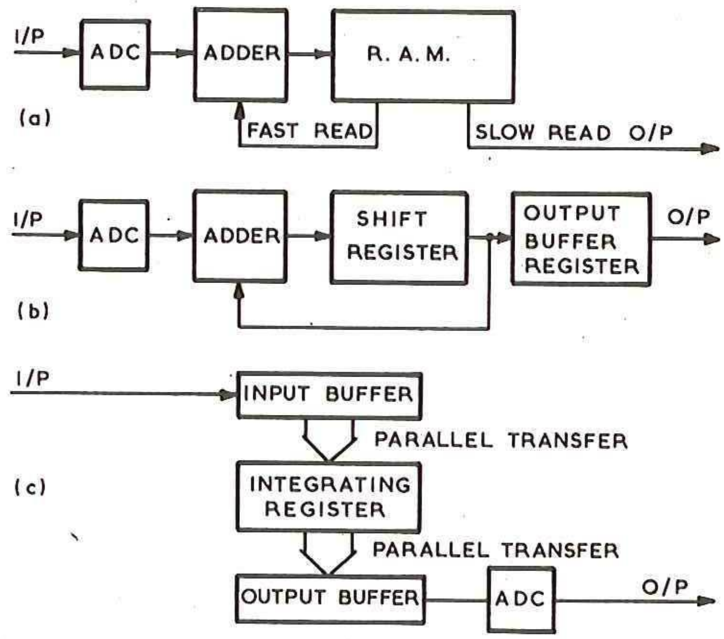


FIG 1: VIDEO INTEGRATOR ARCHITECTURES

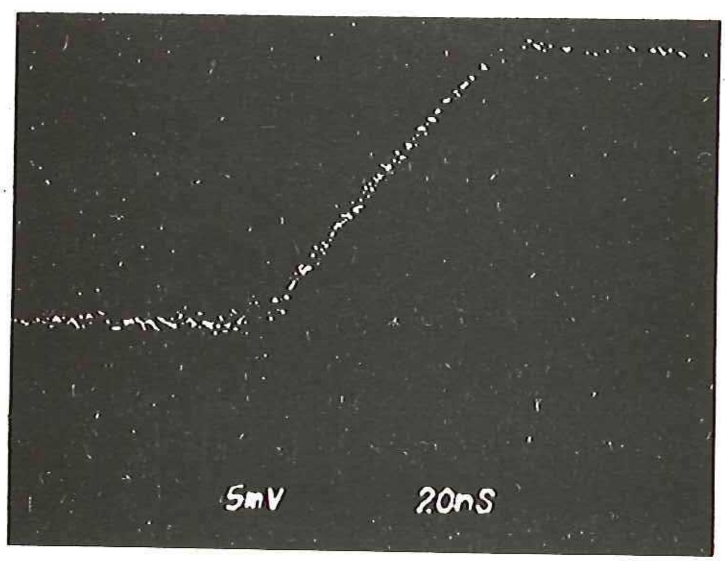


FIG 2: DEPENDENCE OF OUTPUT ON INTEGRATION TIME

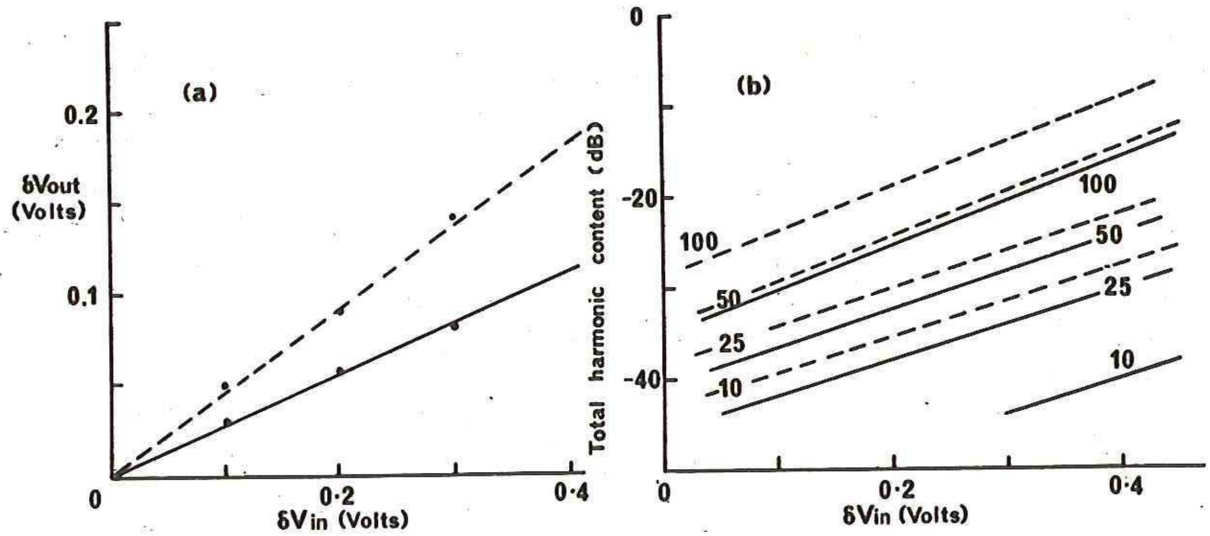


FIG 3: (a) DEPENDENCE OF OUTPUT ON SIGNAL STRENGTH

(b) DEPENDENCE OF DISTORTION ON SIGNAL STRENGTH AND INTEGRATION TIME

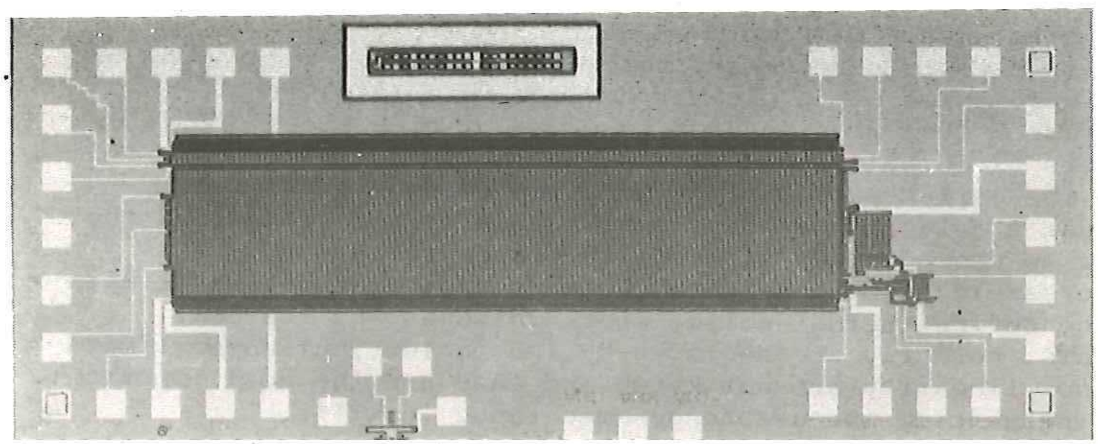

FIG 4: ARTWORK OF CCD VIDEO INTEGRATOR

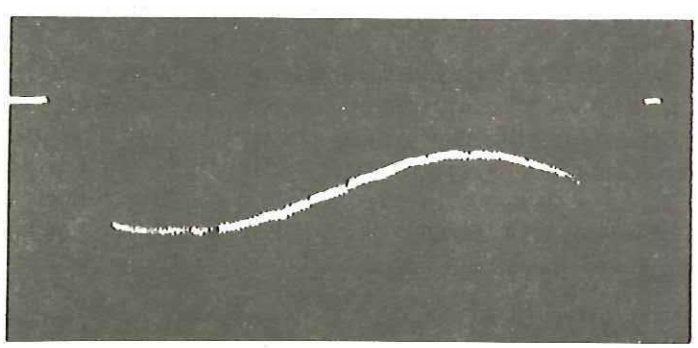

FIG 5: OUTPUT OF MULTIPLEXED VIDEO INTEGRATOR