CHARGE TRANSFER DEVICES FOR BANDWIDTH COMPRESSION

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Currently there is considerable interest in video bandwidth compression both for commercial and military applications. One method of achieving bandwidth compression is to perform an orthogonal transform on a set of signal samples and then remove the redundancy in the transform domain either by discarding higher order coefficients or by digitizing higher order coefficients with decreased resolution. The redundancy in video data arises from the correlation between nearby picture elements. The encoded and bandwidth reduced data is then transmitted. At the receiver the data must be decoded and inverse transformed to recover the video signal. This paper will describe analog integrated circuits devices for performing the transforms and the inverse transforms used in video bandwidth compression.

MATRIX MULTIPLIERS

An orthogonal transform of a sampled data signal S can be represented by the equation: $F_j = \sum_i W_{ij} S_i$. An arrangement of MOS switches and capacitors, termed a matrix multiplier has been devised to perform such a transform.(1) The internal architecture of the chip is shown in Fig. 1. The input signals, which ideally are sampled and held, are presented at the switched nodes where MOS switches can select either the input voltage or a reference potential. The input data is sampled by a two-phase sampling operation between which the switches toggle from one position to the other, causing a step change in voltage on the horizontal matrix lines. These step changes induce charges, $W_{ij} S_i$, on the output plates, which are proportioned to the product of the plate area and the signal voltage. The products are summed on the vertical lines and presented to the output devices shown at the bottom. To implement a positive coefficient, the MOS transistors select the reference potential during phase one and switch to the input signal voltage during phase two. To implement a negative coefficient, the opposite transistors are selected during the respective phases. Thus positive and negative contributions are combined on a single capacitor without requiring any differential amplifiers. Both cases are represented in Fig. 1. A step change in the output is produced at the transition time between phase one and two, and this can be converted back to a signal level by correlated double sampling. That is, the output can be clamped to a reference level in phase one and sampled and held in phase two. This approach has the further advantage of eliminating reset noise.(2)

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Although the matrix multiplier is superficially similar to other circuits where switched capacitors are used to implement a resistor [3] or (in conjunction with op-amps) to implement integrators, [4] the use here is quite different. Here, the objective is to form a desired linear combination of voltages in a single clock cycle with polarity of an individual contribution being implemented by the switching sequence.

Since the summation process is directly performed by superposition, the internal accuracy of the computation only depends on the accuracy of the weighted capacitors. Since the ratio of these plan-view-determined capacitances can be well controlled [5,6] the coefficient values are very precise. The accuracy of the device, however, also depends on the accuracy of the output source followers, and their gain variations can be expected to limit the overall accuracy. Experimental results indicate an accuracy of $\pm 1\%$ can be achieved.

A photomicrograph of a device which performs the Hadamard transform of a set of eight signal samples is shown in Fig. 2. The eight inputs are on the left with input switches just to the left of the capacitor array. The source follower output stages are located at the bottom of the array. The photomicrograph in Fig. 3 shows an eight point device configured to calculate the inverse of the cosine transform of the data samples. The only difference between the devices of Figs. 2 and 3 is the masks used to define the capacitor weights. The single chip mask programmable architecture is particularly useful in performing the forward and inverse transforms on video signals since for orthogonal transforms the inverse is obtained with a capacitor array in which the rows and columns are transposed.

A pair of chips for performing the inverse of a 32-point cosine transform are depicted in Fig. 4. The sixteen low and high order coefficients are obtained from the chip on the left and right, respectively. The entire transform could easily be performed on a single chip, but the particular application dictated the use of a 64-pin package.

The major advantage of the matrix multiplier for calculating transforms is that it is a fully parallel architecture, thereby allowing high speed. The speed is primarily limited by the speed of the MOS switches at the input. All the coefficients for the entire transform can be calculated in 300 nsecs with the present design. In contrast to the devices which use the chirp Z algorithm, where the signal must be premultiplied, convolved and then post multiplied, the matrix multiplier performs the transform directly in a set of parallel multiply-add operations. The disadvantage of a fully parallel architecture is that the devices which implement it become pin limited as the transform block size increases. In the bandwidth compression application, the video data is typically serial and a serial-to-parallel converter is required to use the matrix multiplier. A charge transfer device to perform this function is described in the following section.

SERIAL-TO-PARALLEL CONVERTER

The standard approach to serial-to-parallel conversion is shown in Fig. 5. The video signal is sampled and charge packets proportioned to the signal are transferred serially in a charge transfer device. When readout is desired, the charge packets are transferred in parallel into a set of output amplifiers as shown in Fig. 5. This approach is limited by pattern noise associated with variations in threshholds associated with the parallel transfer [7] and variations in transfer inefficiency in the two directions of charge transfer. Both these problems can be minimized by using square charge transfer cells which are relatively large, but this solution is useful only for relatively low speed applications.

The pattern noise associated with variations in threshholds may be understood by referring to the layout of a conventional CCD serial-to-parallel converter shown in Fig. 6. Note that the effective channel width is reduced in the parallel transfer channel. Since the threshhold of a MOS transistor increases with decreasing channel width [8,9] some charge will be left behind after the parallel transfer even for infinite transfer time [10]. The amount of charge left behind will depend on the exact threshhold at each parallel transfer channel. This charge is subtracted from the signal charge and gives rise to a pattern noise across the parallel outputs.

An approach which overcomes these limitations is shown in Fig. 7 for the case of an eight point serial-to-parallel converter. The video signal is sampled using a conventional fill-and-spill and a charge packet proportional to the signal voltage is transferred under a single long CCD electrode. This charge packet is then divided into eight equal portions which are transferred down eight separate charge transfer channels. For seven out of the eight clock cycles, these charge packets are prevented from reaching the output node by a lateral drain which is held at a negative voltage (p channel). On the eighth clock cycle, the lateral drain is disabled and the eight signal samples reach the output simultaneously where they are held for seven out of the eight clock cycles. The output is a conventional precharge and float circuit with a double source follower to drive about 15 pf of output capacitance.

The device uses 1 1/2 phase clocking for charge transfer. The lateral draining of charge is accomplished with a p-region which extends across the CCD channel as shown in Fig. 8. With the lateral gate turned off the p-region shown in Fig. 9 couples the charge between the gates on either side, in the same fashion as a bucket brigade or a CCD corner turn. When the lateral gate is turned on, the p-region is precharged to a potential which is deeper than the electrodes on either side. Therefore, any charge transferred to this p-region will be lateraly drained and will not reach the output node. This corresponds to the hold cycle of the output sample-and-hold. To transfer

the signal sample to the output node the lateral gate is turned off and the p-region is floated. The signal sample is then transferred to the output node through the p-region just as in a normal CCD, thereby achieving the sample cycle of the sample-and-hold.

When the first charge packet is transferred through the p-region its potential rises to a value determined by the dc voltage on the Φ_D electrode. Since some of the charge is removed from this charge packet to fill the p-region, it no longer represents the input signal and must be discarded in favor of the charge packet which follows it. This is accomplished with the relative timing of the precharge and the lateral gate clock.

A photomicrograph of a serial-to-parallel converter with eight parallel outputs is shown in Fig. 10. The input is at the left and there are five charge transfer stages before the charge is divided into eight equal packets. The lateral gate is connected to the third pad from the right at the top.

The device is designed to sample a standard video raster scan at 10 MHZ and convert it to eight parallel output which are sampled and held at a 1.25 MHZ rate. The output circuit of the chip is designed to drive an eight point matrix multiplier directly with no interface circuitry.

The output of a single channel of the serial-parallel converter is shown in Fig. 11 for a 10 MHZ clock. Channel-to-channel gain variations on the chip shown in Fig. 9 were found to be $\pm$5% at 10 MHZ, but better than $\pm$1% at 100kHZ. The gain variations were systematic; i.e., high on one end and low on the other end. This was attributed to a variation in the potential for the long polysilicon input electrode due to current flow along the electrode associated with the fill and spill operation at 10 MHZ. The chip has been redesigned to eliminate this problem and preliminary measurements on the redesigned chip indicate $\pm$1 1/2% gain variations at a 10 MHZ clock rate.

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The work described in this paper was accomplished with the cooperation of a large number of people in General Electric. John DeBolt and May Dodge were responsible for the processing. Vince Mitchell and George Dimovsky made the masks. Marshall Quick, John De Noon, John Wargo and Dave Ludington have been actively applying these devices in systems. We would like to acknowledge the support of related video bandwidth compressions programs under contracts (F33615-77-C-1118) and (F33615-78-C-1401) monitored by Ron Belt at Air Force Avionics Lab.

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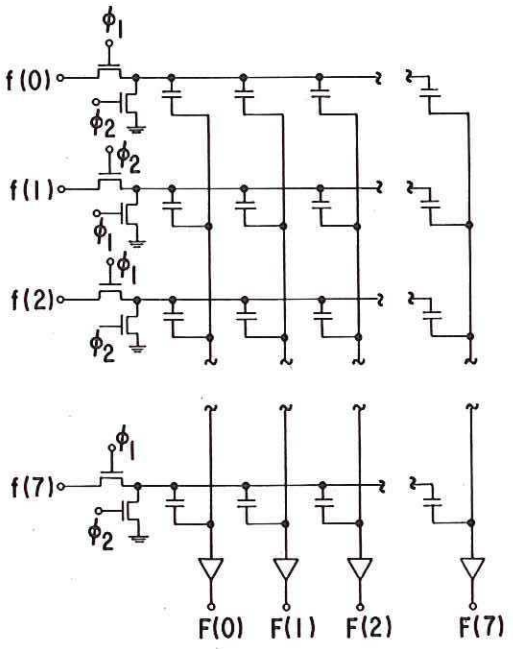

$$F(k) = \sum_{n=0}^{N-1} f(n)\, e^{-j\left(\frac{2\pi nk}{N}\right)}$$

Fig. 1 Matrix Multiplier Architecture

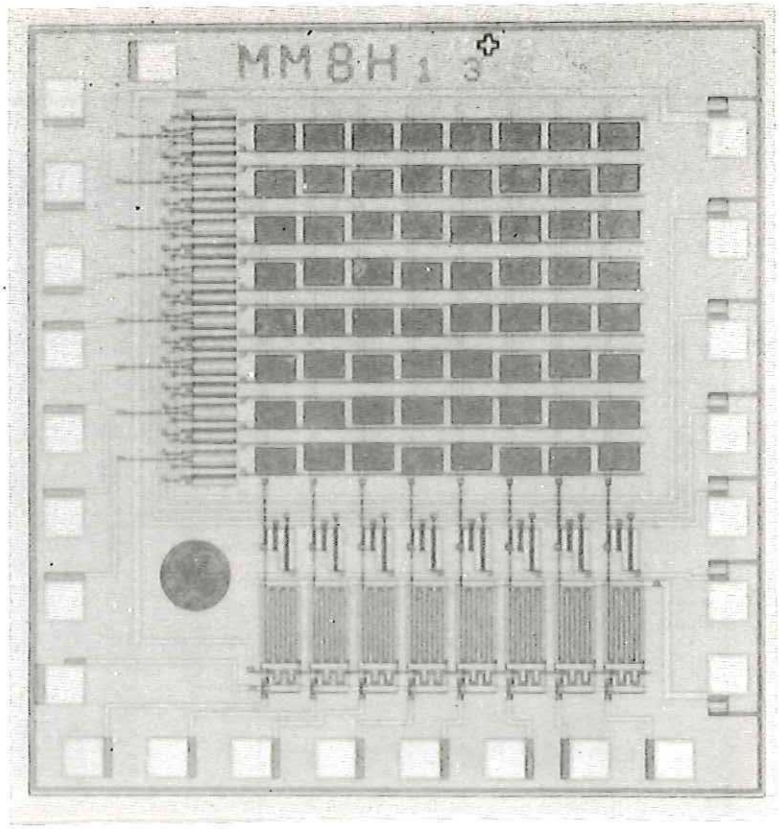

Fig. 2 Photomicrograph of a Chip for Performing an 8 Point Hadamard Transform

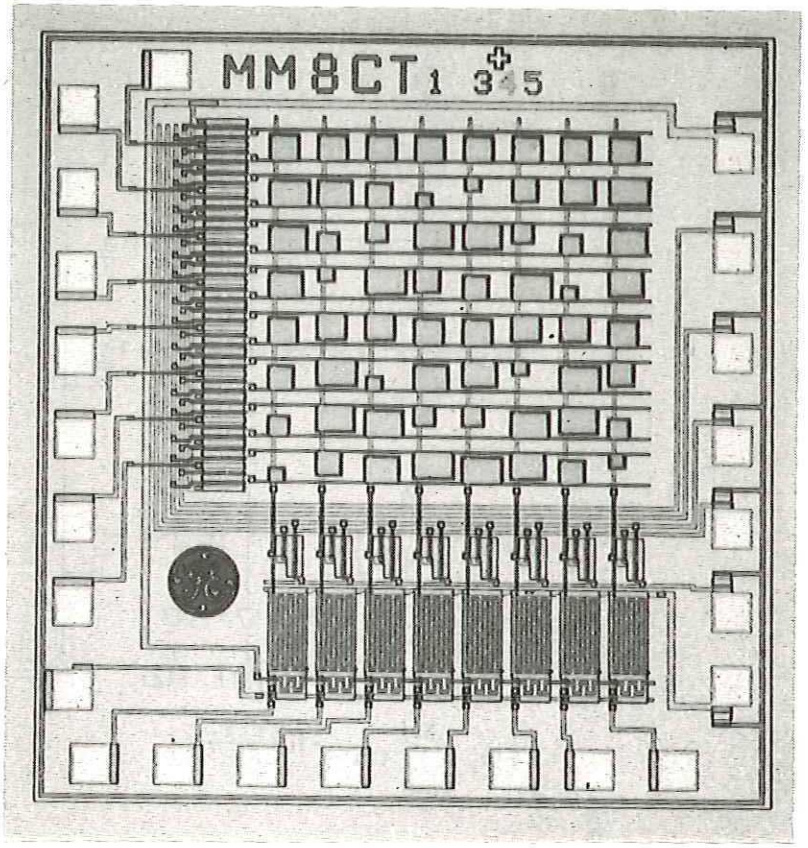

Fig. 3 Photomicrograph of Chip for Performing the Inverse of an eight-point Cosine Transform

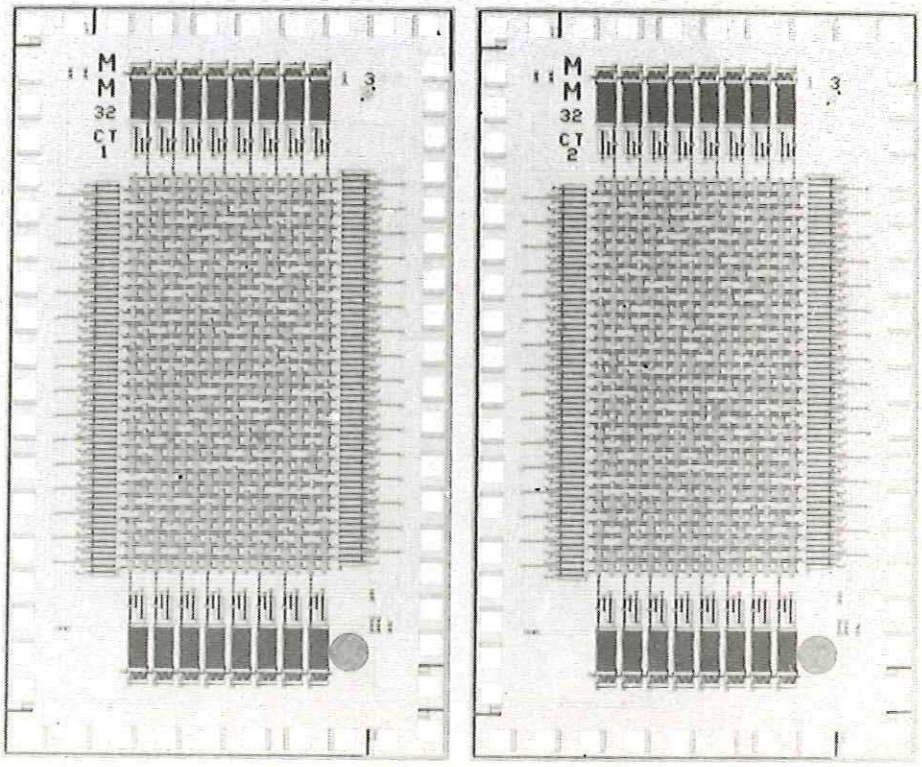

Fig. 4 Photomicrograph of a Chip for Performing the Inverse of a 32-Point Cosine Transform

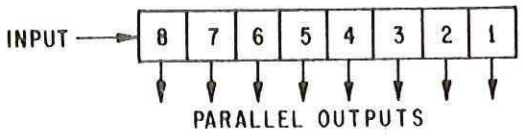

Fig. 5 Conventional Serial-to-Parallel Converter

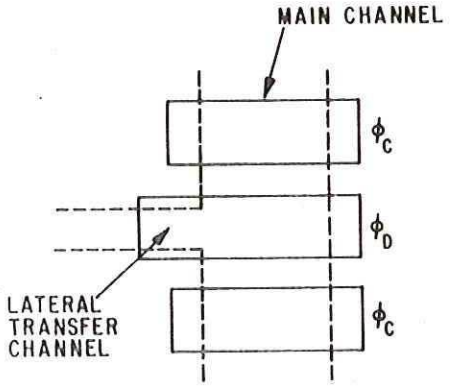

Fig. 6 Layout of Conventional Serial-to-Parallel Converter

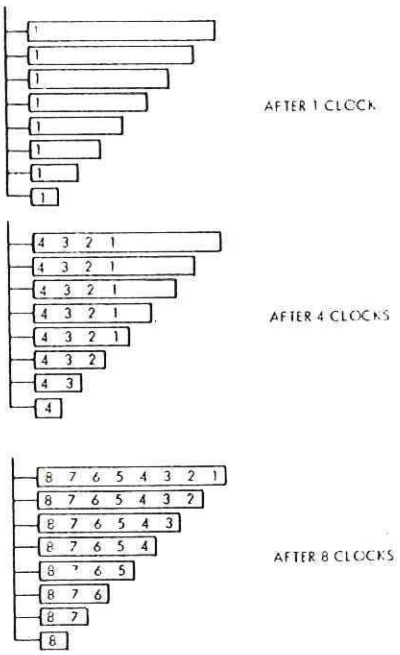

Fig. 7 Data Flow in Serial-to-Parallel Converter

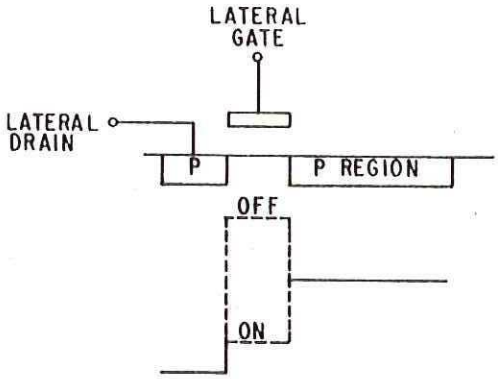

Fig. 8 Cross-section and Surface Potentials across the Channel at the Lateral Gate

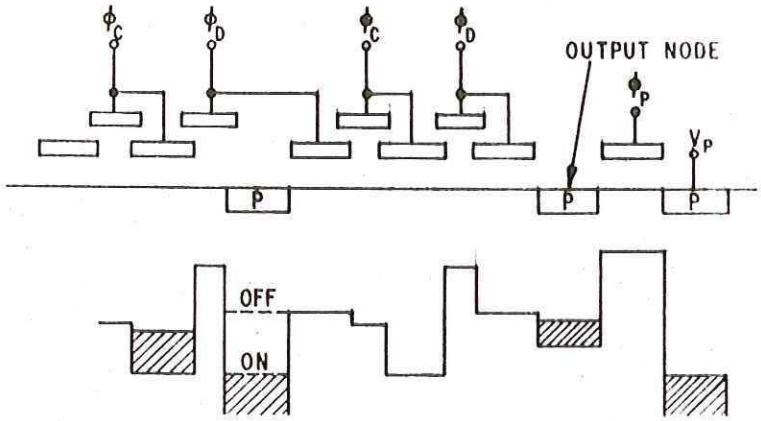

Fig. 9 Cross-section and Surface Potentials along the Channel at the Lateral Gate and at the output node

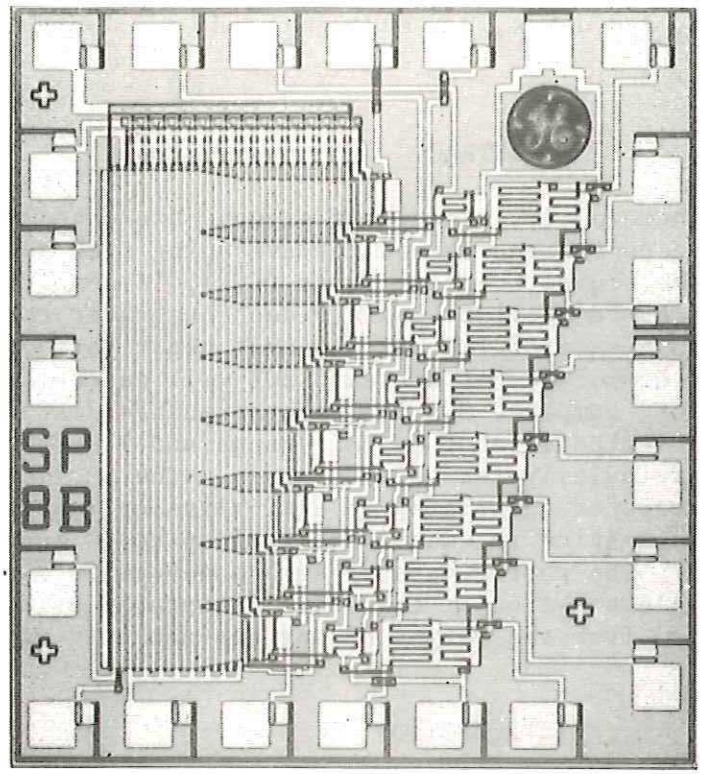

Fig. 10 Photomicrograph of Serial-to-Parallel Converter

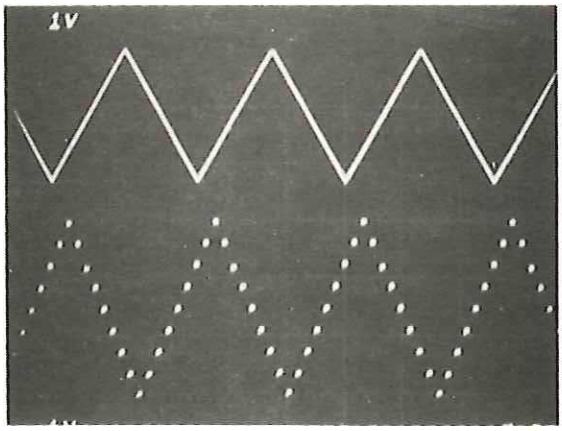

Fig. 11 Input and Output of Serial-to-Parallel Converter for a 10 MHz Clock