A ONE-INCH HIGH RESOLUTION BUTTABLE TDI IMAGING BCCD

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ABSTRACT

The development of a one-inch high resolution buttable TDI imaging device is reported by Bell-Northern Research and Itek Corporation. The device is a 2048 x 96 element buried-channel CCD imager and is fabricated using the BNR double-layer polysilicon gate process. The pixel elements are 13μm square and the time delay operation is in the 96 element direction. The chips are buttable end to end with only 2 pixel elements gap, thus allowing the creation of focal planes having many thousands of elements.

INTRODUCTION

Intensive work has been carried out in recent years on the development of high resolution CCD imaging devices, which are superior to film in many applications. They offer the potential for real-time readout, near-infrared viewing for improved atmospheric penetration and image detection with very low contrast, thus finding use in a variety of areas, including military, medical, and astronomical applications. In applications where the scenery to be imaged has a large linear motion with respect to the CCD chip, the array can be operated in the time-delay-and-integrate (TDI) mode to enhance the signal-to-noise ratio. Some applications also require a large focal plane and this can be achieved with large-dimension buttable CCD imaging devices.

This paper will describe a buttable 2048 x 96 element BCCD imaging device, called the 735A, which was designed to be used in the TDI mode. The resolution in both the X and Y directions is 13μm, and the device was designed to be buttable on both sides in the X direction with less than two pixel spacings between adjacent chips. This device is a third generation product of a joint program of CCD imaging development carried out since 1976 between Bell-Northern Research Ltd., and Itek Corporation.

The precursor to the 735A was the smaller BNR/Itek 719A which was developed primarily as a test vehicle for the 735A. The 719A has been described in ref. 1.

Topics to be discussed include the device design and structure, its fabrication, and representative test results. Emphasis will be placed on those details of the design and fabrication which are unique to buttable, large area devices.

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DEVICE STRUCTURE AND DESIGN

A block diagram of the buttable 735A is shown in Fig. 1. The chip consists of the following sections:

1. TDI imaging area (2048 x 96 elements)
2. Parallel-to-serial interface
3. Serial shift register (1024 stages)
4. Intermediate output taps (7)
5. End output
6. TDI electrical input
7. Shift register electrical input

The combination of overall device length and fine dimensional control near the buttable edges makes it impossible with conventional CAD photomasking equipment to generate the mask set using a single reticle per level. The device was thus designed as a set of subsections, or patches, which were later to be photocomposed. The 735A is organized into eight side-by-side patches, and to simplify design the patches were made as nearly identical as possible. With respect to the TDI imaging area, clock lines, and the parallel-to-serial interface, each patch is similar to the 256-channel 719A chip. The six central patches are identical with the exception of a metal interconnect level, and each contains its own set of clock lines and an output tap. There is no dead space between patches, and the polysilicon electrodes run continuously across the length of the chip.

The device employs 8-phase ripple clocking and "odd-even" interlaced transfer into the shift register to achieve high resolution (ref. 1). The pixel area is 13μm square, and the resulting resolution is 13μm in both the X and Y direction. The charge storage area per pixel is 8μm by 9μm in the TDI array. The device can also be clocked in two-phase and with non-interlaced readout, which decreases the resolution but increases the signal-to-noise ratio. In the vertical direction the number of TDI integrations can be chosen to be 96, 8 or 1, and the first pixel row (nearest the serial shift register) has approximately three times the charge handling capacity of the average sensor array in the TDI array. The larger capacity of the first pixel row gives the device additional flexibility under bright light conditions.

The design goal for buttability was to achieve a gap of less than two pixels between adjacent die, which implies a center-to-center spacing of less than 39μm across the gap. The distance between the scribe channel and the center of the last pixel on the 735A is 18.5μm, including a guard ring diffusion between the last active channel and the buttable edge.

Several design constraints and performance tradeoffs are a consequence of the buttability specification. Since the serial shift register must extend up to the last channel and close to the buttable edge, signal charge readout must take place from the side of the last shift register storage element, as illustrated in Fig. 2. The shift register width must be made large enough to accomodate the maximum amount of charge that can be clocked into it from the TDI array and is approximately 60μm in the 735A. For a shift register of this width, the speed characteristics of the end output preamplifier are dominated by the width of the last storage electrode. Thus the choice of shift register width determines the tradeoff between maximum end output data rate and charge handling capacity of the shift register.

Another feature of the buttable device is that clock line connections to the TDI polysilicon electrodes must run over the active imaging area, because there is not enough space at the edge of the array for

metal-to-polysilicon contacts. The metal lines over the active imaging area are designed so that an equal area of each of the 2048 channels is rendered opaque to optical illumination in either the 96-element TDI mode (4/96 pixels covered) or the 8-element TDI mode (1/8 pixels covered). Two overlapping metal interconnect levels are used.

A major consideration in designing large area devices is to maintain reasonable yields. There are more processing defects per device and fewer possible die per wafer when processing large devices, relative to the fabrication of routine size devices. The experience gained at BNR by processing the 719A lead to a re-evaluation of design rule specifications. The most visible design rule change was increasing the minimum polysilicon electrode gap in the TDI array from 3µm to 4µm. In addition all clock line-to-polysilicon electrode contacts are eight-fold redundant; that is each patch has its own set of clock line connections.

FABRICATION

The 735A wafers are fabricated using BNR's double-layer polysilicon gate CCD process. Active areas are isolated by partially sunken field oxide channel stops, and the entire active area receives an arsenic buried-channel implant. The unit cell in the vertical register consists of a poly1/poly2 pair connected by a butt contact. Charge flow directionality is achieved by a boron compensation implant under the second polysilicon layer. Two aluminum interconnect levels are provided, which are isolated by a CVD oxide layer. A photograph of a completely fabricated 735A is shown in Fig. 3. The overall device measures 26.7 mm by 4.1 mm.

Only 16 potentially good die are placed on a 3" wafer, and each has an area of 1.1 cm^2. Chrome photomasks with extremely low defect densities were generated in order to obtain a reasonable yield. All photolithography is carried out using contact aligners, and working copies of critical layers are recleaned and inspected for defects after each contact.

At the present time experiments are being carried out using chemical etching, plasma etching and mechanical polishing techniques to determine the most efficient method of producing buttable edges. The potentially good die are laid out on the wafer such that all buttable ends are in a line, thus only two buttable edges need to be produced per wafer. A photomicrograph of one side of a buttable 735 die and a SEM detail of the same edge are shown in Fig. 4. Mechanical polishing techniques were used to produce this edge.

EXPERIMENTAL RESULTS

Electrical performance results have been obtained on prototype devices. The transfer efficiency in the serial shift register was measured to be typically 0.99998 at 1 MHz clocking frequency and a signal level of 80% of saturation. The saturation level of the average pixel storage site in the TDI array is 125,000 electrons, and the saturation charge of the pixel storage site in the first sensing row is 350,000 electrons. The saturation level in the serial shift register is 800,000 electrons. Dark current levels have been measured to be less than 4 nA/cm^2.

Mechanically polished and chemically etched 735A die have been butted together with less than the 39 μm pixel-to-pixel spacing specification. No significant increase in junction leakage has been observed near the buttable edge.

ACKNOWLEDGEMENTS

The authors would like to acknowledge the design contributions of A. Ibrahim, K.Y. Yu, and D. Gallant. The authors would also like to thank W.G. Gilmour, J. Saeki, J. Ellul and L. Robinson for their contributions.

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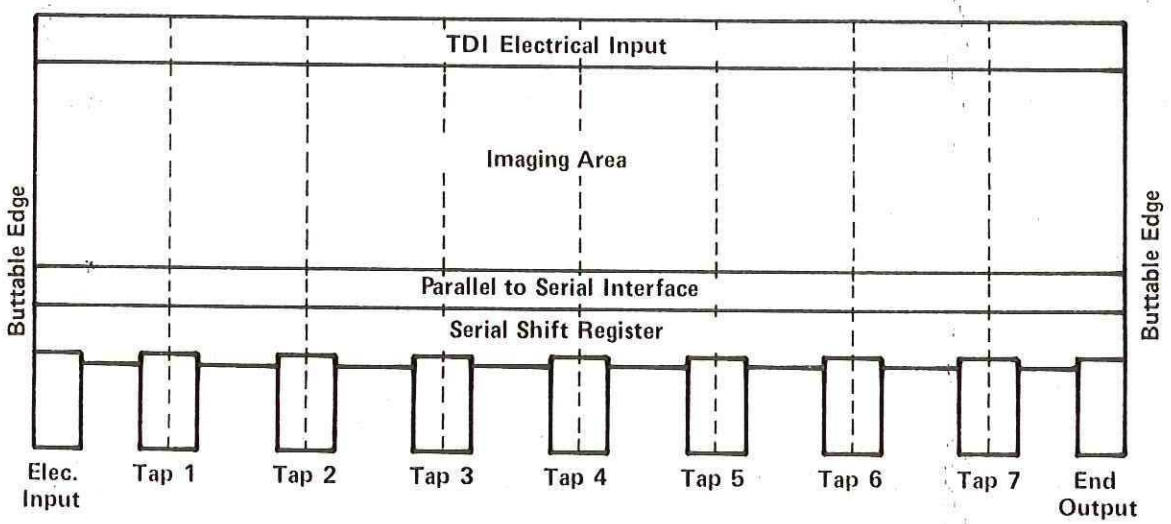

Figure 1 735A Block Diagram

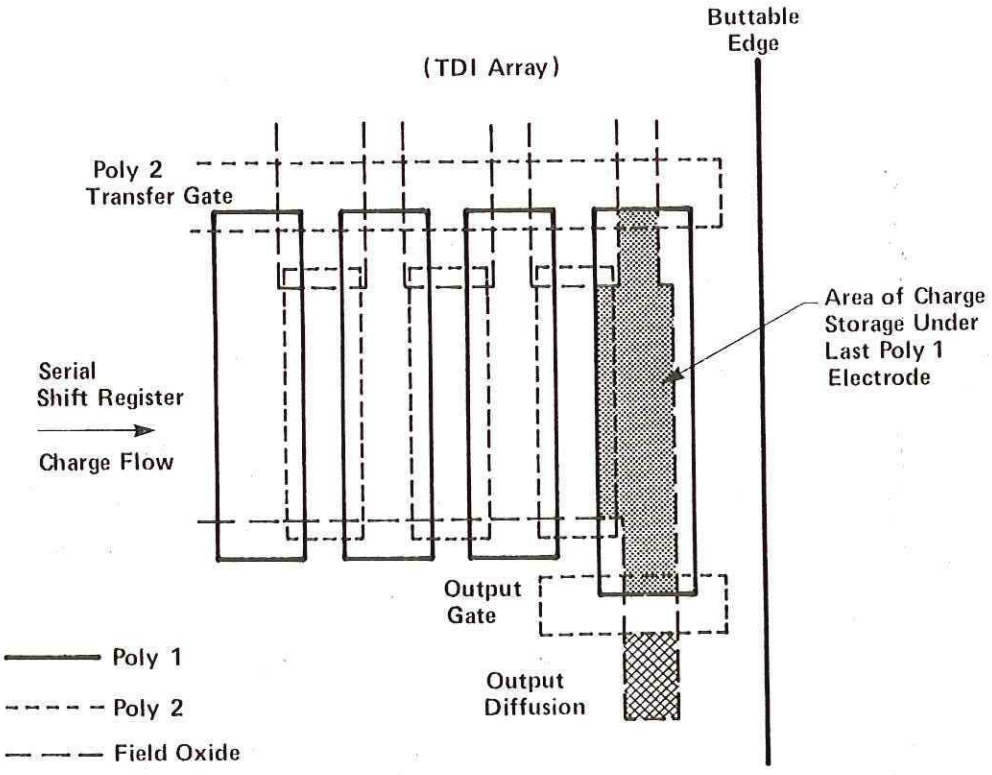

Figure 2 Serial Shift Register Output Near Buttable Edge

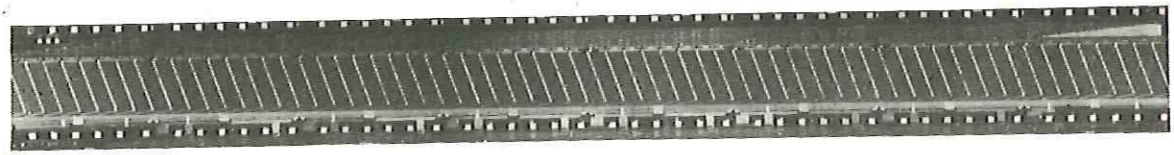

Figure 3 Photograph of 735A Chip

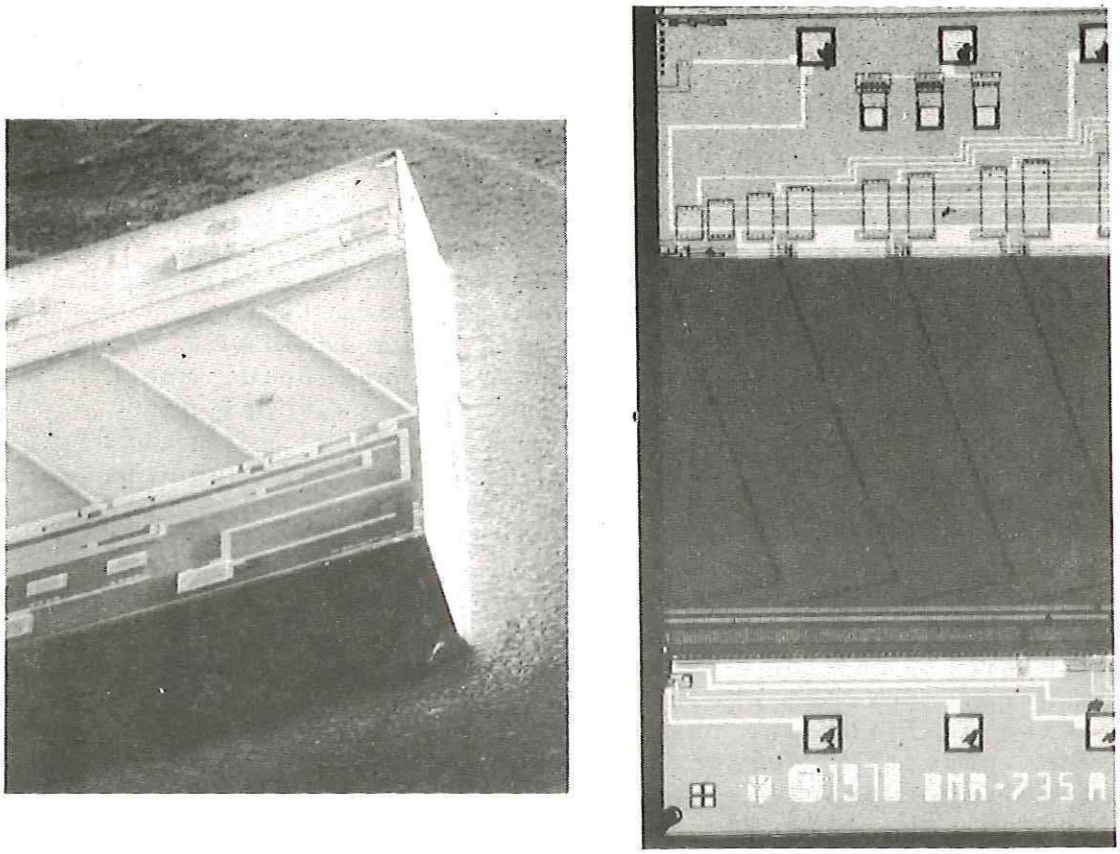

Figure 4 Photographs of Buttable Device and Edge