MOSAIC CCD MULTIPLEXER FOR PYROELECTRIC HYBRID FOCAL PLANE

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ABSTRACT

A pyroelectric detector/Si CCD hybrid focal plane can potentially provide good performance IR detection and imaging at low cost. Room temperature operation and wide, flat spectral response are both attractive features. Flip-chip, bump mounted $LiTaO_3$/CCD modules having 10 x 32 pixels with 50 x 50μm^2 unit cells are under development at Honeywell. The electrical analysis of the directly coupled pyroelectric/CCD interface yields the CCD design requirements that the gate 1/f noise is dominant in the coupling and, therefore, should be minimized, that the CCD input gate capacitance should equal the pyro element capacitance for optimum signal to noise, and that the charge handling capacity should be as large as geometry permits.

Mosaic CCD suitable for pyroelectric hybrid focal plane has been developed having surface channel input structure followed by buried channel shift registers of the mosaic multiplexer. Three independent mosaic multiplexer circuits, each having 10 x 32 pixels, have been implemented; a resettable gate coupled input 100 x 100μm^2 unit cell CCD, using a 2 polysilicon 1 metal process, a floating gate and resettable gate coupled input 50 x 50μm^2 unit cell CCD, both using a 3 poly 2 metal process. The conventional photolithography was used, although the exaggerated topology of the 3 level poly structure has necessitated a refinement of the layout rules to allow for the effects of vertical parallax.

In order to maximize the packing density, the CCD has parallel shift registers placed back to back, and the input circuit makes use of symmetrical layouts. The charge handling capacity, an all important parameter affecting the magnitudes of CCD channel shot noise, dark current noise, and an output reset noise, is 1 x 10^7 and 2 x 10^6 electrons, respectively, for the (100 x 100)μm^2 and (50 x 50)μm^2 unit cell designs. The 1/f noise density in the signal gate, which ultimately determines the pyro coupling noise figure, is found to be of the order of 5 x 10^{-12} V/cm.. The full CCD performance including various noise contributions will be discussed. Finally, the electrical model predicts the detectivity of the $LiTaO_3$/CCD to be in the mid $10^8 cmHz^{1/2}/W$ range for frequencies 1 to 100Hz. The combination of the above mentioned pixel size and detectivity makes the pyro/CCD focal plane suitable for numerous IR detection and imaging applications.

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Pyroelectric/CCD Electrical Interface

Figure 1 depicts the Pyro/CCD focal plane module, in which a flip chip pyro array is physically and electrically mounted via bump interconnects. Gate modulation is the selected signal injection method, in which the individual pyroelectric elements are directly connected to the first (signal) gate of the CCD multiplexer for the gate modulation method. Two approaches are considered.In a floating gate coupled (FGC) scheme, the signal gate potential is set by utilizing the internal resistance of the pyroelectric element. In a resettable gate coupled (RGC) version, the pyro/CCD-gate potential node is d.c. restored via a MOSFET reset transistor from time to time as shown in Figure 2. The enlargement in Fig. 1 identifies the key features of the RGC input circuit.

A pyroelectric detector is, in terms of its impedance characteristics, a moderately good capacitor. As a result, its capacitive reactance dominates its impedance at all but very low frequencies. High input impedance preamplifiers, commonly using J-FET input stages, are used to match the detector characteristics. However, direct coupling between pyroelectric detector and silicon CCD multiplexer is feasible since charge coupled devices with MOSFET type inputs are also high impedance devices. A MOSFET is superior to a J-FET in that a MOSFET is isolated from the silicon substrate by an excellent oxide layer rather than by a reverse biased silicon junction. Consequently, input gate leakage is several orders of magnitude less for the MOSFET. On the other hand, the MOSFET silicon-oxide interface has surface state traps which result in a higher 1/f noise than a comparable J-FET.

A noise model for the pyroelectric detector and CCD input stage is shown in Figure 3. In the frequency region of interest, the detector noise originates from dielectric losses in the material and fluctuations of the thermal interchange in the structure. The CCD noise has four major components: the 1/f-type noise due to surface state traps at the $Si-SiO_2$ interface under the input gate; Johnson noise in the input MOSFET channel; shot noise associated with dark current, and transfer noise in the CCD shift register.

The pyro detector noise is expressed as:

$$e_d^2 = \frac{4kT\ C_d\ \tan\delta}{\omega C_\Sigma} + 4kT^2 R_v^2 C_\Sigma \qquad (1)$$

where $\tan\delta$ is the dielectric loss factor, C_d is the detector capacitance, C_Σ ($= C_d + C_g + C_s$) is the sum of the pyro, CCD gate and stray capacitances, and R_V is the voltage responsivity of the element. When referred to the input gate, the major CCD noise contributions take the expressions as follows:

$$e_c^2 = \frac{2\pi\gamma kT}{C_{ox}C_g\omega} + \frac{4(n_g kT)^2\tau_c}{q^2 N_{max}} + \frac{8J_\phi A_w N(n_g kT)^2\tau_c}{q^3 N_{max}}$$

$$+ \frac{32}{3} \cdot \frac{(n_g kT)^3}{q^4} \cdot \frac{C_o\tau_c}{N_{max}^2} \qquad (2)$$

The definitions of the terms are: γ is the 1/f noise density, C_{ox} the oxide capacitance, n_g the gate transconductance derating factor, τ_c the integration period, N_{max} the maximum CCD charge handling capacity, J_ϕ the dark current density, A_w the shift register area, N the number of shifts and C_o is the output charge sense node capacitance. The relative noise contributions between the detector and CCD determine the design of the hybrid focal plane module.

Multiple Sample Integration

All the CCD noise contributions, except the 1/f noise, are seen to contain the term τ_c (signal integration period) in the numerator and N_{max} (maximum charge) in the denominator. Although a large charge capacity is desirable, N_{max} is restricted in a mosaic CCD structure in a planar configuration; for instance, surface channel CCD typically carries 2×10^{12} electrons/cm^2 for a 10 V well and buried channel carries half as much. What is possible, however, is to implement an off-focal-plane signal processing technique called "multiple sample integration", and effectively reduce the on-focal-plane integration period τ_c. It entails reading out the focal plane several times during a nominal frame period (say, 60 frames per second) and integrating the output in an external frame store. The net result of MSI is to reduce the CCD noise to only the 1/f type noise contribution. Just how many samples are required can be seen from a realistic assessment of these noise contributions as shown in Figure 4. It is seen that 5~10 samples would be adequate.

Optimum Matching Criteria

An unconnected pyro detector will exhibit voltage responsivity R_{vo} given by

$$R_{vo} = \frac{p}{A_d \varepsilon C' w} \qquad (3)$$

where p is the pyroelectric coefficient, A_d the detector area, ε dielectric constant and C' volume specific heat. When connected to the CCD gate, the voltage responsivity is capacitively divided such that:

$$R_v = \frac{C_d}{C_d + C_g + C_s} R_{vo} \qquad (4)$$

The predominant noise remaining after MSI is the 1/f type gate noise given by

$$e_n = \frac{2\pi\gamma kT}{C_{ox} C_g \omega} \qquad (5)$$

The signal to noise ratio of the sensor, expressed as detectivity D*, is given by

$$D^* = \frac{R_v\sqrt{A_d}}{e_n} = \frac{p}{C't} \cdot \sqrt{\frac{A_d C_{ox}}{2\pi\gamma kT\omega}} \cdot \frac{\sqrt{C_g}}{C_d + C_s + C_g} \qquad (6)$$

where t is the pyro detector thickness.
This expression contains the key to designing the mosaic hybrid focal plane. It first of all exhibits the familiar pyroelectric dependence of the signal to noise inversely proportional to the square root of the frequency. Secondly, there exists an optimum value of the CCD gate capacitance at $C_g = C_d + C_s$, namely the matching criterion is that the CCD gate capacitance be made equal to the sum of the detector and stray capacitances. The D* value has a peak value given by

$$D^* = \frac{p}{2C't} \sqrt{\frac{A_d C_{ox}}{2\pi\gamma kT(C_d + C_s)\omega}} \qquad (7)$$

One readily obtains a value of $D^* = 3 \times 10^8$ cmHz$^{\frac{1}{2}}$/W a (4x4) mils^2 $LiTaO_3$ element mounted on a mosaic CCD, when appropriate parameter values such as $t = 25\mu m$ and $\gamma = 1 \times 10^{-10}$ F/cm^2 are inserted in the above equation.
The detectivity value improves as the CCD noise parameter γ is reduced, until the intrinsic detector noise is reached. It is instructive to assess the effects of the CCD noise on the focal plane performance. The dielectric noise due to the materials loss factor $\tan\delta$ is dominant at high frequencies and has the same frequency dependence as the CCD input referred 1/f noise. One can take the ratio to be the frequency independent noise figure of the coupling.

$$N.F. = \frac{e_d^2}{e_c^2} = 1 + \frac{2\pi\gamma}{\tan\delta\ C_{ox}} \qquad (8)$$

This relationship in dB is plotted in Figure 5. When γ values are reduced to values one order of magnitude smaller than presently available (from 10^{-10} F/cm^2 to 10^{-11} F/cm^2), nearly detector noise limited multiplexing would become feasible.

Mosaic CCD Development

Figure 6 gives the chip layout of the Honeywell CCD currently developed for the pyro-focal plane. There are three blocks of 10 x 32 element mosaic multiplexers, with the total of 960 detector pixels. Two blocks have 50 x 50 microns^2 unit cells, where one has a floating gate coupled (FGC) input circuit, and the other a resettable gate coupled (RGC) circuit. The third block consists of 100 x 100 microns^2 unit cells with resettable gates. The maximum charge capacity is estimated at 2 x 10^6 and 10^7 electrons, respectively. In addition to the mosaic CCD multiplexers having bump interconnects, the identical unit cells are laid out in a separate location in a manner accessible for electrical tests. Parameters such as threshold voltage variations, gain, linearity, noise and dynamic range can be independently determined.

Summary

The Pyro-on-CCD focal plane concept is being pursued at Honeywell. The detectivity of mid 10^8 in the frequency range 1 ~ 100 Hz over 1 ~ 30 microns IR should be demonstrable in the current R/D phase, and an order of magnitude improvement is likely in the long run. Even with the modest D* values, it is only a matter of a few years when the pyro-on-CCD focal plane with its room temperature operation, flat IR spectral response and potential low cost will find some military and commercial applications.

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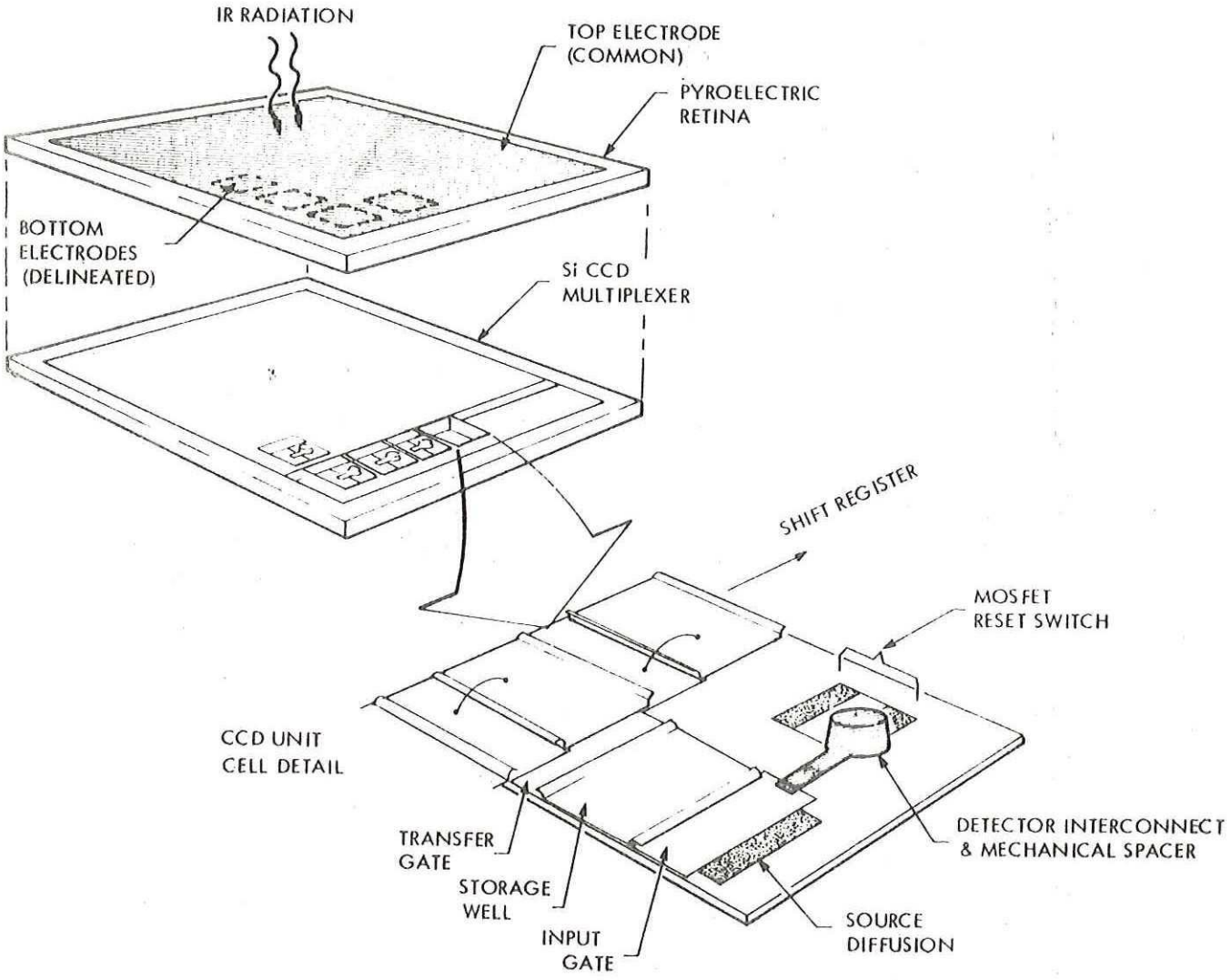

Figure 1. Pyro-on-CCD Hybrid Focal Plane Concept

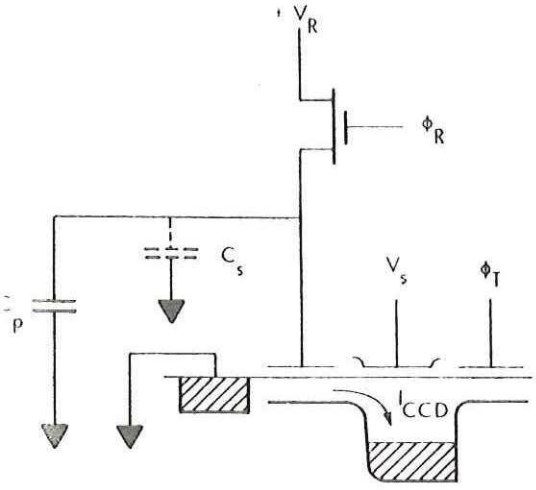

Figure 2. Resettable Gate Couple Signal Injection Scheme

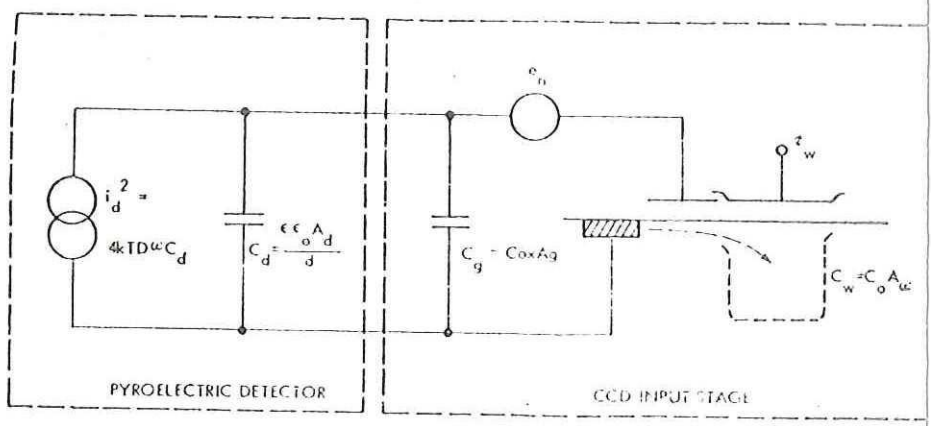

Figure 3. Noise Model

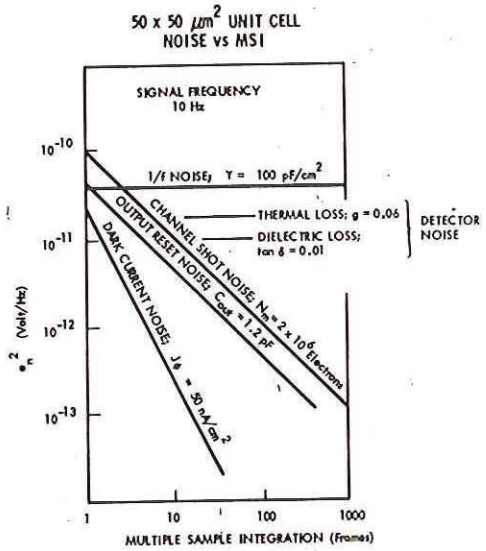

Figure 4. Multiple Sample Integration

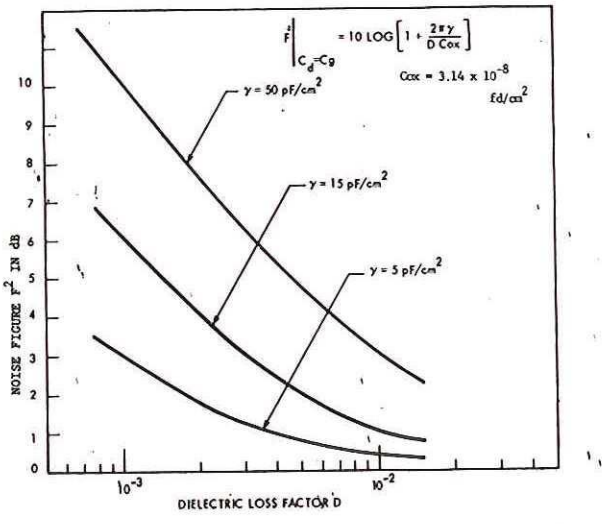

Figure 5. Pyro-on-CCD Interface Noise Figure

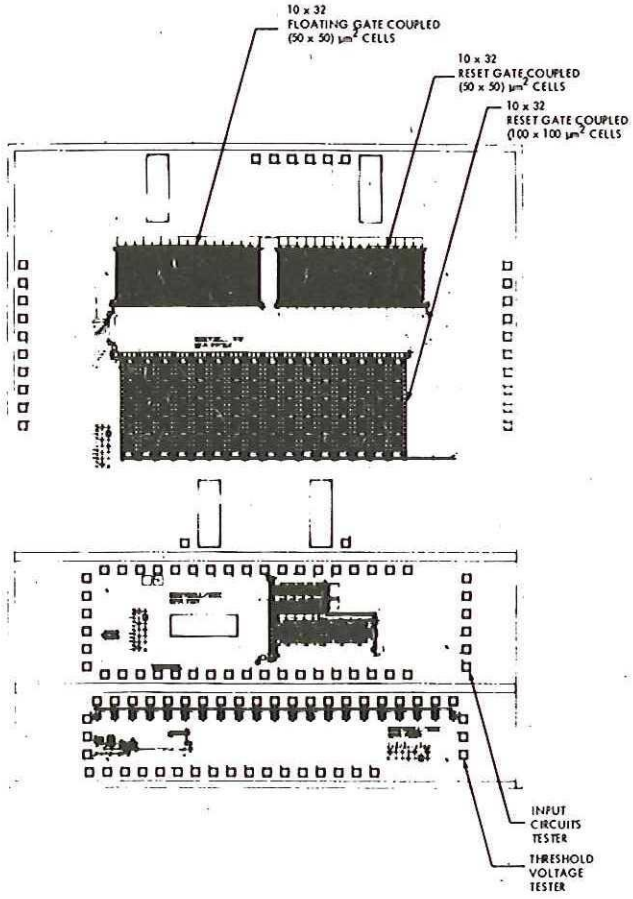

Figure 6. Mosaic Pyro/CCD Chip Layout