MULTIPLEXED HIGH-PASS FILTERS FOR INFRARED SIGNAL PROCESSING

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ABSTRACT

Responsivity non-uniformities in IR detector arrays can result in output variations from background radiation which are several orders greater than the minimum detectable signal. To overcome this problem, a high pass filtering function must be applied to the output of each detector in the array.

A novel technique, based on CCD technology, for implementing such a bank of filters is outlined together with the results obtained from a fabricated device.

INTRODUCTION

High performance infrared imaging and search systems must be capable of detecting signals close to the level of the noise generated by the background radiation falling on any detector in the system. The minimum detectable signal may therefore be three or more orders of magnitude smaller than the background signal on the detector. Any non-uniformities in responsivity from one detector to another, when combined with offsets attributable to readout circuitry, will therefore result in offset errors which may be as large as 60 dB above the signal to be detected.

An appropriate technique for suppressing these offsets is to use a bank of high pass filters, with a separate filter for each detector and a means for multiplexing the signal into and out of its filter.

Several stringent requirements must be placed on a high pass filter for such an application, the most important of which is its dc rejection. This must be 60 dB or greater to adequately suppress the background and give offsets which are comparable to the noise level. Additionally, the 3 dB break frequency must be a small fraction of the sample rate; for example, a 3 dB frequency of 70 Hz for a 12.5 kHz detector readout rate. Another requirement is that the filter 3 dB frequencies be predictable, accurate, and well matched both within a chip and from chip to chip. Finally, any fixed pattern noise such as may arise when multiplexing the filter outputs must also be smaller than the noise level.

In the next section, the theory of the switched capacitor implementation of a high pass filter will be outlined together with a brief discussion of the features and disadvantages of such a filter in this application.

This will be followed by a detailed discussion of the CCD implementation of a multiplexed high pass filter bank for an IR search application.

Finally, the results obtained from a fabricated filter bank will be presented. This device was designed as part of a larger signal processor chip. It has been successfully mounted in a cryogenic chamber next to an indium antimonide CID array and operated at 77° K.

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SWITCHED CAPACITOR HIGH PASS FILTERS

A switched capacitor high pass filter is shown in Figure 1. This circuit uses two capacitors C_1 and C_2 and two switches, MOS transistors S_1 and S_2 operated by nonoverlapping clocks, ϕ_1 and ϕ_2, such that the switches are never closed at the same time.

The combination of S_1, S_2 and C_2 form a switched resistor with an equivalent resistance.

$$R_e = T/C_2 \tag{1}$$

where T is the period for a complete cycle. The filter is thus seen to be a first order series RC filter with a break frequency

$$\omega_o = \frac{1}{R_e C_1} = \frac{C_2}{C_1}\frac{1}{T} \tag{2}$$

This is actually a sampled data filter, which is described by the difference equation

$$V_1 (i) - V_1 (i-1) = V_2 (i) \left[1 + \frac{C_2}{C_1} \right] - V_2 (i-1)$$

which has a Z transform transfer function

$$H (Z) = a \frac{Z-1}{Z-a} \tag{4}$$

where

$$a = \frac{C_1}{C_1 + C_2}$$

This has a frequency response with a magnitude

$$|H (j\omega)| = a \sqrt{\frac{2 (1-\cos \omega T)}{1-2a \cos \omega T + a^2}} \tag{5}$$

For small ωT this is approximately

$$|H (j\omega)| \approx K \frac{\omega}{\sqrt{\omega^2 + \omega_o^2}} \tag{6}$$

which is the form of a single pole RC high pass filter.

The filter of Figure 1 will exhibit excellent dc rejection, since a capacitor with low leakage appears in series with the signal path. It will have a frequency response which depends only on the clock frequency and the ratio of capacitors C_1 and C_2, and should have good dynamic range; the kTC noise on C_2, assuming a 0.1 pf capacitor at 77^o K, will be approximately 100 uV which is 80 dB below a 1V peak signal level.

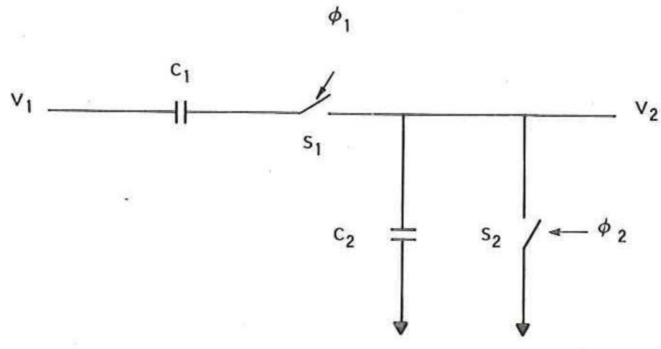

Figure 1. Switched Capacitor High Pass Filter

Its major disadvantage is in the pattern noise which may be generated when a number of such filters are multiplexed together. Each switch S_2 will produce a different output offset due to small differences in gate charge which are a function of threshold voltages and the drive levels used to address the filters.

A CCD technique has been developed similar in operation to these switched capacitor filters, but which overcomes this disadvantage.

CCD MULTIPLEXED HIGH PASS FILTER

The CCD structure, shown in Figure 2, implements a number of separate high pass filters coupled into a parallel load CCD shift register. Each section contains a switched capacitor filter as described in the previous section and has a transfer function given by

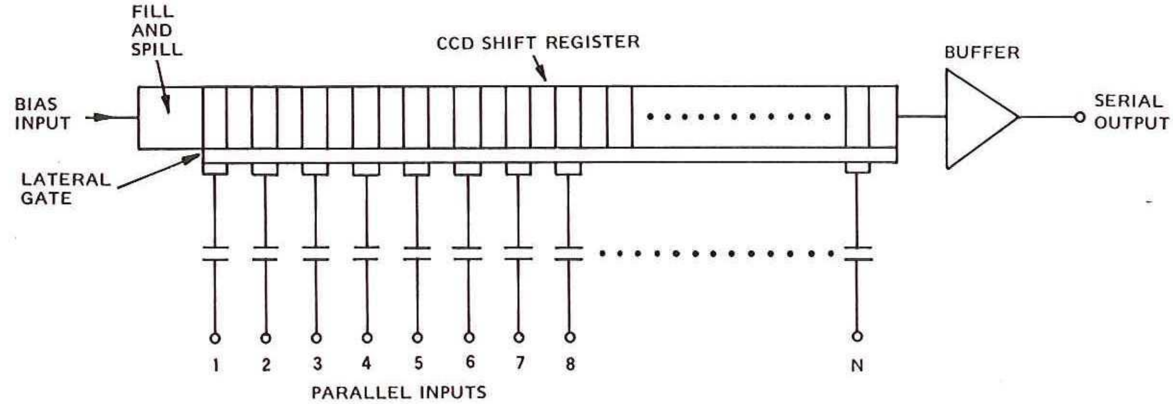

Figure 2. CCD Multiplexed High Pass Filter

Eqn. 4. This structure is similar to the charge transfer accumulator[1] with the exception that the inputs are to one end of the storage capacitor and a fixed bias charge is serially clocked into the CCD register. A multiplexing operation is performed by the parallel in, serial out operation of the CCD.

The CCD structure of Figure 2 may be related directly to the circuit in Figure 1. The capacitor C_1 is repeated N times coupling between each input and the respective stage of the CCD. The switch S_1 is formed by the lateral transfer gate, the capacitor C_2 by the CCD gate over the thin channel oxide and the reset switch S_2 by clocking a fixed quantity of bias charge into all CCD storage locations during each cycle.

After the lateral switch is operated, the filtered samples for each filter are stored in the CCD. As new bias charge is clocked in, these samples are clocked to the output where they are sensed by one of the commonly used charge sensing techniques.

The high pass multiplexed CCD structure offers several advantages over other techniques. The primary advantage lies in the fact that the zero in the transfer function is inherent in the capacitive coupling at the input of the structure. Thus, the dc rejection is limited only by the signal dependent leakage currents through the input capacitor.

The second advantage is the low pattern noise achieved with this structure. Since one input structure makes each packet of bias charge for each parallel input, and since for a constant input on each parallel channel no charge will be shifted laterally in the steady state, each charge packet delivered to the output will be equal, and independent of the threshold voltages at each stage. The only source of pattern noise is nonuniform leakage currents in each site, and this should be extremely small at cryogenic temperatures.

A third advantage is that the frequency response is determined only by the ratio of the input and CCD capacitors, and by the clock frequency. Since the capacitor ratio is determined by the ratio of two areas, the frequency response may be accurately predicted and controlled.

The parallel inputs are simultaneously sampled when the parallel transfer gate operates. This is particularly advantageous in any application such as a parallel channel infrared system with CCD processing preceding the filter, since the filter input signals exist only for a fraction of a clock cycle.

The kTC noise from the input fill and spill circuit generating the bias charge will be reduced by the filter, since for this signal path the CCD with the lateral wells is a low pass filter with a low cut-off frequency relative to the clock. For example, for a filter cut on frequency of 1/180 of the data rate, the bias kTC noise will be reduced by 17 dB. Transfer noise generated as the bias charge packet is clocked to its filter site will also be reduced by the low pass filter. As the filtered output charge packet is clocked to the output, transfer noise will be generated. This will make the total transfer noise greater for the filter channel requiring the most transfers to the output.

FILTER IMPLEMENTATION

The multiplexed high pass filter was implemented in a p-channel technology as part of a focal plane signal processor chip designed to interface with four 32 element I_nS_b linear CID imagers. The chip is mounted adjacent to the CIDs and is cooled to 77° K.

Figure 3 shows a block diagram of the Preamplifier-Filter Multiplexer (PFM) chip, and a photograph of the device is shown in Figure 4. The preamplifiers raise the peak signal level to 1 volt. During each complete read cycle, each of the four inputs processes 32 sequential data samples. Each 32 stage demultiplexer CCD performs a "corner-turning" operation, to simultaneously place each of the 32 samples on separate output lines, for a total of 128 simultaneous samples on the chip. The demultiplexer CCD uses a diffusion tap lateral readout, and relies on the CCD clocking to reset each of the output diffusions.

Each output from the demultiplexers is buffered in a separate source follower to drive the filter/mux inputs. These source followers are gated on only during one of the 32 cycles in order to minimize power dissipation in the dewar: the 128 buffers dissipate 0.8 milliwatt.

The 128 separate signals which represent the outputs from each of the 128 detector sites are applied to separate inputs of the filter/mux structure described in the previous section. Each of the input capacitors is 5.3 pF, operating against the effective CCD gate capacitance of 0.19pF, which gives a break frequency which is 1/180 of the detector sample rate.

The output parallel to serial CCD operates at a clock rate of 1.7 MHz which is 4 times the input clock rate. Blank stages are provided to allow for correction of the 4 to 1 fixed clock interference pattern at the output due to the lower frequency input clocks.

The measured performance of the PFM chip excluding the preamplifiers is given in Table I. These data were measured with the device clocked

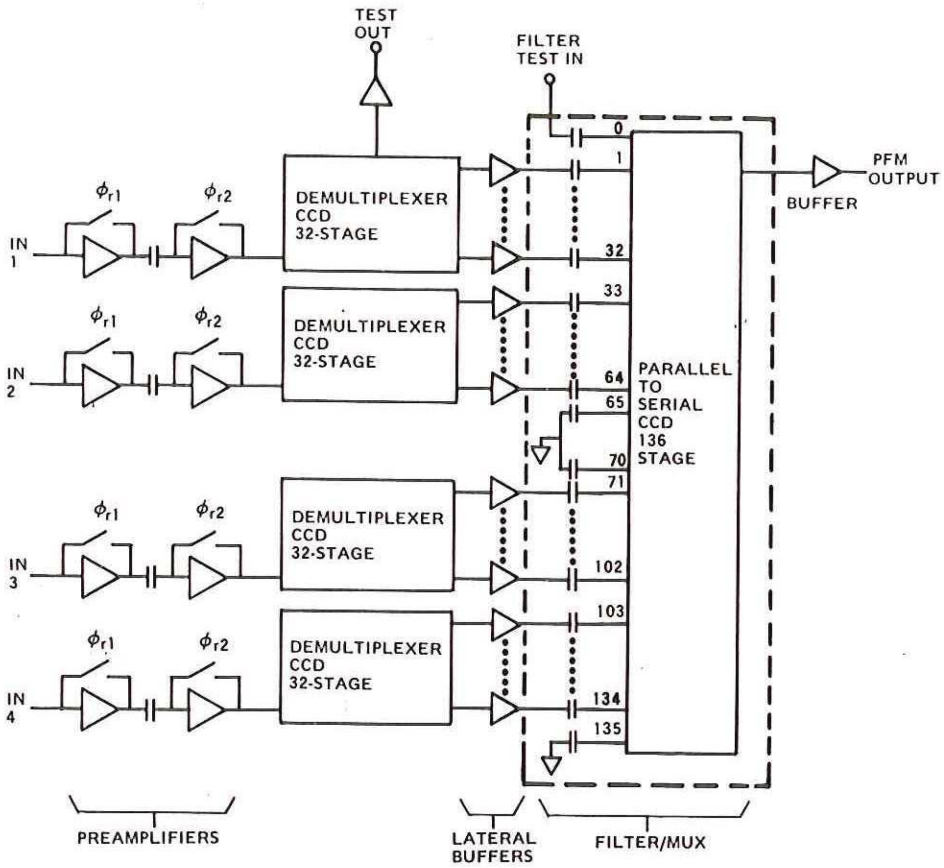

Figure 3. PFM Block Diagram

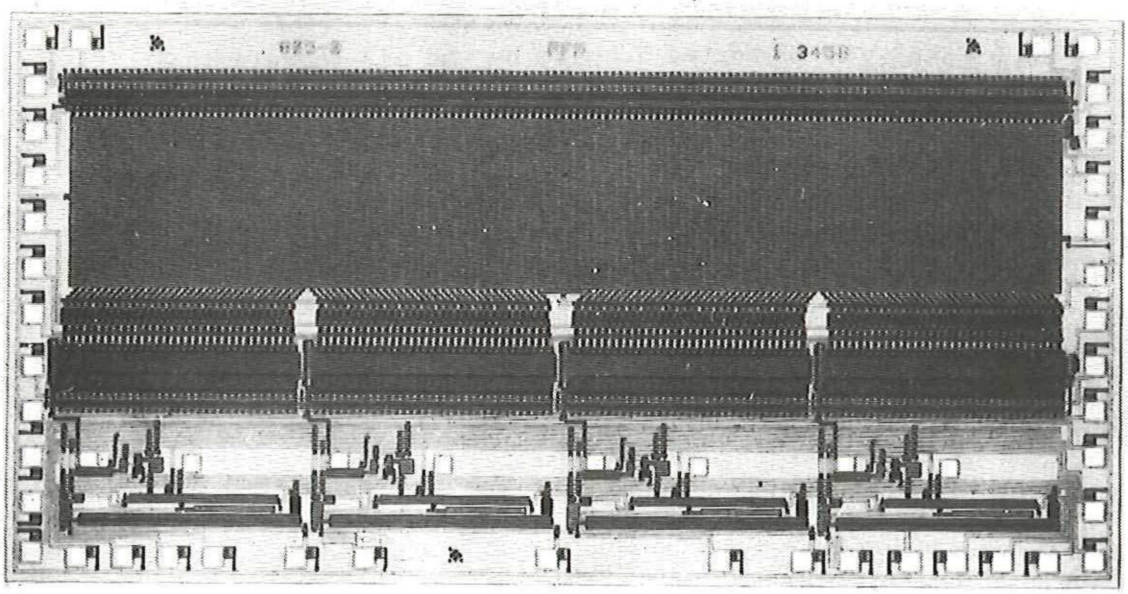

Figure 4. PFM Die

at 1.7 MHz at 77° K. The dc rejection could only be measured to 73 dB due to the measurement technique used. The pattern noise included a 1 out of 4 clock interference. With this regular pattern removed, the remaining fixed pattern noise had a peak-to-peak level which was 60 dB below peak-to-peak signal level. The break frequencies were well matched, consistently being within 10% of the design nominal value both on a chip and between chips.

TABLE I. MEASURED PERFORMANCE OF PFM EXCLUDING THE PREAMPLIFIERS AT 77° K

	REQUIRED	MEASURED
DC Rejection	>70 dB	>73 dB
Pattern Noise	-60 dB	<-60 dB
Cut-On Frequency	70 ± 60 Hz	70 ± 60 Hz
Dynamic Range	>60 dB	68 dB (136 STAGE)
		71 dB (64 STAGE)

The predominant source of noise in the filter structure is transfer noise in the output shift register. For the filter stages requiring the most transfers to the output (up to 136 stages), this limits the dynamic range to approximately 68 dB. For inputs near the center of the CCD the dynamic range is approximately 71 dB.

CONCLUSIONS

A technique for implementing a bank of high pass filters in a CCD technology has been demonstrated. The filter bank exhibits the essential characteristics of excellent dc rejection, well controlled low break frequencies and low fixed pattern noise required by advanced infrared systems.

ACKNOWLEDGEMENTS

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Reference

[1] A Charge Transfer Recursive Filter
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H. S. Goldberg. ISCC77 page 154.