A 1024-CELL CTD SHIFT REGISTER CAPABLE OF DIGITAL OPERATION AT 50 MHz*

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ABSTRACT. We have recently designed and fabricated a 1024-cell CTD shift register that was successfully tested at 50 MHz. This is a peristaltic buried channel device that utilizes a dual channel 2 x 512 cell approach in which the channels are offset by 180°or two gates in the four gate/cell configuration. The offset provides automatic input and output multiplexing to allow 25 MHz operation in each channel while maintaining a 50 MHz total data rate. The individual cell has a 20 x 65 μm geometry designed to store 6 x 10^5 electrons and to transfer the charge at up to 100 MHz rates.

The four-phase clock voltages are provided by a tuned circuit with a Q of 10 that lowers the driver power from 4 mW/bit to 0.4 mW/bit. A correlated sampling circuit eliminates the clock interference and the charge transfer inefficiency (CTI) effects as well as amplifying the signal. The complete off-chip driver circuit also provides the input sampling and output reset pulses.

From the output signal test data, we determine a total CTI around 15% or a CTI/gate = 7 x 10^{-5}. The signal voltage is about 0.12 volts and the rms noise voltage is about 1 mV, yielding a signal/noise ratio of 120. This number combined with the total CTI suggests a bit error rate less than 10^{-100} in binary operation.

INTRODUCTION

The goal of this project was the development of a family of digital delay line devices suitable for use in a pipeline fast fourier transform convolution processor. Here we will describe the most elaborate device in this family, namely a 1024-cell CTD capable of 50-100 MHz continuous operation. The device is driven by an external driver with an output processor that eliminates the clock and reset signals picked up at the output and makes the output signal ECL logic compatible.

DEVICE DESIGN

The cross-section of a typical high speed silicon CTD fabricated at Rockwell is shown in Figure 1. This is the profiled peristaltic buried channel structure [1] that combines some of the charge storage advantage of the surface channel design with the transfer speed and efficiency of buried channels. The gate configuration is four-phase as shown with a two-level overlapping polysilicon structure. The bus lines feeding the gate arrays must be overlaid with aluminum, however, to ensure low RC charging time constants.

In this device, the charge is stored in the more heavily doped ion implant layer near the surface where it is most sensitive to the clocking voltages applied to the input and transfer gates. The completion of charge transfer from gate to gate, however,

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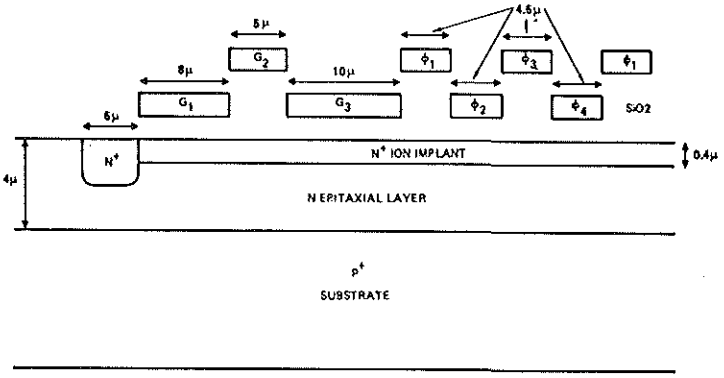

Figure 1. PCCD Input Configuration

takes place in the epitaxial layer well removed from the surface. This transfer region provides a high mobility layer free from trapping surface states where transfer-aiding fringing fields are near their peak. The so-called peristalsis analogy is apt because, during transfer, the charge is squeezed by the strong vertical field against the reverse biased junction at the N epilayer/P substrate boundary where the transverse fields are strong. Since the volume under the adjacent gate is a nearly empty potential well for electrons, the charge naturally flows into it.

Figure 2 contains a theoretical family of curves for the normalized transverse electric field versus distance below the gate at the gate center where the field drops to a minimum from the gate edges. This data comes from a solution of Laplace's equation (i.e. no mobile charge, fixed ionic charge treated by superposition) so it is most accurate for the transfer of the last increment of charge. This is the main point of interest for good transfer efficiency anyway, so this simple analysis has considerable relevance.

A gate width that is easily obtainable with the present projection alignment photolithography systems and can give some yield in a 1024-cell device is 4.5 μm. This produces a cell width, W, of 18 μm. The figure indicates that a typical epitaxial layer that is 4 μm deep (i.e. X_o = 0.22W) can give a peak electric field that is about 75% of the potential maximum field (∿V/W) at the gate

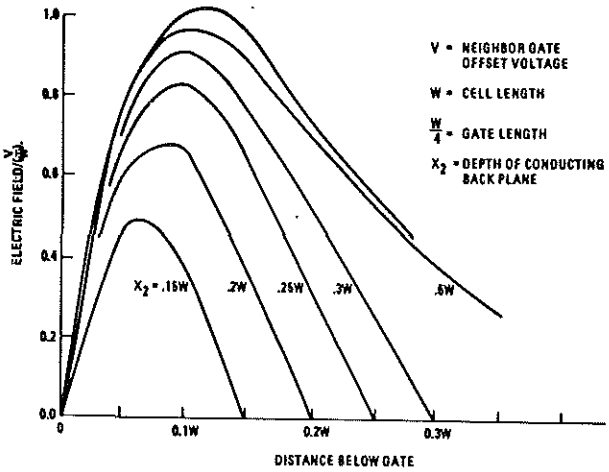

Figure 2. Normalized Transverse Electric Field at Center of Gate Electrode Operating in Four-Phase for Buried Channel CTD with Conducting Back Plane

center. V is the neighbor gate offset voltage. This peak field occurs about 0.1W or 1.8 μm below the gate, which happens to be the region in the epitaxial layer between the surface and junction depletion layer to which the charge is squeezed.

If we assume that V = 10v and V/W = 5.6 x 10^3 v/cm, a reasonable value for the field might be half this or 2.8 x 10^3 v/cm. At this field strength, the velocity of electrons in silicon is about 4 x 10^6 cm/s, so that the transit time across an 18 μm

cell is 0.45 ns. This suggests permissable clock rates approaching 1 GHz, but certainly 50-100 MHz is easily achieved with the 4.5 μm gate dimension. In fact, we have demonstrated the practicality of 1 GHz transfer rates in similar structures [2].

Figure 3 contains some calculations [3] of charge storage capacity versus the implantation dose in the profiled layer. This is a one-dimensional solution of Poisson's equation assuming two regions of constant doping density. The requirement for ECL logic compatibility gives an input voltage on the order of one volt. On the other hand, we must be able to saturate the charge capacity with an applied clocking gate voltage of around 10V. This will insure that the CTD channel can be pinched off to isolate the charge packets. From the figure, there is an allowable dose range of 0.75×10^{12} - 1.75×10^{12} cm^{-2} which satisfies these two conditions, so a design goal of 1.25×10^{12} cm^{-2} seems appropriate.

The calculations indicate that the storage capacity is fairly insensitive to substrate doping and epitaxial layer thickness and also to epitaxial layer doping in the 10^{15} cm^{-3} range. At a fixed voltage swing, the charge capacity decreases with increasing implant layer thickness, but not drastically so until the thickness approaches three times the minimum oxide thickness. That is the point where the oxide capacitance equals the pinched off semiconductor depletion capacitance. We want to get the charge as far away from the surface as possible for transfer efficiency, so an implant depth approaching 0.45 μm (i.e. 3 times the 0.15 μm typical oxide thickness) is a good choice. For a 1 volt input, this will give a charge capacity of about 10^{11} cm^{-2}, if the signal is slightly DC biased. An input storage gate 10 μm long x 65 μm wide will then provide about 6.0×10^5 electrons per charge packet, which will give adequate signal strength. In transfer, the charge is stored in effective storage lengths of $2 \times 4.5/\sqrt{2} = 6.4$ μm when using four-phase sinusoidal clock drives, but the factor of 1.5 decrease from the input storage gate length is easily made up by the increased clock voltage swing (~10V) in the transfer gates.

The input and clocking gate structure is shown in the cross-sectional view of Figure 1. The dimensions shown are the result of the charge transfer and storage

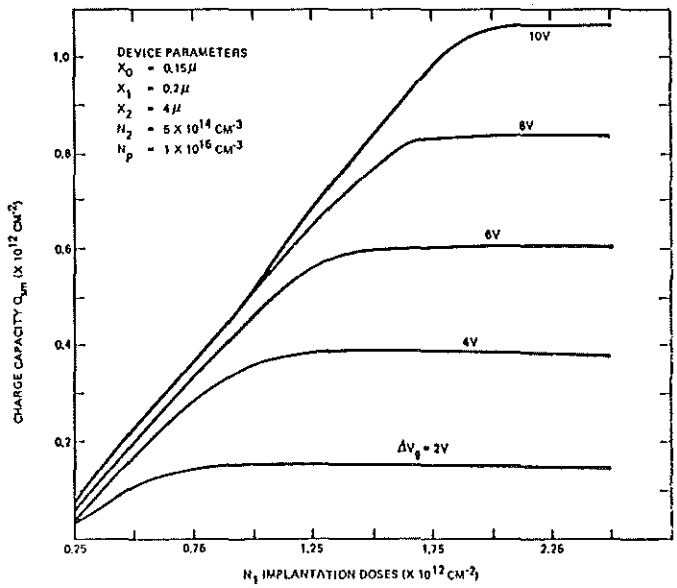

Figure 3. Charge Capacity Q_{sm} as a Function of N_1 Layer Implant Doses for Different Gate Voltage Swing ΔV_g; X_o = Oxide Thickness, X_1 = Implant Thickness, X_2 = Channel Thickness, N_2 = Channel Doping, N_p = Substrate Doping.

capacity analyses we have done. The input consists of three gates: G_1 is used optionally to provide additional isolation or gating of the N+ diffusion charge source; G_2 is a metering gate used as a backflow gate or a chopper gate; G_3 is the input charge storage gate.

The three available input techniques are shown in Figure 4. The first of these in Figure 4(a) is the very simple pulsed diffusion method whereby a signal raising the N+ source potential injects charge directly into the first transfer gate. The input gates are biased to turn on the channel. This method is simple to operate but does not provide a well-defined charge packet or sample aperture. The second input technique in Figure 4(b) is the fill-and-spill or charge equilibration method. Here the input signal is applied to either G_2 or G_3 while the other input gates are fixed. The charge source is pulsed to a high potential (1) to fill the G_3 storage gate region with mobile charge. At this time, ϕ_1 is also at a high potential to help define the G_3 potential well. Then the source potential is dropped (2) and the excess charge under G_3 diffuses back over the G_2 backflow gate (3) to form a well-defined charge packet under G_3. The first transfer gate is then clocked to its low potential (4) to allow the charge packet to transfer into the CTD (5). This technique is widely used for its low noise and good linearity [4]. Because the charge packet is allowed to thermally equilibrate, input noise sources other than kTC noise are removed. These include shot noise associated with the input charge injection. However, the equilibration time required for the thermal diffusion of the excess carriers is obtained from the continuity equation to be $\tau_{th} = 4L^2/\pi^2 D_n$. For a diffusion coefficient $D_n = 25\ cm^2/s$ and L (i.e. the width of G_2 and G_3) = 15 μm, we get τ_{th} = 36 ns. This is too long for frequencies in excess of about 5 MHz, since equilibration can only take place during the half cycle when the ϕ_1 potential is high, and we need at least $3\tau_{th}$ for good equilibration.

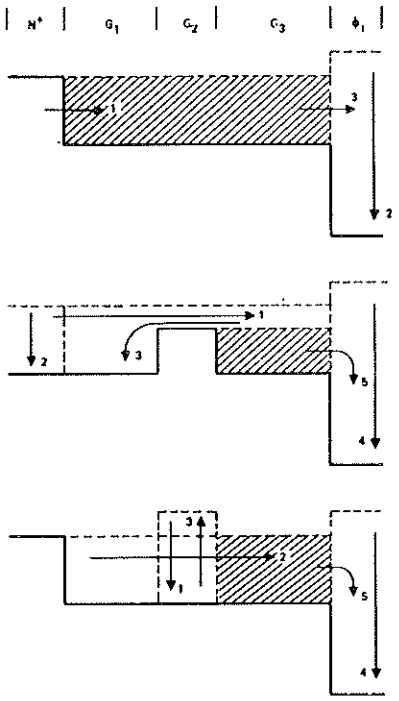

Figure 4. Input Modes
(a) Pulsed Diffusion
(b) Charge Equilibration (Fill-and-Spill)
(c) Charge Partition

The input technique of choice is the charge partition method shown in Figure 4(c), in which the chopper gate, G_2, is used to isolate the charge source from the CTD while the charge packet is being loaded. The input signal is applied to either the source diffusion or the G_3 storage gate. When the chopper gate potential is periodically pulsed low (1) (while the ϕ_1 potential is high), charge flows into the region under the storage gate (2). The amount of charge is determined by the difference in potential between the diffusion and the storage region and is continuously tracking the input. Sampling occurs when the chopper gate potential is pulsed high (3) to isolate the charge packet just before the ϕ_1 potential clocks low (4) and the charge packet transfers into the CTD (5). The input shot noise is not fully equilibrated as it is in the charge equilibration input, but, as we will see later, this is not a

significant problem. The sample aperture is particularly small in this input technique and is determined by the rise time of the chopper pulse.

The speed of the charge partition input is very high, being determined by the field-aided injection time of the charge across G_1 and G_2. An experiment to determine this time is described in Figure 5 using a similar device. In the experiment, the CTD was clocked at a slow rate, and the injection time was controlled by a well-defined diffusion source pulse width. In the first example, a potential well was formed under the ϕ_1 and ϕ_2 gates during the quarter cycle when they are both at low potential. The pulse was applied during this interval to inject charge over the 30 μm barrier and fill the well. Any excess injected charge has time to flow back to the source after the pulse relaxes just as in a normal fill-and-spill. The relationship between the amount of charge in the well and the pulse width indicates the injection time required. In this case, the well saturates in about 21 ns.

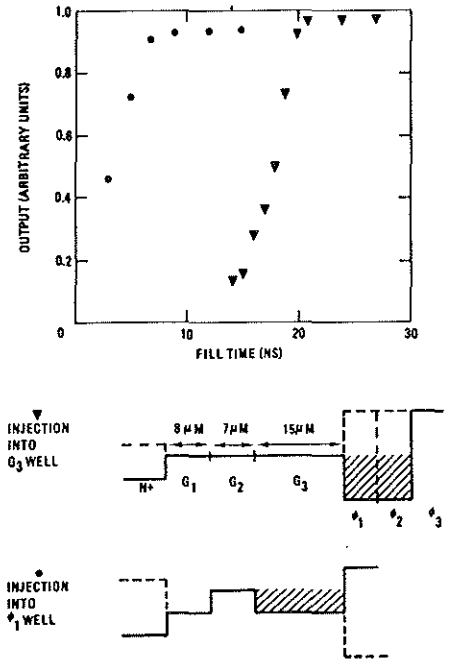

Figure 5. Input Charge Injection Time Experiment

In the second example, the well is formed under gate G_3 while the ϕ_1 potential is high. The charge is then injected 15 μm over the barrier and into the well. The injection time for the 15 μm injection distance is about 9 ns. In the design of Figure 1, the 13 μm injection distance under gates G_1 and G_2 suggests an injection time less than 9 ns from an extrapolation of the above results. This is within the 10 ns half-cycle window available in an input to be run at 50 MHz or below. Higher frequency operation can be achieved by narrowing or eliminating the G_1 gate which is usually only an optional addition.

The long, single channel CTD structure presents many problems, especially at high speed. The first of these is a long aspect ratio which would be about 280 for the active region 65 μm wide and 4.5 x 4 x 1024 = 18432 μm long. Even with the 5 mil bonding pads, scribe lines and bus lines all located on the short dimension, the chip aspect ratio would be about 40. Also the long dimension would be nearly 2 cm which is too long for routine step-and-repeat mask making. Serpentine structures used to alleviate this problem at low frequencies do not work well at high frequencies due to poor transfer at the corners. Another problem related to the length is the amount of bulk state trapping that occurs due to the large number of bulk impurities seen by a charge packet in its long journey down the channel. This trapping is the most important source of transfer inefficiency at frequencies below 100 MHz in these devices, and it also contributes significantly to the system noise.

A technique for reducing channel length by going to a dual channel arrangement is shown in Figure 6. The two channels employ overlapping gates to maintain matched characteristics and to minimize capacitance from additional gate clock bus lines. The key to efficient operation, however is the 180° (two gates) offset at the input and output that provides automatic multiplexing of the signal. Figure 6 concentrates on the input structure showing the common input to the two source diffusions. The G_3 and G_1 gates are also common to both channels, so only the G_2 chopper gates are separate. By operating the chopper gates 180° offset from each other in synchronization with the automatic offset of the first transfer

gates, alternate charge partition input sampling occurs.

The dual channel approach decreases the active region aspect ratio a factor of four and cuts the channel length in half. This also reduces by one-half the dominant bulk trap transfer inefficiency and the trapping noise. Because of the input and output multiplexing, the transfer frequency of the CTD is halved to maintain the data rate and time delay. This proportionately reduces the wideband power consumption in the circuits needed to drive the transfer gate capacitances.

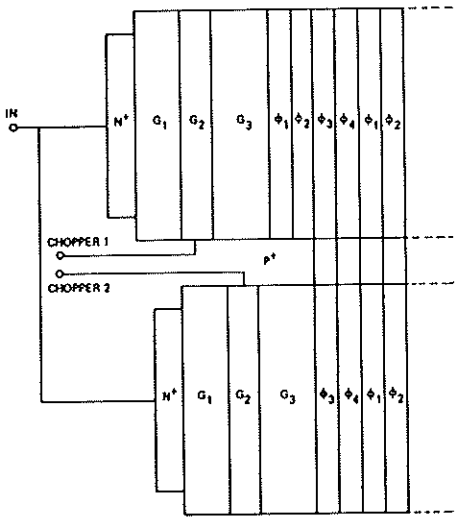

Figure 6. Self-Multiplexing Dual Channel Charge Partition Input

The output circuit used in this device is shown in Figure 7. It is an FET source follower with reset arrangement designed to drive a small capacitive load at the 25-50 MHz frequency required for each of the dual channel outputs. The inset in the figure illustrates the source follower FET which has a serpentine structure to provide a large gate width (~200 μm) with a short gate length (5 μm) in a limited chip area. This will give a large transconductance, g_m, with a high rolloff frequency, ω_o. After the CTD charge has been transferred to the output FET gate and the final transfer gate is at its high electron potential, the reset FET is turned on by applying a positive pulse to the reset gate. This drains the charge off the output FET gate to the reset drain. Because of the channel offset the two channel outputs operate 180° out of phase with different final transfer gates, and the two outputs can be recombined off chip.

A simple gain calculation indicates the adequacy of this design. The AC source current of a MOSFET is given by $V_g g_m$, where V_g is the gate signal. The gate signal on the output FET is Q/C_{g1}, where Q is the CTD charge output and C_{g1} is the output FET gate capacitance plus a small stray capacitance. The reset FET is turned off when the charge is transferred onto the output gate, so it presents a very large impedance. Combining these results, the output FET source current is Qg_{m1}/C_{g1} and the source follower FET gate signal is $Qg_{m1}/\omega C_{g1}C_{g2}$. C_{g2} is the source follower FET gate capacitance plus a small stray capacitance, and the assumption here is that the bias FET offers a small AC load by comparison. The output current can now be written as $Qg_{m1}g_{m2}/\omega C_{g1}C_{g2}$ and the output voltage is $Qg_{m1}g_{m2}/\omega^2 C_{g1}C_{g2}C_L$, where C_L is the output capacitive load. This analysis is accurate for this two stage source follower amplifier if the voltage gain at each stage is less than one as it is assumed to be here. Although we have sufficient voltage generated by Q on C_{g1}, we have difficulty obtaining enough current to drive the output load capacitances at these frequencies.

Typically, the transconductance has a corner frequency or 6 db point where it begins to roll off at $f_o \approx 5$ MHz. Above this frequency, we can expect to have $g_m \cong g_{mo}\ \omega_o/\omega$, where g_{mo} is the low frequency transconductance. Now the output voltage becomes $Qg_{mo1}g_{mo2}\omega_o^2/\omega^4 C_{g1}C_{g2}C_L$ and we see that the ω^4 factor can quickly make the higher frequencies prohibitive. Table 1 lists the anticipated numerical values of the constant factors based on our calculations and experience with similar devices. The predicted output voltage at 25 MHz per channel into a 5 pF load is 0.15 volts.

A photograph of the fabricated device is shown in Figure 8. It has 29 bonding pads, but requires only a 22-pin package, since

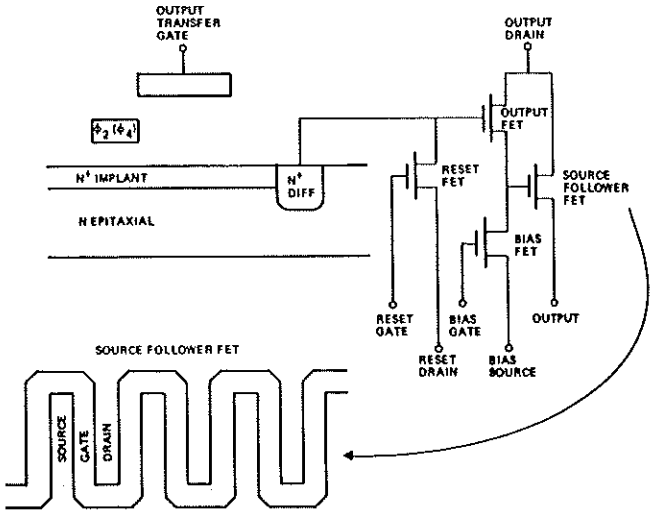

Figure 7. FET Source Follower with Reset Output Circuit Showing Long Channel FET Source Follower Structure

some of the pins are bonded to two pads, each at opposite ends of the long device. This is required to minimize long bus lines and their associated RC time constants. Even so, aluminum must be deposited on the transfer gate polysilicon bus lines and on certain input and output lines to insure low resistance. The individual gates themselves, however, do not suffer from charging time limitations for frequencies less than 1 GHz. In the figure, the input is at left and the output is at the right.

Table 1. Output Transistor Parameters

g_{mo1} = 0.2 mmhos	f = 25 MHz
g_{mo2} = 1.0 mmhos	C_{g1} = 0.1 pF
Q = 10^{-13} Coulombs	C_{g2} = 0.5 pF
f_o = 5 MHz	C_L = 5 pF

DRIVER CIRCUITRY

The fundamental power requirement of the CTD is the power required to propel the charge packets down the CTD channel and make up their scattering losses. In buried channels, this real power is approximated by I^2R, where R is the channel resistance and I is the average CTD charge packet current, Qf. Even though the power is proportional to f^2, it is still less than 1 mW in the 1000-cell device operating at 100 MHz. In practice, however, the main power loss is due to the reactive power given by $P = (C_G + C_{DL})V^2f$ required to drive the gate and drive-line capacitances, C_G and C_{DL}. V is the voltage swing and f again is the clock frequency. In a wideband driver, this power must be dissipated in the driver amplifiers. If the cell gate area is 65 μm x 20 μm = 1.3 x 10^{-5} cm^2, then C_G is about 0.2 pF/cell or about 200 pF in a 1000-cell device with gate oxides averaging around 2000Å. The bonding pads and drive-lines will add another 10 pF or so. For V=10 volts and f=100 MHz, the power requirement is about 2 watts, or 2 milliwatts per bit. If a 2 x 512 cell device is used, the driving frequency is halved and the power reduces to 1 watt or 1 milliwatt per bit.

If the CTD is to be operated in a continuous high speed mode at a single frequency, it is possible to utilize an inductor to resonate the gate capacitance and thereby reduce the power dissipation by an amount equal to the Q of the resonant circuit. A block diagram showing the resonant circuit driver is given in Figure 9, and the accompanying timing diagram is in Figure 10. The clock input is first shaped into a square wave by a differential amplifier and Schmitt trigger to

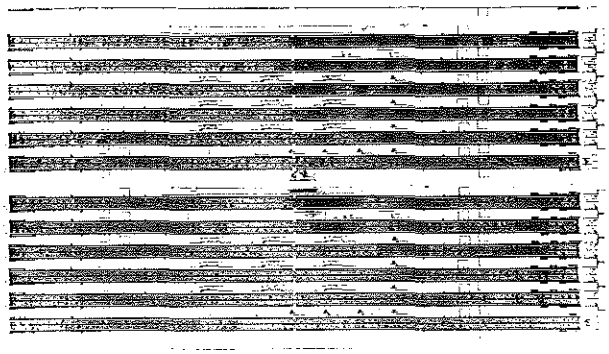

Figure 8. Rockwell 30309 1024-Bit 50 MHz Continuous CTD Shift Register. Each Chip Contains 6 Devices.

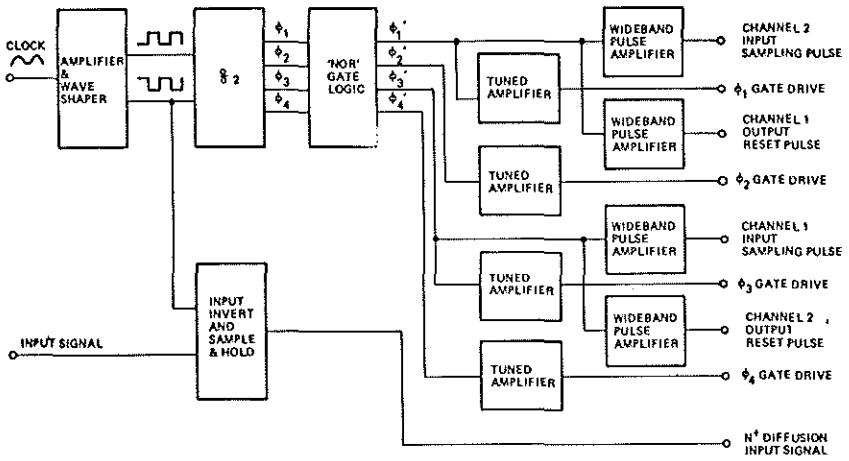

Figure 9. Block Diagram of CTD Test Circuitry Using Tuned Gate Drive Amplifiers

permit a wide variety of driver input waveforms. The final amplifier in this series provides complementary outputs of the shaped and buffered square wave. These two square waves are then fed into a dual flip-flop divide-by-two circuit that gives four outputs at half the original frequency offset from each other by 90° phase shifts. The first two of these clock phases, ϕ_1 and ϕ_2, are shown in the timing diagram. In the next step, the four-phase square wave signals are gated through four "nor" gates to obtain the logical outputs denoted as ϕ_1'-ϕ_4' in the timing diagram. These are pulse trains in a four-phased array, and they are used to drive the transfer gate voltage amplifiers and the input chopper gate and reset FET gate amplifiers.

The circuit diagram for one of the four channel gate amplifiers is shown in Figure 11. As stated earlier, it is designed to drive a tuned load consisting of an inductor, the CTD gate capacitance and a variable tuning capacitor. The output is a sine wave, as shown in the timing diagram, that peaks at the same time as the input pulse. This is accomplished by inverting the signal twice, once in a digital inverter and then again in the single transistor amplifier. The once-inverted pulse input to the PNP transistor turns it on when the CTD drive signal is near its peak. This means that the voltage across the transistor and, thus, its power dissipation is small and this tends to keep the Q

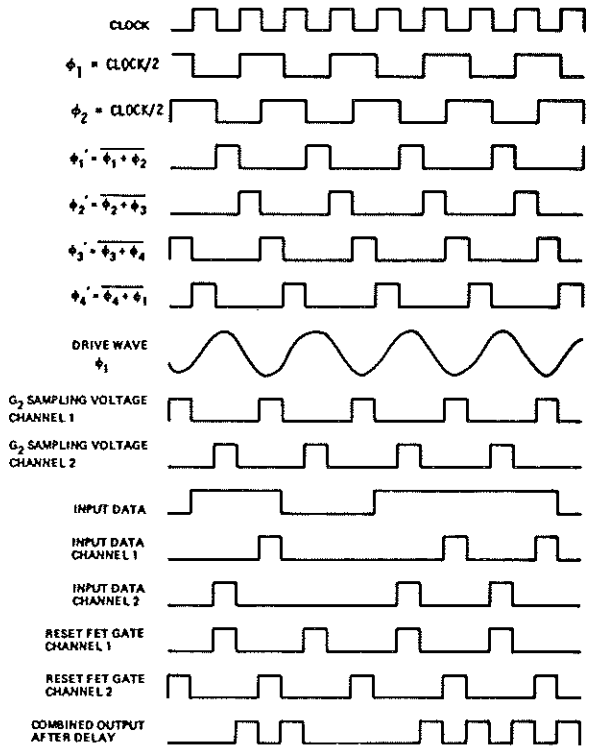

Figure 10. Timing Diagram for CTD Test Circuitry Using Tuned Gate Drive Amplifiers

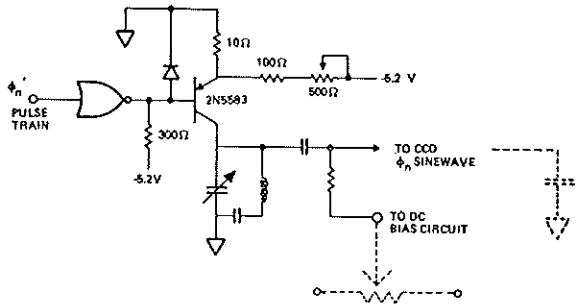

Figure 11. Tuned CTD Channel Gate Drive Amplifier

of the circuit high. The pulsed transistor output into the resonating load is analogous to punching a damped oscillating spring at appropriate intervals to maintain oscillation. The transistor supplies the power required to compensate for the finite circuit Q. In practice, the Q of the tuned load is about 20 and the Q of the entire circuit is around 10. This reduces the power consumption of the CTD channel gate drive by a factor of 10 from 1 watt (2 x 512 cells) to 0.1 watts and from 1 milliwatt per bit to 100 microwatts per bit. The driver clock voltage is around 20 volts peak-peak.

The inputs to the channel gate drivers are also used in the output reset gate and input control gate driver circuits. No attempt has been made to tune these circuits, however, because the load capacitances are so small. These circuits are just simple inverters cascaded into one transistor amplifiers. The sampling voltages applied to the two input control gates and the voltages applied to the two output reset FET gates in a dual-channel device are shown in the timing diagram. Notice that the channel one input sampling pulse train and the channel two output reset pulse train are identical to the ϕ_3' channel gate pulse train. Also, the channel two input sampling pulse and the channel one output reset pulse are the

same as the ϕ_1' channel gate pulse. The reset and sampling voltage pulses are about 4 volts in amplitude. The signal input to the system is also buffered by an input amplifier and processed through a flip-flop so that the input to the CTD changes only between sampling intervals. This is just a simple sample-and-hold operation and is depicted in the timing diagram in terms of an example. Finally, the outputs from the two channels are combined, resulting in an output pulse to denote a "1" and no pulse for a "0". The output pulses will always, of course, occur between the reset pulses.

The CTD output as it is taken from the on-chip output amplifier will normally have a large amount of clock frequency interference superimposed on it. This is not a random noise effect and so it does not affect the bit error rate. However, it could cause a problem in certain signal processing techniques downstream and it detracts from a potentially clean output signal. Fortunately, it is fairly simple to eliminate this interference using a correlated output sampler such as that shown in Figure 12.

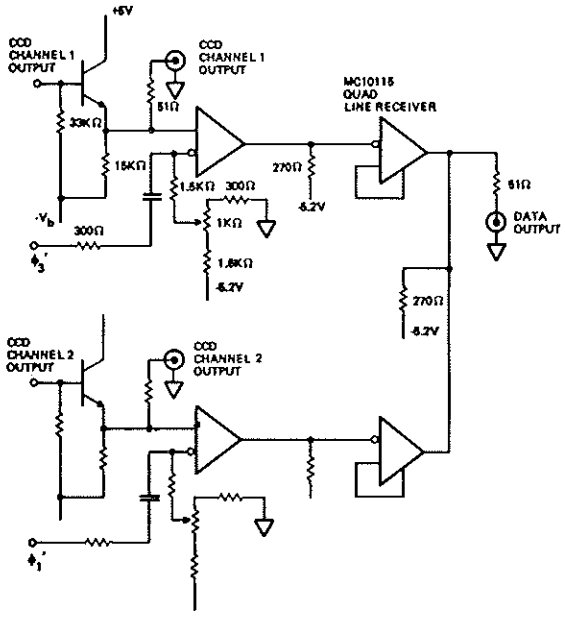

Figure 12. Correlated Sampler and Amplifier Circuit for Output Signal

The CTD output signal is first amplified in a single one-transistor buffer circuit which feeds into a differential amplifier. The other input to the differential amplifier is the ϕ_3' pulse train (ϕ_1' for channel two).

Referring to the timing diagram in Figure 10, we see that the ϕ_3' pulse occurs exactly between the channel one reset pulses when the output signal is at a peak. A DC bias is added to the ϕ_3' sampling pulse and tuned so that the pulse peak occurs halfway between the "0" and the "1" signal output values. The differential amplifier output is always pinned high except when there is a "1" output signal at which point it is pinned low. An inverter reverses the signal so that "1" is high and "0" is low, and the two ECL inverter outputs in the dual channel set-up are shorted into a common load to combine the two outputs into one signal. The timing diagram for this technique is shown in Figure 13. By sampling the output at discrete points where the actual signal pulse exists, the clock interference which is synched to the sampling pulse and occurs at the pulse frequency is equivalent to a constant DC contribution and is simply subtracted out.

OPERATING RESULTS

Figure 14 shows a typical input of a repeated 16-bit word, namely 1100111100000000. The total word length is 320 nanoseconds with a bit length of 20 nanoseconds corresponding to a 50 MHz rate. The logic levels are about 1.2 volts ("1") and 0.3 volts ("0") for standard ECL logic.

After processing by the external input circuit, the signal is inverted and biased negative to be appropriate for application to the input diffusion of the CTD. The corresponding outputs from the two channels are shown in Figure 15. A "1" here is denoted by a negative pulse, and we can see the substantial clock interference superimposed on the signal. The upper trace is the channel one signal and the lower trace is the channel two signal. Figure 16 shows the final output after processing by the external output circuit. The signal has been inverted, the clock interference has been eliminated and the dual-channel output has been combined. Also, the signal size is an ECL compatible 0.8 volts. Finally, Figure 17 contains the input (upper trace) and output (lower trace) of the total system on a compressed time scale of 10 μs/div. Thirty-two (32) words of 16 bits each

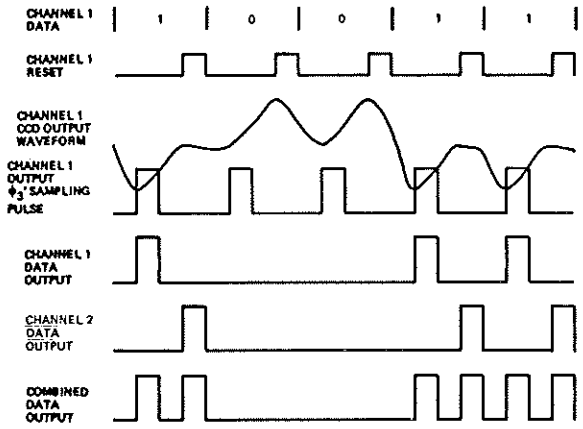

Figure 13. Timing Diagram for Output Signal Processor Circuit

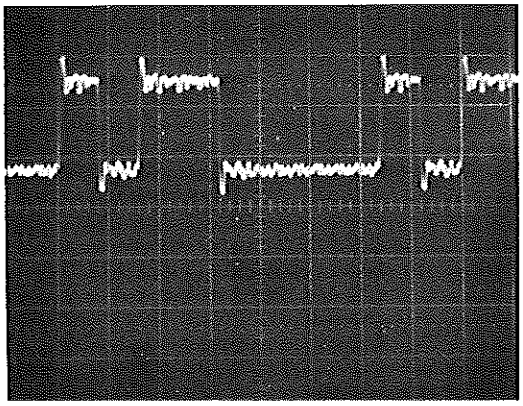

Figure 14. Oscilloscope Photograph of 30309 Device Operation Showing Input Data

Vertical Scale: 0.5V/Div.
Horizontal Scale: 50 ns./Div.
Center Line: 0V

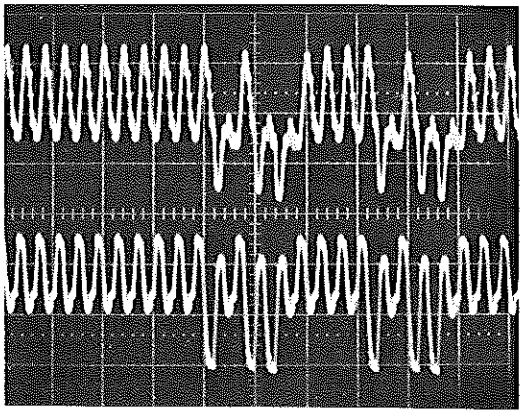

Figure 15. Oscilloscope Photograph of 30309 Device Operation Showing Dual Channel Output Data ("1's" Preceded by a String of "0's").

Vertical Scale: 0.1V/Div.
Horizontal Scale: 100 ns./Div.

separated by 32 completely zero words are used to fill the 1024-bit storage capacity. The input signal is similar to that of Figure 14 which exhibits some high frequency noise. This noise is contained in the deep white bands of Figure 17. The output signal is significantly cleaner, and of course, it is delayed by 20.48 μs or the channel transit time.

The worst case charge transfer inefficiency (CTI) will occur for a "1" or full charge packet preceded by a string of "0's". This charge packet will not pick up any charge left by previous packets to compensate for its own transfer losses, and it must fill bulk states that have been thermally emptying for many periods. Therefore, we can deduce CTI from the waveforms of Figure 15. In channel one, the first "1" following many "0's" is down about 17% from the "1" that follows it. The "1" that follows another "1" should have practically no loss because it picks up the charge loss from the

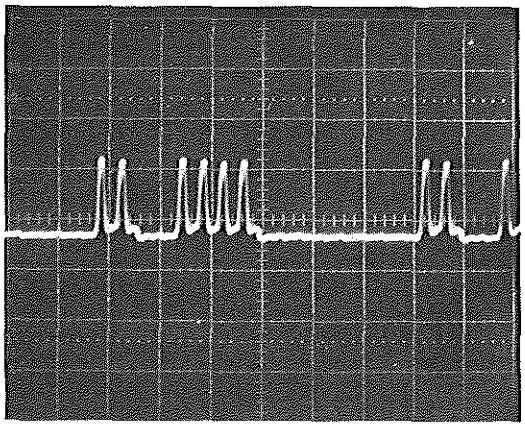

Figure 16. Oscilloscope Photograph of 30309 Device Operation Showing Processed and Combined Output Data from Figure 15.

Vertical Scale: 0.5V/Div.
Horizontal Scale: 50 ns./Div.

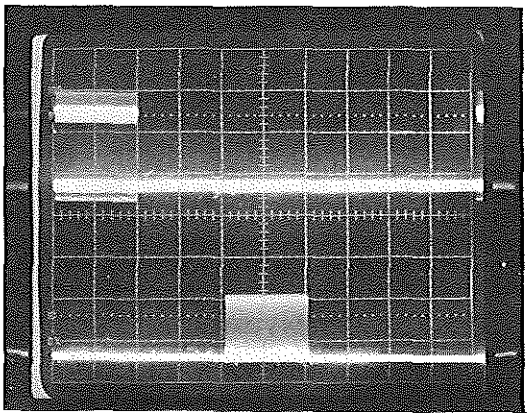

Figure 17. Oscilloscope Photograph of 30309 Device Operation Showing Total Shift Register Input (Upper Trace) and Output (Lower Trace) Data

Vertical Scale: 0.5V/Div.
Horizontal Scale: 10 μs/Div.

preceding "1" to compensate for its own loss and does not have to fill the bulk states. Therefore, we can use it as a reference. If the total transfer inefficiency is ε_T = 0.17, the CTI per cell is $\varepsilon = \varepsilon_T/512 = 3.4 \times 10^{-4}$. In channel two, however, the results are somewhat better, and we get $\varepsilon_T = 0.07$ and $\varepsilon = 1.4 \times 10^{-4}$. This latter number corresponds to a transfer inefficiency at each gate transfer of 3.5×10^{-5}.

The spectral data in Figure 18 was taken at one of the CTD outputs before it was processed by the external output circuit. The input data was a simple square wave of frequency 12.5 MHz, and the output data was run through a spectrum analyzer. The 0 Hz or DC component represents the system offset voltage. The input square wave fundamental and third harmonic give rise to the spikes at 12.5 and 37.5 MHz respectively. The input square wave second and fourth harmonics contribute partially to the frequency components at 25 and 50 MHz, but these are primarily due to the sampling and clock frequency at 25 (fundamental) and 50 (second harmonic) MHz. The magnitude of the 12.5 MHz data output signal is about 0.12 volts as taken from Figure 15, so this becomes the reference for determining voltage values from the spectrum analysis.

The white noise can be determined by examining the flat portion of the spectrum above 25 MHz. In the figure, the noise at high frequency is a constant 74 db below the signal output. The spectrum analyzer bandwidth is 100 KHz, so, if the data signal power is $(0.12 \times 0.12/10^5 =) 1.44 \times 10^{-7}$ V^2/Hz, the noise power is $(1.44 \times 10^{-7}/2.5 \times 10^7 =) 5.8 \times 10^{-15}$ V^2/Hz. Integrating over 50 MHz, the noise power is 2.9×10^{-7} V^2 and the RMS noise voltage is 0.54 mV.

In addition to the white noise, there is substantial 1/f noise at frequencies below 25 MHz. Since this 1/f noise amplitude just about equals the white noise at 25 MHz, in channel one it can be characterized by a noise power voltage of $(5.8 \times 10^{-15} \times 2.5 \times 10^7/f =) 1.45 \times 10^{-7}/f$ V^2/Hz. When this is integrated from 100 KHz to 50 MHz, we get a noise power of 9.0×10^{-7} V^2 or an RMS noise voltage of 0.95 mV. Combining the two noises gives a noise power of 1.19×10^{-6} or an RMS noise voltage of 1.1 mV. This noise plus the 0.17 total transfer inefficiency implies a bit error rate less than 10^{-100} at the 50 MHz combined data rate and 2×10^{-2} at the 100 MHz rate. This drastic change is based on the calculated ω^{-4} drop-off in signal output. For reference, a bit error rate of 10^{-17} implies less than one error per year at the 50 MHz rate.

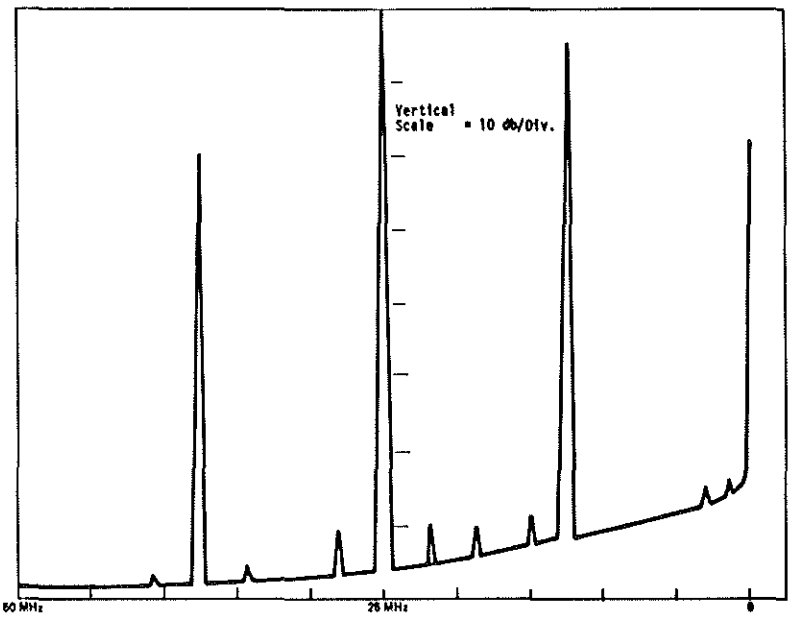

Figure 18. Spectrum Analyzer Characterization of CTD Output Signal

SUMMARY

We have presented design criteria and demonstrated the performance of a 50 MHz, 1024-bit CTD digital shift register. The typical device bit error rate appears negligible at this frequency. Although there is additional speed to permit increasing the frequency in the CTD input and charge transfer sections, the output circuit limits operation to 50-75 MHz. For transient data recorder schemes, where data is input fast, stopped and output slow, this is not a limitation, and we have achieved operation at 340 MHz (i.e. the ECL logic limit) in the laboratory. However, for continuous delay lines such as we have been discussing here, the output circuit speed will need to be improved. This will probably occur through the use of bipolar, V-groove or DMOS technology.

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