SAW/CCD BUFFER MEMORY*

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ABSTRACT

A surface acoustic wave (SAW) piezoelectric delay line has been integrated with a silicon CCD shift register to produce a fast-in, slow-out buffer memory. A prototype device with an input bandwidth of 40 MHz centered around 107 MHz, a maximum input signal duration of 3.5 μs, and an output clock rate of 100 KHz has been fabricated and tested. The SAW/CCD device consists of a lithium niobate ($LiNbO_3$) piezoelectric substrate, which functions as a SAW delay line, in close proximity (typically 300 nm) to an array of 300 sampling fingers connected to a 300-stage CCD on a silicon substrate. The output of the CCD retains both amplitude and phase of the input signal.

INTRODUCTION

New signal-processing capabilities are achievable by integrating a surface acoustic wave (SAW) device with a suitable CCD by coupling the piezoelectric fields associated with the surface wave directly to the charge in the CCD. Such a combination could make use of the advantages and compensate for the limitations of each of the two classes of devices. We report here the first step toward such a class of integrated SAW/CCD devices, a buffer memory device with wide input bandwidth and temporary storage capability. The fast-in, slow-out buffer memory device is shown in Fig. 1. It consists of a CCD shift register with parallel inputs connected to a set of sampling fingers, all on a single silicon substrate. The substrate is pressed against spacer-rails on a piezoelectric crystal with an acoustic delay line on its surface. The rails produce an air gap between the delay line and the CCD sampling fingers.

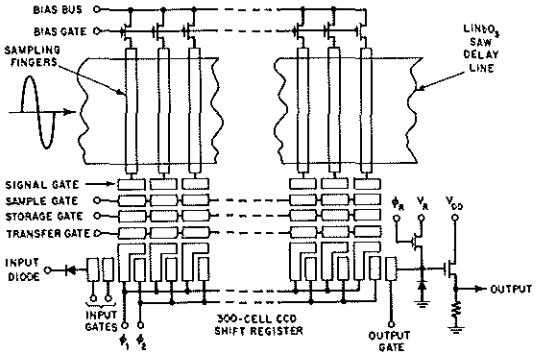

Fig. 1. Schematic diagram of an acoustoelectric SAW/CCD fast-in, slow-out buffer memory.

THEORY OF OPERATION

A schematic diagram of the device is shown in Fig. 1, and the sequence of device operation is as follows. Prior to the application of an input signal, the sampling fingers are pre-charged to the potential of the bias bus by means of the linear array of enhancement-mode MOS transistors. The sampling fingers are allowed to float by opening the bias gate, and a wideband data signal is applied to the input transducer of the SAW delay line. The piezoelectric RF field associated

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with the acoustic wave modulates the potential on each of the sampling fingers and thus modulates the charge in a set of signal wells under the signal gates shown in Fig. 1. Charge is exchanged between these signal wells and a set of storage wells through a set of sampling wells. At the time when it is desired to capture the signal, the sampling gates are closed by an applied voltage step with a transition time which is short relative to one-half an RF period, and a sampled replica of the SAW waveform is now stored in the CCD storage wells. The transfer gate is then opened to parallel-load these charge packets into the CCD shift register, whereupon the data, which had been riding on the SAW signal, is shifted out in serial fashion at a rate determined by the CCD clock.

FIXED-PATTERN NOISE

The dynamic range of these devices is limited by fixed-pattern noise caused by threshold voltage variations in the CCD. We have devised a charge equilibration clocking scheme which significantly reduces the effect of these threshold voltage variations. This scheme is an extension of the "fill and spill" technique and is similar to the technique devised by Emmons, et al[1,2].

The details of this scheme are illustrated in the potential well diagram of Fig. 2. The charge storage wells (labeled SAW, SAG and STG) are first filled from the CCD ϕ1 wells. Next the ϕ1 wells are emptied and the excess charge is spilled over the partially closed transfer gate (labeled XG). The sampling gate (SAG) is closed momentarily in order to make the total charge independent of its threshold voltage. With the sampling gate open and the transfer gate closed, the RF piezoelectric displacement field causes charge to be exchanged between the two wells labeled SAW and STG. After the sampling gate is closed to capture the charge pattern resulting from the RF data signal, this charge pattern is transferred to the CCD by again partially opening the transfer gate and skimming off the signal charge from the storage well (STG) as shown at the bottom of Fig. 2. If some charge is left behind in the storage well, the output charge will be proportional only to the difference in charge, and will therefore be independent of all threshold voltages.

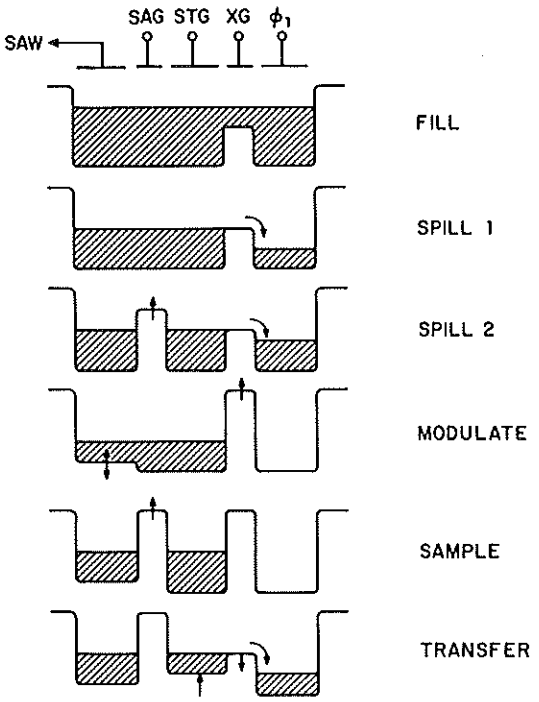

Fig. 2. Potential well diagram of the charge transfer states in the SAW/CCD device.

UNDER-SAMPLING

It is not necessary to recover the full spatial content of the piezoelectric wave if the input signal is of limited bandwidth, Δf. The required spacing of the sampling fingers can be determined by defining an effective sampling frequency, f_s, which is related to the spatial period of the sampling fingers, S_c, through the velocity of the surface acoustic wave, V_a, by

$$f_s = V_a/S_c \qquad (1)$$

S_c also defines the length of the CCD cell since there must be one CCD cell for each sampling finger. Since the input signal is contained in a limited band from $f_c - \Delta f/2$ to $f_c + \Delta f/2$, where f_c equals the center frequency of the input signal spectrum, the piezoelectric wave can be under-sampled at a frequency below the input spectrum as shown in Fig. 3a. With this sampling scheme,

the effective output center frequency is translated down by an amount equal to f_s.

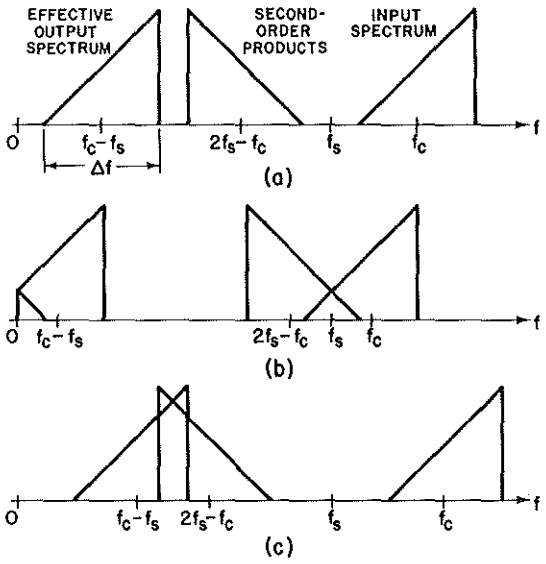

Fig. 3. Frequency spectrum of an input signal centered around f_c and under-sampled at a frequency f_s: (a) f_c acceptable, (b) f_c too low, and (c) f_c too high. Frequencies above the input spectrum are not shown.

The frequencies f_s and f_c must be chosen carefully so that the output sampled data stream from the CCD is an accurate replica of the input signal and does not contain undesirable signal distortions as a result of the sampling process. In sampled data theory such distortions are called "aliasing", or "frequency folding". Folding and spectral overlap can be seen in Figs. 3b and 3c. In the following paragraph, we will derive a set of inequalities which can be used to select f_s and to find the maximum bandwidth for a given f_s.

According to the sampling theorem, the effective sampling frequency must be greater than twice the desired information bandwidth

$$f_s > 2\,\Delta f \qquad (2)$$

This relation can be used to select the effective sampling frequency. Once a sampling frequency has been chosen, there are limits on the permissible range of input frequencies. The input frequency f_{in} cannot be below the sampling frequency:

$$f_{in} > fs. \qquad (3)$$

There is also an upper limit on the input signal frequency. Second-order mixing products (sidebands of the second harmonic of the sampling frequency) must not overlap the output spectrum (see Fig. 3c):

$$2\,f_s - f_{in} > f_{in} - f_s \qquad (4)$$

Inequalities (3) and (4) can be rearranged into one relation for the acceptable range of input signal frequencies:

$$f_s < f_{in} < 3\,f_s/2 \qquad (5)$$

This relation can be used as a guide in designing the SAW input transducer.

For our initial experiments we chose a convenient CCD cell size of 40.6 μm which defines f_s to be 85.7 MHz for a lithium niobate ($LiNbO_3$) delay line with a propagation velocity of 3480 m/s. This sampling frequency constrains the input signal to be in the range of 85.7 to 128.6 MHz for a maximum bandwidth of 42.9 MHz. A 300-stage device with this cell size is 12.2 mm long and has an acoustic delay time of 3.5 μs.

FABRICATION

A prototype device has been fabricated and tested; a photomicrograph of the die is shown in Fig. 4. It is 14 x 3.7 mm and is dominated by the 2.8-mm long polysilicon sampling fingers which dwarf the CCD shift register running along the bottom of the chip. A 2-phase, implanted barrier structure is used, with polysilicon for storage gates and aluminum for the barrier gates[3]. An n-type ion-implanted buried channel is used to ensure high-speed exchange of charge between the signal well and the storage well. Alignment marks are etched on the ends of the die for precise angular alignment of the sampling fingers with the wavefronts generated by the SAW transducers on the delay line. The finished die is attached to a specially fabricated header using a flexible sheet of Kapton so that it can be pressed against spacer rails on the

SAW crystal. Fig. 5 shows the SAW crystal mounted on a base and ready to be mated with the silicon-Kapton header sub-assembly This assembly scheme is based on the technique developed for acoustoelectric convolvers[4], and is described in more detail elsewhere[5].

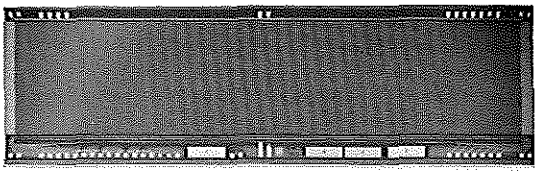

Fig. 4. Photograph of a 300-stage SAW/CCD buffer memory device. Die size is 14 x 3.7 mm.

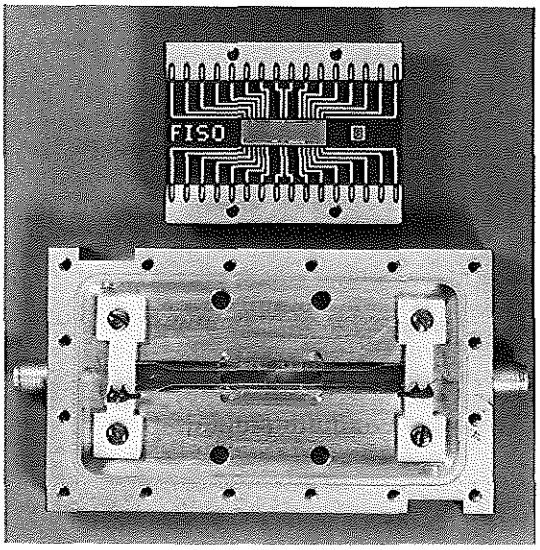

Fig. 5. Photograph of a partially assembled SAW/CCD device including silicon CCD die, Kapton sheet, $LiNbO_3$ delay line, and metal parts.

EXPERIMENTAL RESULTS

The prototype has been tested at a CCD clock rate of 100 KHz and at input signal frequencies between 80 and 130 MHz. From the sampling theory presented above, one would expect frequency folding to occur at 85.7 and 128.6 MHz. Frequency folding occurred in the prototype at 85.6 and 128.4 MHz, within 300 KHz of the predicted values. The output signal amplitude should be critically dependent upon the fall time of the 10-volt negative-going step applied to close the sampling gate when the fall time approaches the 5-ns half-period of the input signal. In fact, this fall time could be varied from 1 to 10 ns with no apparent change in the output waveform. The reason that this transition can be so slow compared to the 5-ns half-period of the input signal is the fact that the closing of the gate actually occurs over one volt of the 10-volt step, or in a time interval approximately one-tenth the total transition time. For transition times greater than 10 ns, the output signal amplitude dropped with increasing transition time as expected. No partitioning noise was observed even with the sharpest edge available (around 1 ns).

Figure 6 is an example of the full 300-cell CCD output waveform at a CCD clock frequency of 100 KHz. The input signal is a 90 MHz sinusoid with a duration of 1.8 μs at an input power level of 1 watt. Sampling occurs when this input pulse is near the center of the delay line. This input frequency is translated by the sampling process to an effective output frequency of 4.4 MHz, which is the difference between the input of 90 MHz and the 85.6 MHz effective sampling frequency. As a result of this frequency translation, the sampled output waveform in Fig. 6 has 4.4 MHz x 1.8 μs = 7.9 cycles rather than the 90 x 1.8 = 162 cycles contained in the 1.8-μs pulse at the input. The amplitude

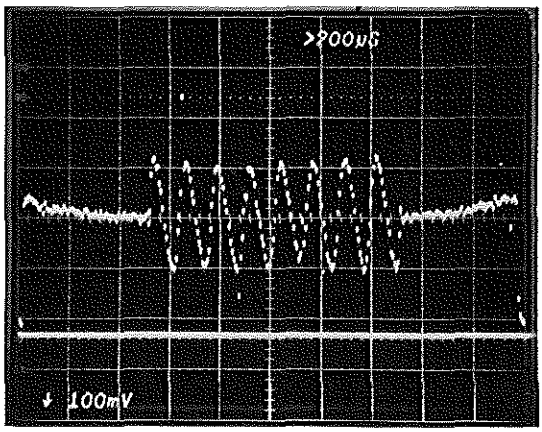

Fig. 6. Oscillograph of SAW/CCD buffer memory operation at an input carrier frequency of 90 MHz and an output clock rate of 100 KHz. The input pulse width is 1.8 μs.

and phase of the output signal tracks that of the input signal as expected. A clock generator to fully implement the charge equilibration scheme depicted in Fig. 2 is not yet available, so that excessive fixed-pattern noise is visible in Fig. 6. Even so, a dynamic range of 25 dB has been observed. With the more sophisticated clocking scheme, a higher dynamic range is expected.

CONCLUSION

We have used successfully the acousto-electric interaction between a piezo-electric surface wave and a silicon CCD to implement a fast-in, slow-out buffer memory function. This compact solid-state device serves to store wideband analog signals and read them out at a slow data rate. Devices of this type promise to provide wideband analog buffer memory functions for as many as 1000 discrete samples.

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