DEVELOPMENT AND DESIGN OF A NOVEL TWO LEVEL 64k-BYTE CHARGE-COUPLED MEMORY SYSTEM FOR MICROCOMPUTER APPLICATIONS.

S.G. Chamberlain R.J. Inkol

University of Waterloo, Electrical Engineering Department,
Waterloo, Ontario N2L 3G1

ABSTRACT: Charge-Coupled Device memory technology offers potential economic advantages over semiconductor random-access memory technologies. However, the limitations incurred by the serial nature of the Charge-Coupled Device (CCD) have restricted most efforts to apply CCD memory technology to large memory systems. This paper demonstrates the feasibility of a CCD memory technology for moderate size memory systems.

A 64k-byte memory system using commercially available Charge-Coupled Devices has been developed for microcomputer applications. Design objectives included low-cost, adequate performance, reliable operation, small size and low power consumption as well as simple interfacing to standard microprocessors. The design of the developed memory system features a two-level organization which includes a RAM to buffer the Charge-Coupled Device serial memory; this improves the average access time and simplifies interfacing with standard microcomputers.

By taking advantage of the track-sector organization of the Intel 2416 CCD memory device, a relatively simple hardware implementation of the memory system was realized; this eliminated the need for the software implemented operating system which characterizes many other bulk storage memory systems.

The developed memory system fills a gap between high performance semiconductor random-access memory and the slower serial magnetic memory technologies. Design details of the memory system and experimental results obtained with a 16k-byte prototype will be presented in this paper. Testing of the memory system prototype with a KIM-1 microcomputer system demonstrated that the technical objectives have been successfully realized. It is anticipated that the memory system can be easily modified to use the new Intel 2464 which is 64k word X 1 bit CCD memory device.

I. INTRODUCTION

Charge-Coupled Device (CCD) memories offer significant economic advantages for bulk storage of digital data [1] relative to MOSFET and bipolar RAMs. However, the serial organization of data in CCD memories has the disadvantage that the random access of data is slow due to the serial latency time. Typical values for commercially available designs are 100 μs average [2] and 0.8 ms maximum [3]. Thus CCDs cannot directly compete with semiconductor RAMs where the high speed random access of data is important. However it is anticipated that CCDs may find usage in microcomputer systems where a CCD memory buffered by a random access memory offers a logical solution to the problem of economic bulk memory.

The intention of our paper is to demonstrate the feasibility of this concept. Features of our developed 64k-byte two-level memory system include simple interfacing with standard microprocessors, parity checking, low power consumption and small size.

II. CONSIDERATIONS FOR A TWO-LEVEL CCD MEMORY SYSTEM

The cache memory concept makes use of the fact that data in a memory system is seldom accessed from memory locations at random [4]. Consequently selected blocks of data from a large and slow primary memory (M_p) can be stored in a small fast cache memory (M_c) where they may be rapidly accessed by the Microprocessor Unit (MPU). Requests for other data in the memory system necessitate the comparitively slow transfer of the requested data from M_p,

either directly or via M_c with some consequent reduction in the average memory system speed.

The simplified direct address buffer organization defined in Figure 1, is the simplest possible cache memory organization. It involves the division of the 2^n word primary memory (M_p) into pages of 2^m words in length. The (n-m) highest order address bits of a word determine the page that it is located in (the page address), while the remaining m lowest order address bits define the location of the word within the page. The cache memory (M_c) provides random access storage of a single page of data. The MPU can directly address a word of data within this page by using the m lowest order address bits.

Page oriented cache organizations such as the direct address buffer organization are well suited for applications with CCD primary memories. Pages of data may be stored in a CCD shift register memory on consecutive sectors (shift register data locations) in one or more tracks (shift registers). After the latency time required to reach (search for) the first bit in the page, data may be transferred at a rate equal to the product of the data shift rate and the number of tracks accessed on each data shift. Consequently one search operation (for the first bit of the page) is sufficient for the transfer of the entire page.

The average time to transfer a page of data will then be:

$t_{pt} = t_\ell + \frac{p}{d_{max}}$ where t_ℓ = latency time, p = page size.

d_{max} = CCD average data rate for uninterrupted data transfer from consecutive sectors.

Accordingly the average data rate (d) during the page transfer will be:

$$d = \frac{p}{t_{pt}} = \frac{d_{max}}{1 + \frac{t_\ell \, d_{max}}{p}}$$

Normally $t_\ell >> \frac{1}{d_{max}}$, so the average data rate is substantially increased for page sizes much larger than 1 word.

The serial nature of the CCD memory becomes a useful property for data transfer between M_c and M_p since a single data bus is sufficient. With appropriate three-state logic techniques, the same data bus may be used to interface M_c to the processor. Another useful design economy may be realized by using the CCD memory sector address counter to generate the address for M_c during data transfers between M_c and M_p.

These factors all favour a hardware rather than a software implementation of a two-level memory system. A hardware implementation offers useful performance advantages since normally a limited set of logical operations will be performed for each memory access; these can be realized with specialized logic modules of sufficiently high performance that system speed is not adversely affected. A hardware implementation may be designed to be almost completely transparent; i.e., the memory system is functionally identical to a conventional memory system based on random access memory technology except for the necessity of requiring the processor to enter a wait state during internal data transfers between M_c and M_p resulting from data requests for new pages.

A most fundamental design problem is to determine the optimum sizes of M_c and M_p. Clearly M_p should be much larger than M_c, otherwise a single-level memory system would be both simpler and more economical. On the other hand, M_c should be large enough that the ratio of the number of times that requested data is in M_c to the total number of data requests (the h or "hit" ratio) should be high; otherwise the memory performance will be poor.

Parity checking may be performed either on the M_c I/O buffer or on the M_p I/O. The former has the advantage that parity checking is effective on M_p as well as M_c while the latter requires fewer components since M_c need not store parity bits.

III. MEMORY SYSTEM DESIGN AND IMPLEMENTATION

Basically our memory system consists of the four components blocks illustrated in Figure 2; the Primary Memory M_p realized with commercially available 16k-bit CCD memories for economic bulk data storage, the Cache Memory M_c for random access storage of data pages fetched from M_p, and the I/O

Buffer to interface M_c to the external data bus, and the Control Unit which generates the control signals for both M_p and M_c.

A design capacity of 64k words x 9-bits (including parity bits) for M_p was selected as a suitable value for potential microcomputer requirements. This also provides some hardware compatibility with the new 64k-bit CCD memories. Due to the modular design philosophy employed, word length expansion can be directly achieved by the parallel operation of additional M_p and M_c units from a common control unit.

To realize a 64k word x 9-bit memory capacity for M_p, the Intel 2416 16k x 1-bit CCD memory devices are conventionally organized as a 4 x 9 matrix (Fig. 3). The 2416 memory device is internally organized as a linear array of 64 recirculating shift registers which are each 256-bits in length. As a consequence of the serial nature of the CCD memory, the memory system uses two modes of addressing to access data in the 2416 memory devices:

(i) Track addressing: Each 2416 track (representing a 256 bit recirculating shift register) has a single I/O port which may be used to access a bit of data stored in a sector (representing a shift register storage cell). The decoded 6-bit CCD track address (A_0 - A_5) selects 1 of 64 tracks for data I/O operations. Between shift operations performed by the 4ϕ CCD clocks, it is permissible to sequentially access different tracks for I/O operations by utilizing this track addressing feature. In this respect, the 2416 memory I/O design resembles that of a 64-bit dynamic RAM, the major difference is that only 1 of 256 sectors in each track is addressable by the track address at any given time, whereas every data location in a RAM is addressable.

A 1 x 9 device organization in each row of Figure 3 corresponds to a 16k word x 9-bit data organization when both sector and track addressing modes are used. Memory Bit/Word expansion is most directly accomplished by affecting a track expansion; additional rows of 2416s are operated in parallel with data selected from the appropriate device in each column. This is demonstrated in Figure 3 where the two additional address bits, CA_{14} and CA_{15}, are decoded to select 1 of 4 rows via the 2416 Chip Select (CS) inputs. In each column the 2416 data inputs and outputs are connected in parallel and WIRED-OR configurations respectively. The unselected devices continue to recirculate their data, but their inputs and outputs are disabled. The four devices in each column are thus functionally equivalent to an array of 256 tracks of which 1 is selected for data I/O by an eight-bit track address for a total data capacity of 64k x 1 with both track and sector addressing.

The organization of the track address bits in the memory system is closely related to the memory data page organization. The 64k word x 9-bit capacity of the CCD memory (M_p) is divided into 256-byte pages for data transfer operations to the cache memory (M_c). Each page of data in M_p corresponds to 16 consecutive sectors x 16 tracks in each column of Figure 3. On page transfer operations, the CCD A_0 - A_3 track address bits are stepped from 0 through 15 on each data shift by the CA_0 - CA_3 address generated by a 4-bit binary counter C_1 in the Control Unit. These address bits partially define data locations within a page. The CA_{12} - CA_{15} address bits select blocks of 16 tracks from which data is accessed by the CA_0 - CA_3 address bits on each data shift during page transfers, therefore pratically defining the page address.

(ii) Sector Addressing: The basic CCD data storage element is the shift register. Each of the shift registers in the 2416 memory device is composed of paired 128-bit shift registers multiplexed to function as a 256-bit recirculating shift register. A data or sector location in each shift register will physically change with each data shift; returning to the same location after 256 data shifts. To access a particular sector, it is necessary to perform a data search operation by waiting for the desired sector to be shifted to the track I/O port by the CCD 4ϕ clocks. As each sector is cyclically shifted through 256 shift register cells, and the relative locations of the sectors are fixed, the relative location of the sector at the shift register I/O port is defined as a sector address which can be specified by the output of an 8-bit binary counter clocked at the data shift rate.

In the memory system Control Unit (Figure 4), and 8-bit counter, C_2, is clocked at the CCD data shift rate by the ϕ_B clock to generate the sector address bits AC_4 - AC_{11} ($\triangleq$ CA_4 - CA_{11} during data transfers between M_c and M_p). Address bits AC_8 - AC_{11} define blocks of 16 consecutive sectors on each track, thereby specifying a page address in combination with track address bits CA_{12} - CA_{15}. Page trans-

fers are permitted by the Control Unit when the page subaddress AD_8 - AD_{11} in the M_c Page Register corresponding with the page to be transferred matches AC_8 - AC_{11}. Sector addressing thus consists of counting and comparison operations performed in the control unit; no explicit sector addresses appear in M_p.

A page address is completely specified by the CA_8 - CA_{11} sector address bits and the CA_{12} - CA_{15} track address bits while the word address within a page is defined by the CA_0 - CA_3 track address bits and the CA_4 - CA_6 sector address bits. Thus 16 address bits define a word location in the 64k word memory M_p.

During page transfers, CA_8 - CA_{15} define the page address of the data being transferred while address CA_0 - CA_8 is incremented from 0 through 255 to effect the transfer of 16 consecutive sectors of data from 16 tracks for each bit/word. This is illustrated in Figure 5 for a conceptual page transfer involving Page 0 in M_p.

The design of the M_p memory is illustrated in Figure 6. The 2416 address lines A_0 - A_5, CE, CS and WE lines are driven by Intel 3245 quad TTL to MOS level translators. These devices have the advantage that they offer suitable output levels for the CCD memory devices without additional power supplies. The CCD 4ϕ clocks are driven by a 5224 quad clock driver for each 4 memory devices. The 5224 is specifically designed for the required output levels and transition times for the 2416 memory devices.

Page transfers between M_p and M_c involve the serial transmission of eight-bit parallel words. The ninth bit is used for single error detection on the M_p data lines. A 74LS280 parity generator/checker generates single parity bits for each word of input data to M_p; these parity bits are stored in M_p with the corresponding 8-bit data word. Another 74LS280 performs a parity check on the M_p output data. A JK flip-flop is used to monitor the parity check output for error indications during data transfers from M_p to M_c. A momentary contact switch permits the flip-flop to be manually reset.

The directly addressed cache memory of figure 7 has a capacity of 1 page (256 words x 8-bits). Static MOS/RAMs of the 2101A-2 type were employed because they offer adequate performance and their simple timing requirements facilitated interfacing M_c to both M_p and the MPU data bus. Intel 3212 latch/buffers with 3 state outputs are used to interface M_c to the bidirectional MPU data bus. The address organization of M_c is equivalent to that used by M_p with the difference that the CA_4 - CA_7 address bits exist explicitly since M_c is a random access memory.

During memory system operation, the Control Unit executes the sequence of operations defined in Figure 8 in response to the MPU I/O signals. There are basically two modes of operation:

(i) I/O Mode: When the MPU requests data from a page stored in M_c, M_c is placed under the direct control of the MPU I/O signals via the I/O logic. M_c then looks like a conventional static RAM to the MPU which addresses it via the SA_0 - SA_7 address bits.

During the I/O mode, data is recirculated in M_p at the minimum shift rate (55 KHZ) to reduce AC clock power requirements. The M_p I/O is forced into an inactive state by keeping the CCD CE and WE signals low and disabling the outputs of the latch used to buffer the CCD data outputs.

(ii) Page Transfer Mode: When data from a new page is requested by the MPU, the Memory Management Logic implements the required data transfer operations between M_c and M_p to reach the conditions satisfying the I/O mode criteria. During the page transfer mode, the MPU is placed in a wait state via the Mready signal and the I/O Logic is disabled.

A major difference between the two modes of operation is that M_c is synchronized to the MPU clock in the I/O Mode, and to the CCD 4ϕ clocks in the Page Transfer Mode.

The essential purpose of the I/O Logic is to use the MPU I/O control signals to interface the MPU to M_c via the I/O Buffer and address latches A and B. The I/O Logic was designed after a study of the I/O signals from several standard MPUs. The major restriction is that the MPU can be placed in a wait state with a Wait or Ready signal after a valid address is available. This is to permit the Control Unit to place the MPU into a wait state during the Page Transfer Mode following a request for data in a new page by the MPU. Many MPUs such as the Intel 8085 and 8080, the Zilog Z-80 and with some restrictions, the MOSTEK 6502 can readily meet this requirement.

IV. EXPERIMENTAL RESULTS

A prototype of the CCD memory system was constructed with a reduced M_p capacity of 16k x 8, (Figure 9). A total of 53 integrated

circuits on two 9" x 4 1/2" circuit boards were required. The total number of integrated circuit package, and types required for both 16k word x 8 bit and 64k word x 9 bit memory systems is given in Table 1.

The memory system functioned as intended. Figures 10 and 11 illustrate the major control signal waveforms used in serial data transfers from M_p to M_c; the CCD $\phi 1$, CCD CE, $\overline{\text{RAM WE}}$ and CCD D_{out} signals in Figure 10 and the CCD $\phi 1$, CCD CE, $\overline{\text{RAM WE}}$ and CCD A_0 waveforms in Figure 11. The relative timing of the CCD CE and $\overline{\text{RAM WE}}$ signals is very important since the timing of the data output from M_p will be dependent on the CCD CE signal, and in turn the $\overline{\text{RAM WE}}$ signal must be set up to write the data from M_p into M_c. The data track and sector organization used in the memory system results in 16 data cycles on each shift, or 32 for each complete 4ϕ clock cycle; the relationship of the CA_0 address bit used for the A_0 track address bit on the CCD memory device to the CCD $\phi 1$, CCD CE and CCD WE signals can be seen in Figure 11.

A MOS Technology KIM-1 microcomputer was successfully interfaced to the memory system with the aid of some additional support circuitry to:

1. Buffer the KIM 6502 I/O.
2. Synchronize the Mready signal to the MPU $\phi 2$ clock.
3. Fully decode the MPU address lines.
4. Temporarily store the MPU data and address during write operations to new pages. This is necessary as the 6502 MPU will enter a wait state only during a read operation.

Tests conducted with the KIM microcomputer demonstrated that the major technical criteria for a memory system were fulfilled:

(i) Performance: Conservative timing margins were obtained in the I/O mode for the standard 1 MHz clock frequency of the KIM microcomputer. In the Page Transfer Mode, an average latency time of 128 μs and a page transfer time of 144 μs were achieved without difficulty. The average time to perform a data transfer between M_c and M_p is therefore 144 μs + 128 μs = 272 μs which corresponds to the average memory cycle time if data in M_c has not been modified. Otherwise two page transfers are required and yield an average memory cycle time of 544 μs.

(ii) Reliability: Reliability is a fundamental memory system consideration. It is essential that the memory system be free of pattern sensitivity problems which may manifest themselves as troublesome "soft" errors. It has been demonstrated that a few simple test patterns predicated on the CCD internal organization are sufficient for adequately testing a CCD memory.

Tests conducted with the recommended test [5] patterns revealed reliable memory operation was possible over a wide range of supply voltages.

(iii) Power Consumption: Three standard power supply voltages are required by the memory system: + 12 V, + 5 V, - 5 V. The measured current requirements for the 16K x 8 prototype are shown in Table 2.

The + 12 V current consumption may be extrapolated for the full 64k x 9 memory capacity to yield a total I/O Mode power consumption of only 13.8 μW per bit.

V. CONCLUSIONS

The use of two-level memory organizations featuring a CCD primary memory is both feasible and practical in microcomputer systems.

VI. REFERENCES

[1] L.M. Terman and L.G. Heller, "Overview of CCD Memory", IEEE Journal of Solid State Circuits, Vol. SC-11, February 1976, pp. 4-9.

[2] Intel Data Catalog 1977, Intel Corporation, 1976.

[3] TI's 65 K CCD, Electronics, March 17, 1977, p.38.

[4] G.G. Scarrot, "The Efficient Use of Multi-level Storage", Proc. IFIP Cong., 1965, pp. 137-141.

[5] I.D. Vancov, "Pattern Sensitivity Techniques for Testing CCD Memories", Computer Design, November 1977, pp. 106-109.

VII. ACKNOWLEDGEMENTS

This work was supported by a research grant from the National Research Council of Canada, grant number A7384.

TABLE 1. MEMORY SYSTEM INTEGRATED CIRCUIT LIST

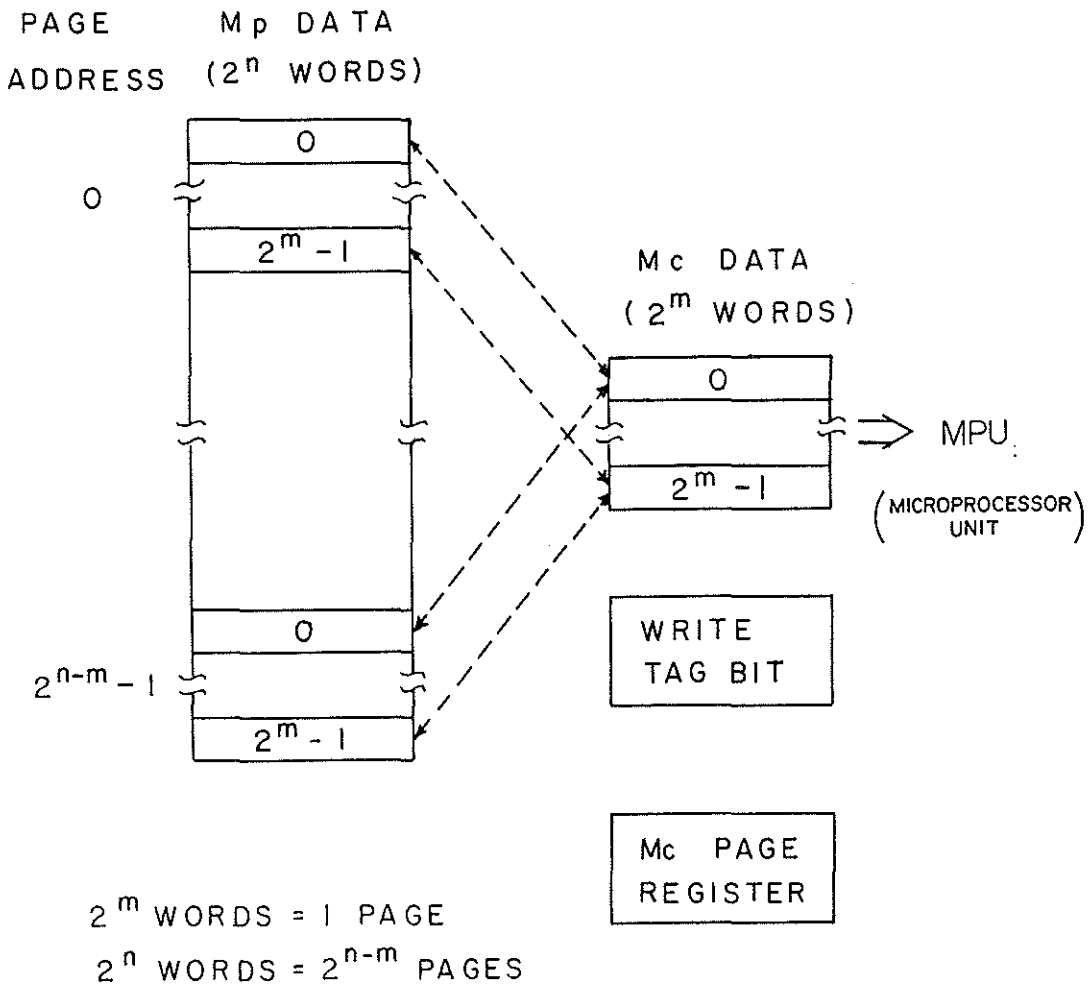
Integrated Circuit Type		Quantities	
		16K word x 8-bit	64K word x 9-bit
2416	CCD Memory Device	8	36
5224	Quad CCD Clock Driver	2	9
3245	Quad TTL to MOS Buffer	2	3
2101A-2	256-Bit x 4 Memory	2	2
8212/74S412	Octal Latch/Buffer	6	6
74LS00	Quad 2-Input NAND Gate	1	1
74LS04	Hex Inverter	6	6
74LS08	Quad 2-Input AND Gate	1	1
74LS28	Quad 2-Input NOR Buffer	1	1
74LS37	Quad 2-Input NAND Buffer	3	3
74LS74	Dual D-type Flip-Flop	2	2
74LS76	Dual JK Flip-Flop	2	3
74LS85	4-Bit Comparator	3	3
74LS86	Quad 2-Input EXCLUSIVE-OR Gate	1	1
74123	Dual Monostable Multivibrator	4	4
74LS126	Quad 3-state Buffer	2	2
74LS132	Quad 2-Input NAND Schmitt Trigger	1	1
74LS138	3 to 8 Line Decoder	1	2
74LS161/ 74LS163	4-Bit Binary Counter	3	3
74LS164	8-Bit Shift Register	1	1
74LS221	Dual Monostable Multivibrator	1	1
74LS280	9-Bit Parity Checker/Generator	-	2

TABLE 2. MEMORY SYSTEM POWER CONSUMPTION*

		I_D	Power
+ 12.0 V	I/O MODE	49mA (220mA)	.59W (2.64W)
+ 12.0 V, Page Transfer Mode	Data Search	170mA (765mA)	2.04W (9.18W)
+ 12.0 V, Page Transfer Mode	Data Transfer	105mA (472mA)	1.26W (5.66W)
+ 5.0 V		1.1A	5.5W
- 5.0 V		~ several μA	

* for 16k x 8 prototype memory system, values in parenthesis pertain to estimates for full 64k x 9 capacity.

Figure 1. Direct Address Memory Organization.



DIRECT ADDRESS ORGANIZATION

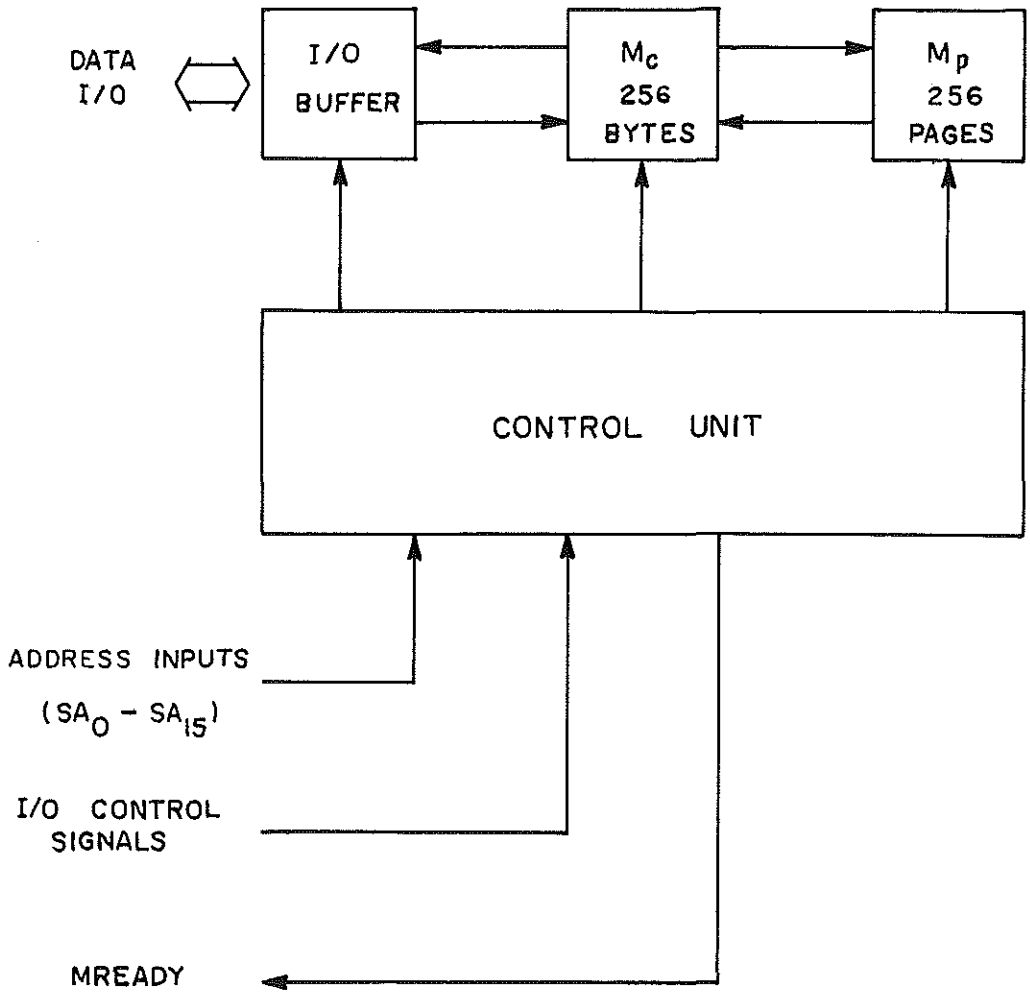


Figure 2. Block Diagram of a Simplified Two-Level Memory System Using A CCD Primary Memory

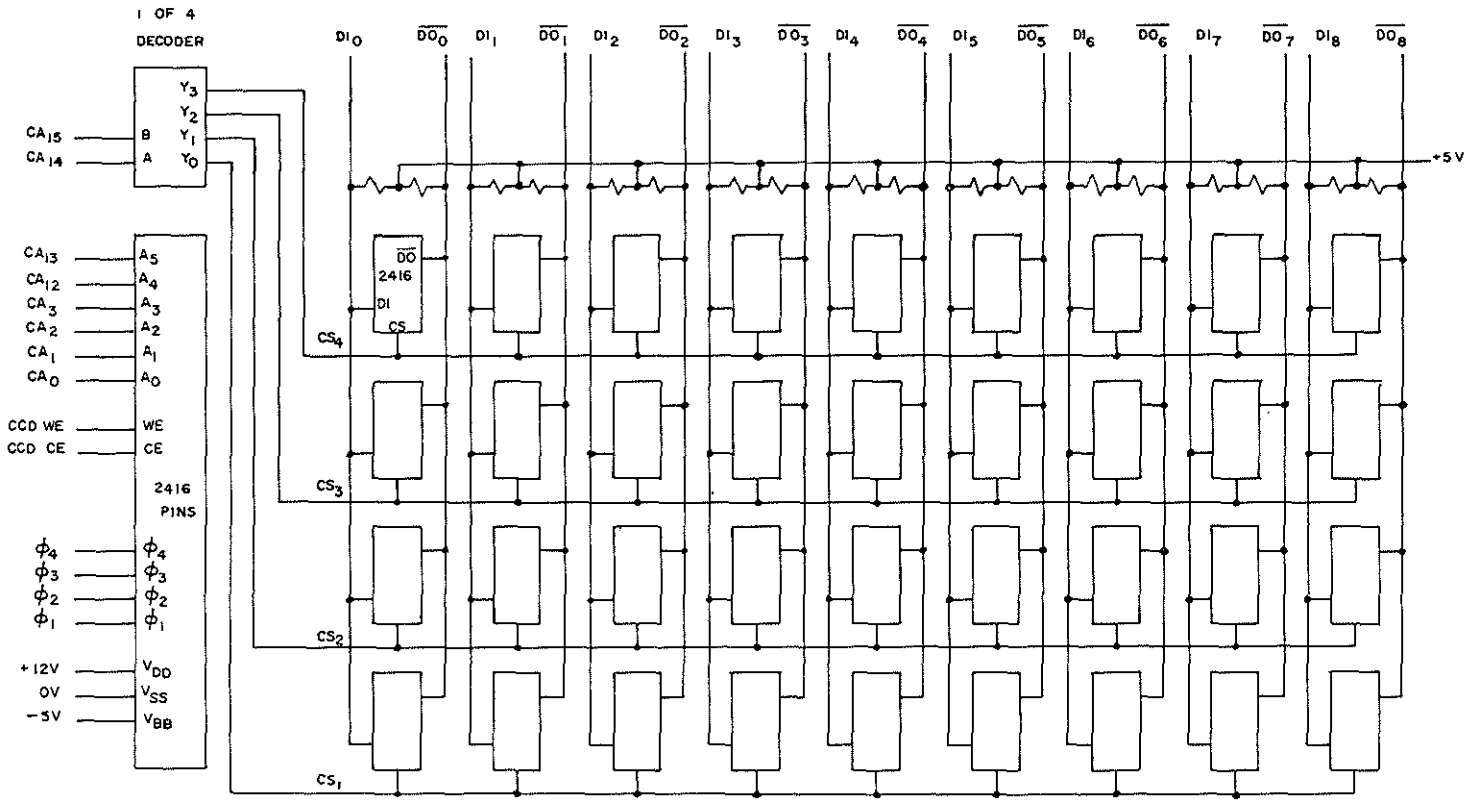


Figure 3. Organization of 16K word X 1 bit CCD Memory Devices for 64K word x 9 bit Memory Capacity

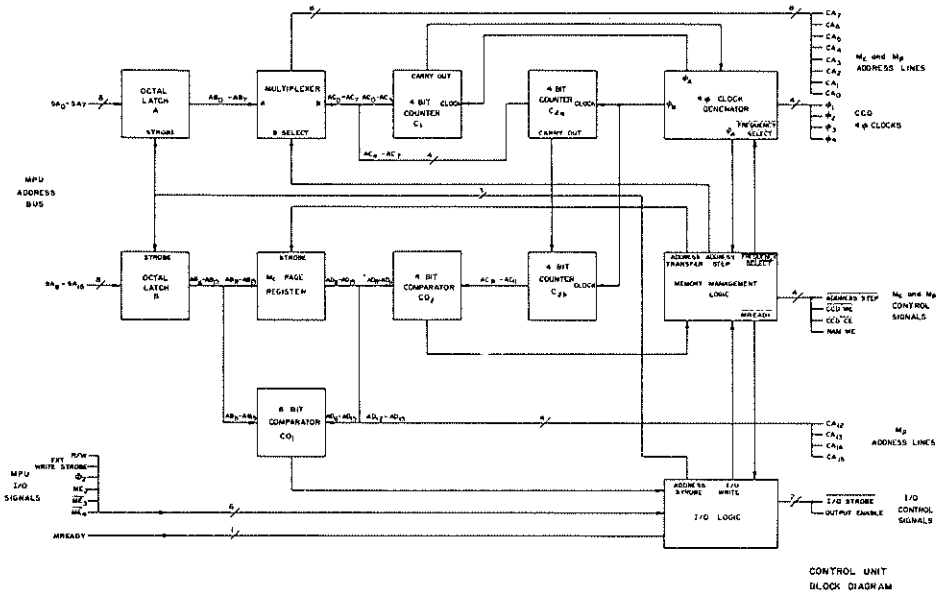
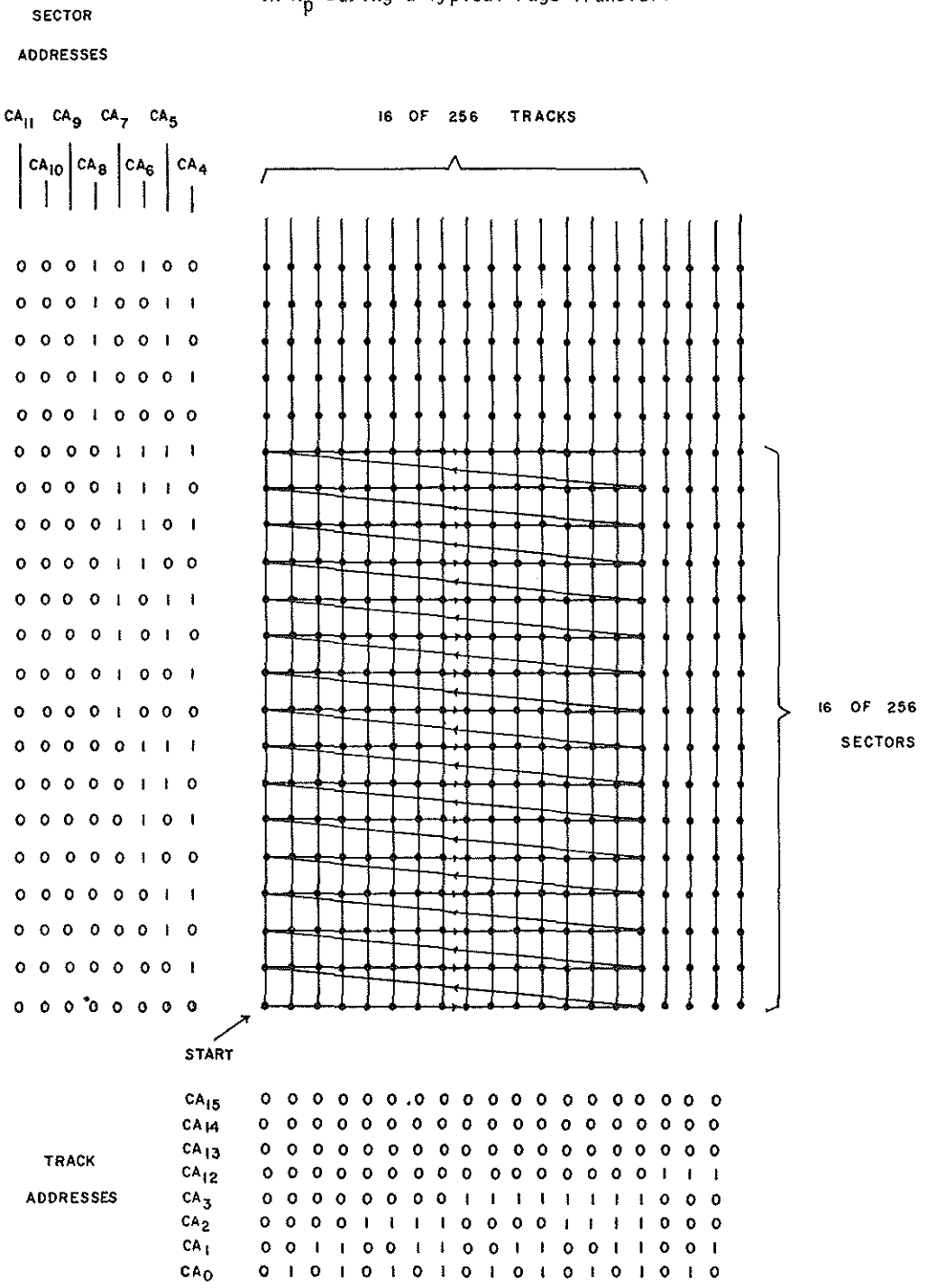


Figure 4. Control Unit Block Diagram

Figure 5. Representation for the Addressing of Data in M_p During a Typical Page Transfer.



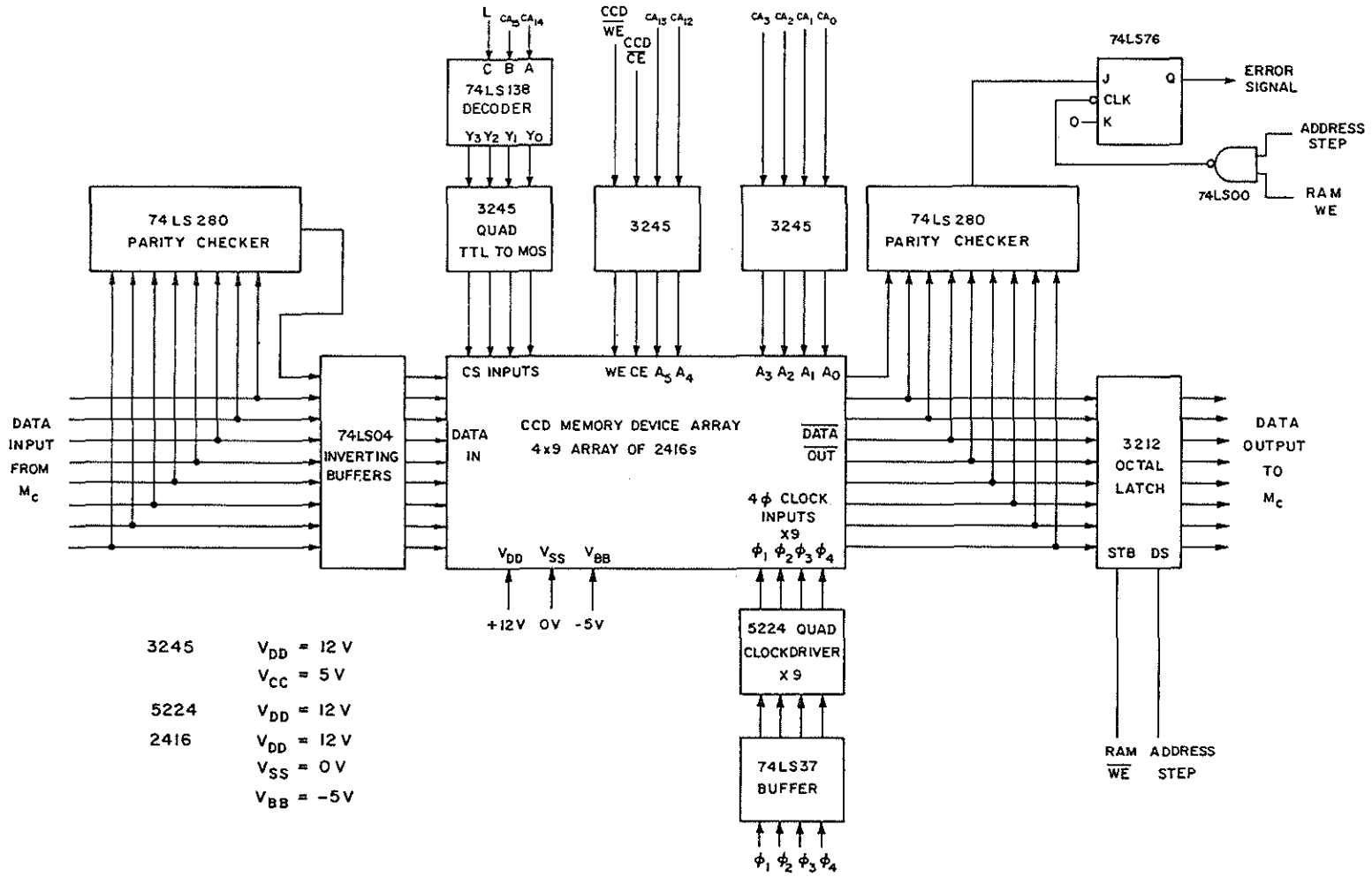


Figure 6. Organization of M_p with Support Circuitry

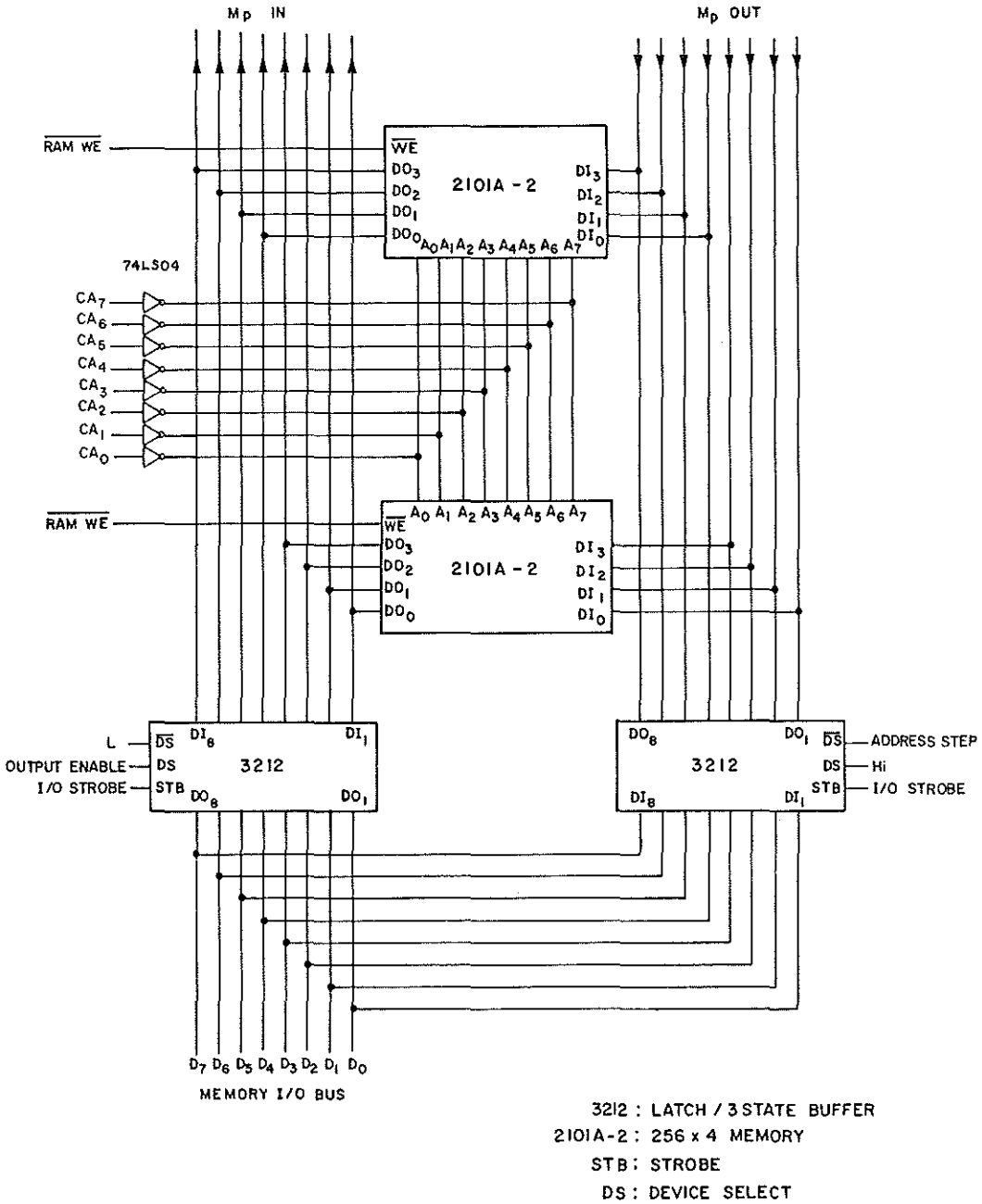


Figure 7. Organization of M_C and I/O Buffer

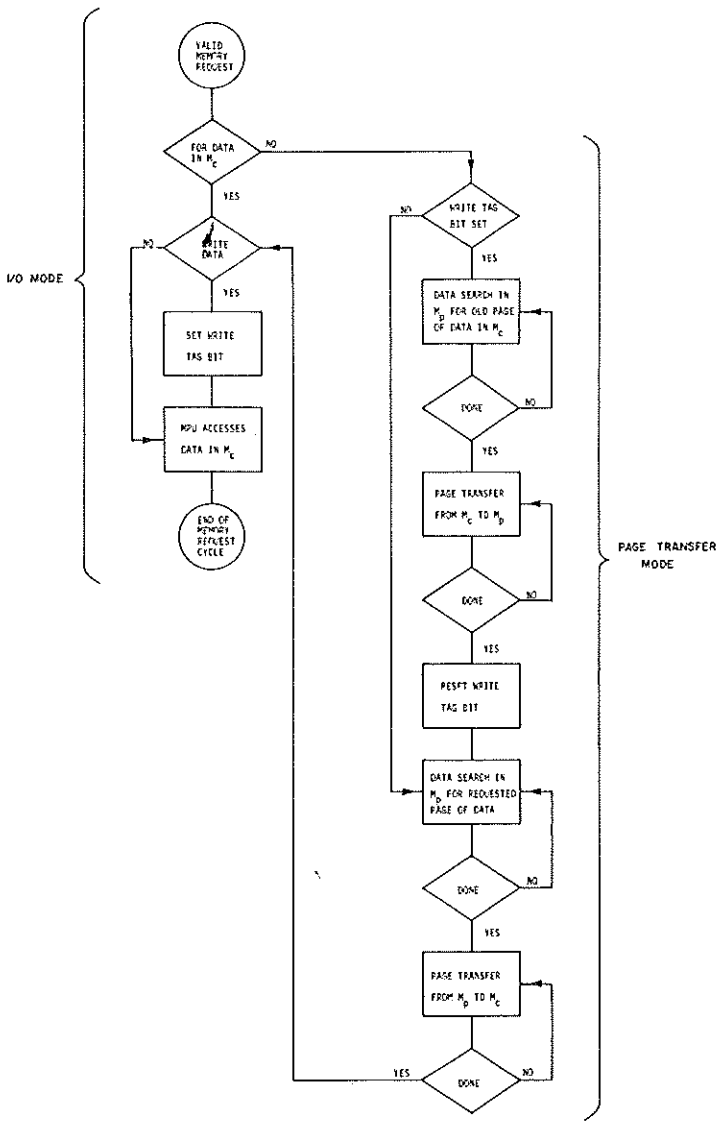
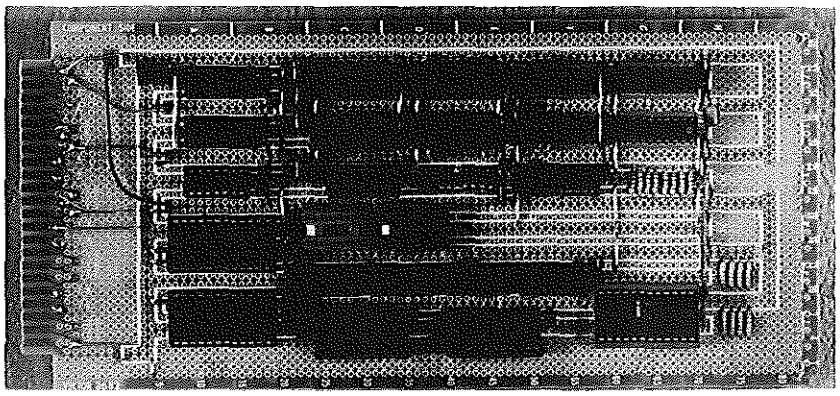
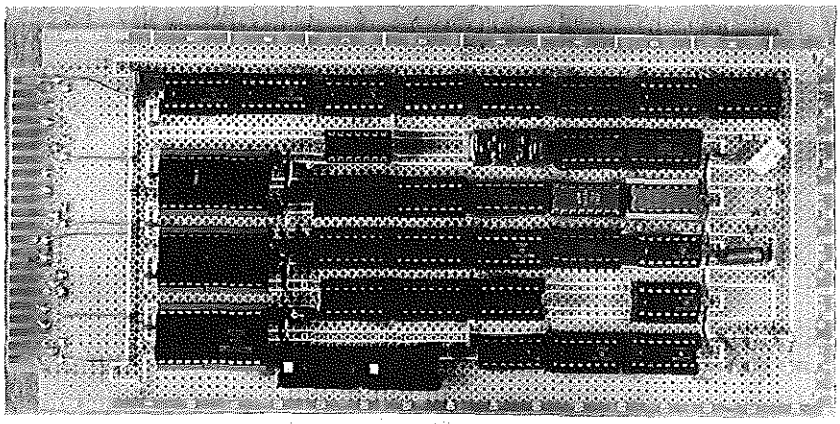


Figure 8. Flowchart of Memory System Operation



Top view of the Memory Board containing M_c, M_p, and the I/O Buffer.



Top view of the Control Unit Board.

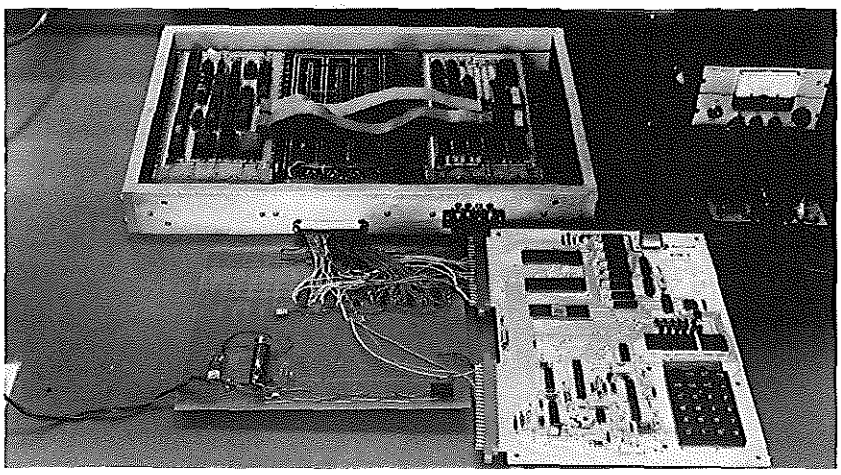


Figure 9. View of the 16k x 8 memory system prototype with 6502 Interface Adapter, KIM Buffer Unit, and the KIM-1 microcomputer.

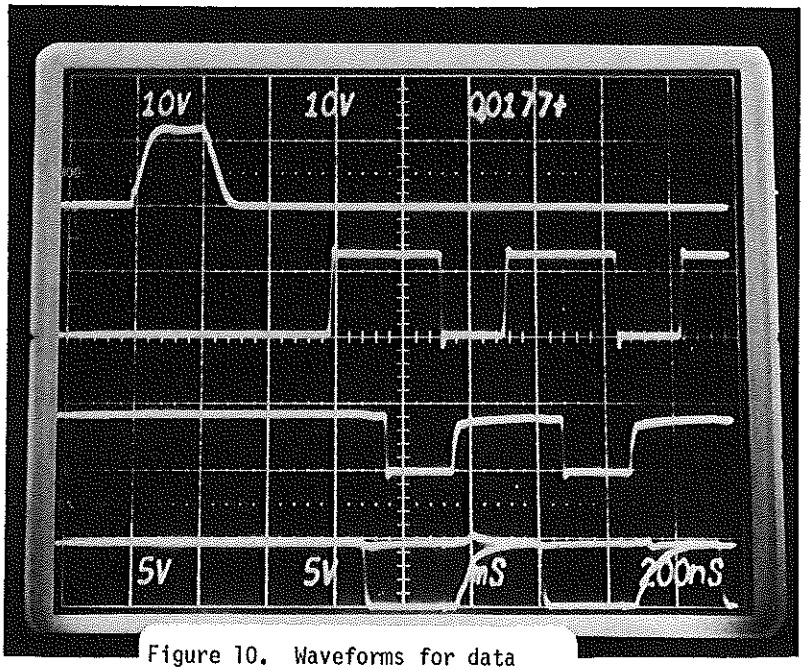


Figure 10. Waveforms for data transfer from M_p to M_c.

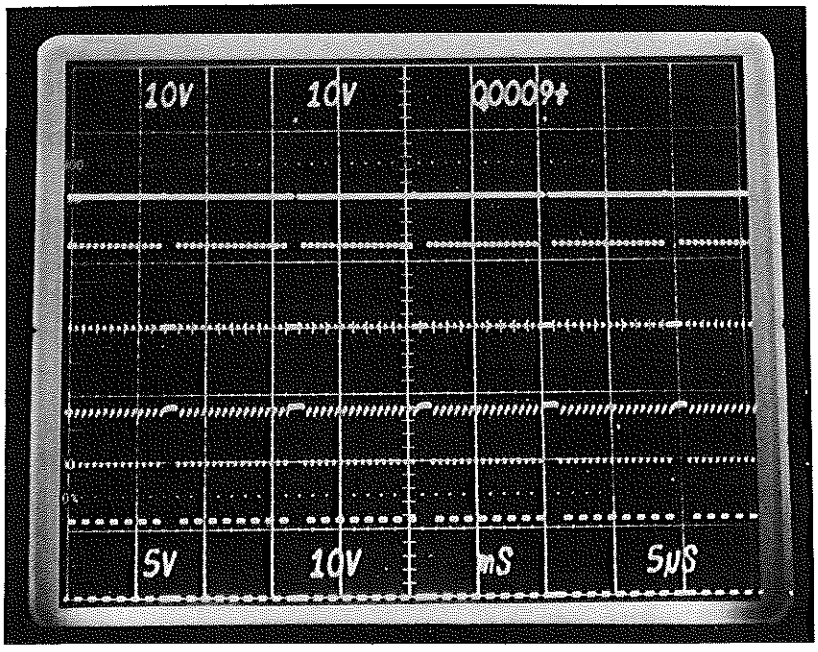


Figure 11. Waveforms for data transfer from M_p to M_c.