ELECTRONIC PROCESSING OF INFRARED SCANNER SIGNALS USING CCD MEMORY TECHNIQUES

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ABSTRACT

This paper describes the design of a video quick look which electronically processes signals of an infrared linescanner to a moving-map presentation on TV display. The image memory for display is composed of 16-kbit dynamic Charged Coupled Devices (CCD). These CCD memories are line addressable which is attractive in the case of the line scan orientation of sensing and display.

The paper gives a description of the video quick look and outlines the design of the CCD image memory. An application of the video quick look is shown in the field of thermal infrared remote sensing.

Keywords: Charge Coupled Device, Quick Look, Infra Red Scanners, Data Acquisition.

1. INTRODUCTION

A video quick look system has been built which functions as an element in the processing of airborne-recorded infrared (IR) data. The use of the quick look presentation of the infrared data is two-fold:

(i) Control of the quality of the signals from sensing equipment (Reconofax IR line scanner) and the airborne recording

(ii) Selection of significant images out of the large amount of imagery recorded during flight. The procedure of selecting the IR images directly from the flight tape prior to image processing reduces computer time (figure 1).

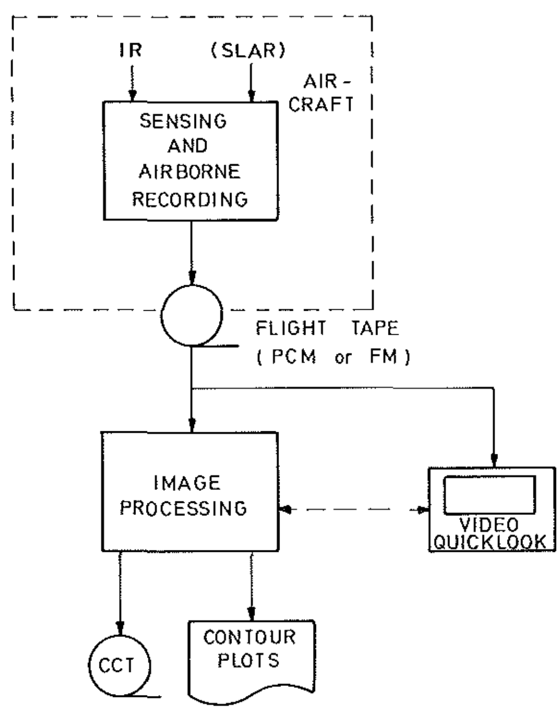


Figure 1. Recording and processing of infrared image data

The video quick look system accepts both FM analog and PCM high-density signal recordings. The system electronically processes the IR scanner signals to a moving-map presentation on TV display. At present the spatial resolution is determined by the 128*128-pixel presentation on the display. Expansion till a 512*512-pixel format is planned. The dynamic range corresponds to an 8-bit dataword per pixel. A flexible pseudo-color coding of the pixel values has been used to maintain the required dynamic range on the display.

A central part in the electronic processing of the IR line scanner data is the CCD image memory. This memory stores the incoming IR data with a linescan frequency of 380 Hz and functions as a high-speed video memory required for the TV display. The application of Charge Coupled Devices (CCD) with a line-addressable structure is attractive. This structure corresponds to the line-scan orientation of sensing and display.

For the video quick look system a 128-kbit image memory has been composed from 16-kbit dynamic CCD's.

The color coding circuitry has been developed in co-operation with the Technological University of Twente.

2. SYSTEM DESCRIPTION

The functional blockdiagram of the video quick look system is shown in figure 2. The modules of the system are: (i) the input handling, (ii) the CCD image memory, (iii) the color coding, and (iv) the presentation on color TV display.

(i) Input handling

The input section performs the signal conditioning and the analog-to-digital conversion of the analog recorded IR signals. This section also has an electronic zoom facility which determines the interval of sampling and the sampling frequency.

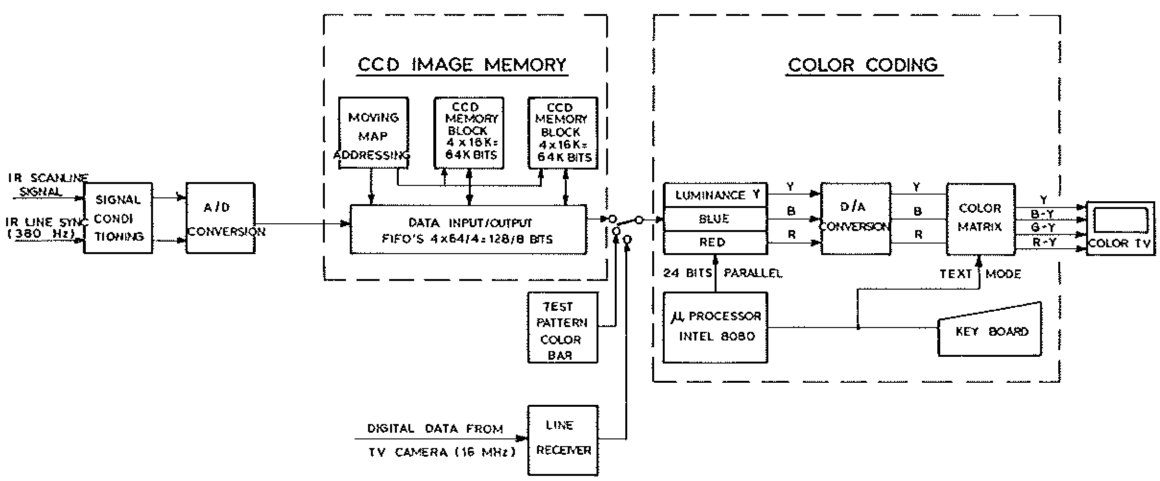


Figure 2. System blockdiagram of the video quick look

The resulting change in the spatial resolution in cross-track direction requires an equivalent change in the number of IR lines on display. This is to balance the resolution in cross-track and flight direction.

(ii) CCD image memory

The CCD image memory accepts digitized IR lines with a line frequency of 380 Hz. A selected IR image consisting of a sequence of 128 scanlines can be stored in the memory and is available for display without time limit. A real-time playback of the flight with the IR scanner is possible using the moving-map addressing of the CCD memory. The CCD image memory will be described in Section 3 in more detail.

(iii) Color coding

The color coding of pixel points is performed by means of look-up tables. The look-up tables are stored in fast random-access memories under control of the microprocessor. In this way the gray value of a pixel is translated into three separated values: luminance Y, blue B and red R. These digital values are converted into analog signals. The color matrix takes care of the transformation into luminance and color difference signals acceptable for the TV display.

Using the "text mode" three color tables can be stored, each color table containing 17 decimal values. The color-coding circuitry performs a linear interpolation between the selected color values. The decimal values of the color coding are shown on the TV display. The resulting color codes for each of the possible pixel values are made visible by means of a test pattern which generates a color bar on the display.

(iv) Presentation on color TV display

The resolution on display is determined by the 128*128 pixel presentation. It is realized by 128 pixels per TV line and 2 TV lines per IR scanline for one TV raster of 312.5 or 312 TV lines. This technique is compatible with the standard TV signal in 625 line format or in a special 624 line format. The IR images are displayed from TV line 1 to 512 included the interleaving. The color bar, generated by a testpattern, is displayed from TV line 512, thus at the foot of the picture. This color bar is available together with the IR image and can be used for calibration purposes.

3. THE CCD IMAGE MEMORY

The design of the CCD image memory is given in figure 3. The CCD image memory consists of three segments: (i) the CCD memory structure, (ii) the moving-map address circuitry, and (iii) the data input/output control.

(i) CCD memory structure

The 128-kbit memory consists of 8 Charged Coupled Devices (CCD), type Fairchild CCD461. These CCD's are dynamic line addressable RAM (LARAM) memories, each with 16-kbit memory. The CCD 461 has a 10 msec refresh period at an ambient temperature of + 55 °C. The operating frequency is 2.5 MHz and the power demand is less than 200 mW. The CCD contains four sections of 32 lines and each line has a length of 128 bits. The sections have a separate 1-of-32 decoding matrix, recirculating loop and data input/output circuits.

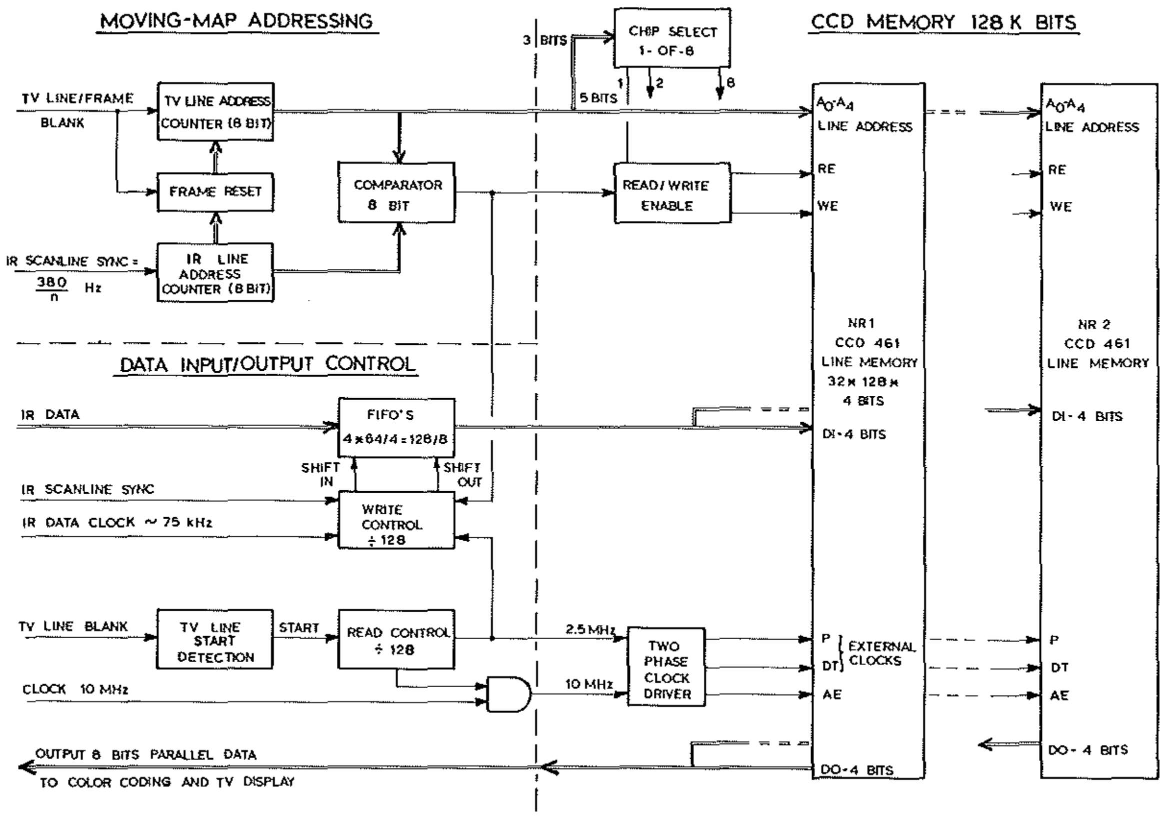


Figure 3. Design of the CCD image memory

This means that the CCD is organized as 32 serial shift registers with 4-bit data in/out and a length of 128 data points. Common to all sections are the external clocks, the control signals and the addresses (A0–A4). The external clocks are Precharge (P) and Data Transfer (DT); the control signals are Address Enable (AE), Read Enable ($\overline{RE}$), and Write Enable ($\overline{WE}$).

The required 128*128-pixel format on display permits a straightforward use of the CCD line structure. The 128 lines on display are composed of 4 CCD's activated by the "chip select" decoder. The pixel value of 8 bits is attained by the parallel operation of 2 blocks of 4 CCD's.

A two-phase clock driver has been developed for the required external clocks (Precharge and Data Transfer) and the Address Enable. The total capacitive loading on the 0 V–12 V drive inputs is about 1000 pF.

The CCD line addressing operates on the TV line frequency of 15.625 kHz. Most of the time the data in the addressed lines are recirculated and refreshed.

In the Read mode, the data of the addressed line appears at the output with a data rate of 2.5 MHz. In the Write mode, the new 128 datawords are stored in the addressed line.

(ii) Moving-map address circuitry

The contents of the TV line address counter is updated at the TV line rate of 15.625 kHz. The contents determines the Read mode for the addressed CCD register. The roll-stabilized synchronization signal of the IR scanline continuously updates the contents of the IR line address counter. The IR line sync has a low frequency of 380/n Hz, where n is the line reduction factor.

The Write mode is activated when the addressed CCD register corresponds to the contents of the IR line address counter.

The moving-map addressing is present when the contents of the TV line address counter at the start of a new TV frame is given by the current value of the IR line address counter. This mechanism is outlined in figure 4. A "picture freeze" is simply realized by disconnecting the IR sync signal.

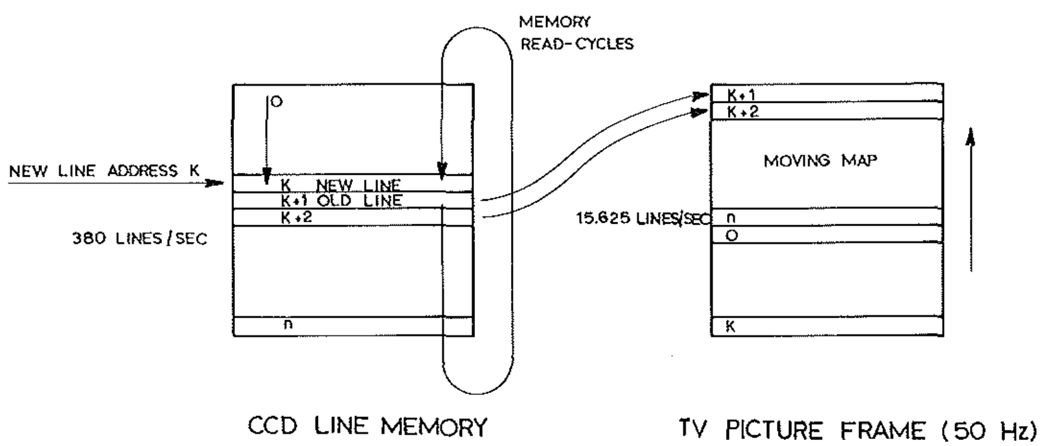


Figure 4. Moving-map display

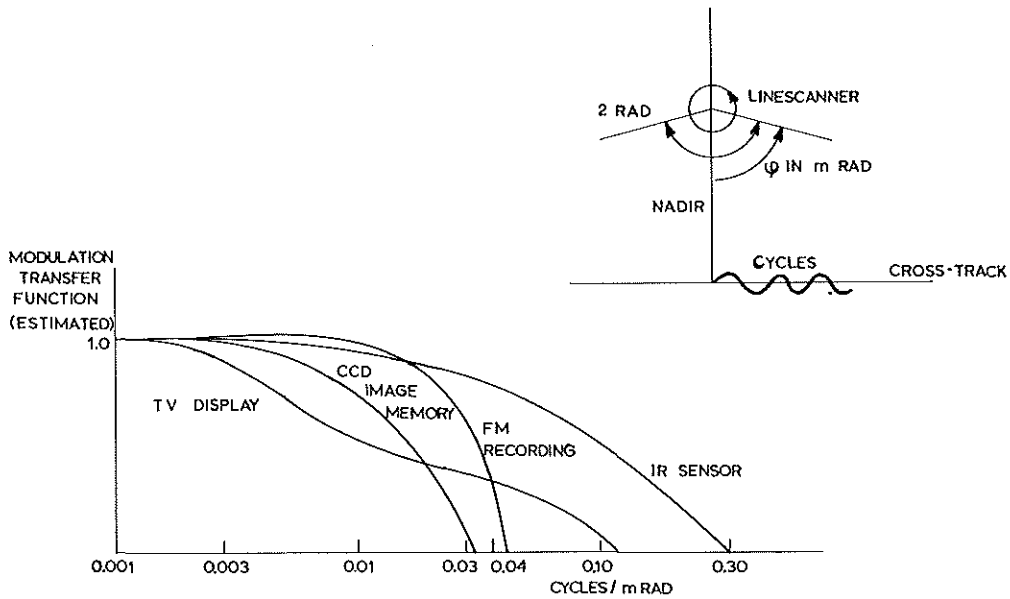
(iii) Data input/output control

The CCD memory continuously operates at the standard TV line frequency with a pixel rate of 2.5 MHz. The conversion of the IR scan-lines with a relatively low frequency to the TV line frequency requires a line buffer memory accepting a wide range of input/output data rates. FIFO line buffers with a register of 64*4 bits and maximum operating speed of 10 MHz have been selected. Shift-out of the IR line data of 128 pixels is activated by the address circuitry. Transfer of these data to the addressed line of the CCD memory occurs at the 2.5 MHz data rate.

The advantage of this design of the CCD image memory is that the support circuitry can be kept limited. Only three printed circuit boards (Euroformat: size 10*16 cm^2) have been required: one print each for the two-phase clock driver, the address circuitry and the data input/output control. The present 128*128-pixel memory is constructed on two printed circuit boards. The design is made in a modular way, e.g. extension to a 256*256-pixel format on display will be possible.

4. SYSTEM RESOLUTION

The design of an electrooptical imaging system requires a careful analysis of the spatial resolution of the system (Ref. 2). The use of Charged Coupled Devices introduces a two-dimensional sampling process, which in the flight direction is performed by the line-scan mechanism and in the cross-track by means of digitizing into picture elements. The system resolution can be analyzed using the Modulation Transfer Function Technique.



System Component	Characteristic	Estimated Resolution $(\frac{cycles}{mrad})$
Sensor	Instantaneous Field of View(IFOV)	0.3
Magnetic Recording	FM:Bandwidth DC to 40 kHz	0.04
CCD Image Memory	Pixels per addressed line: 128	0.03
TV Display	Horizontal line response	~0.15

Figure 5. Estimated resolution in cross-track of system components

The MTF describes the sine wave response of the system components or the overall system. Figure 5 gives a survey of the estimated resolution in cross-track of the system components. In this case the system components are the (i) Reconofax IR line scanner with a scanfrequency of 380 Hz and an IFOV of 3 mrad, (ii) FM analog recording, (iii) CCD image memory determining the pixel format on display, (iv) spatial frequency response on the TV display. The survey of figure 5 shows that the recording and the memory format are the limiting factor in the system. It can be shown that this is also the case in the resolution in the flight direction. Therefore, the aim of further investigations will be improving the recording method (PCM high-density recording) and expanding the CCD image memory.

5. RESULTS

Flight 1191 has been carried out to investigate the cooling-water discharge near a power station in the North Sea coastal area. For this flight the NLR laboratory aircraft has been equipped with the Reconofax infrared scanner. Figure 6 shows the flight tracks over the North Sea area near the power station (Maasvlakte).

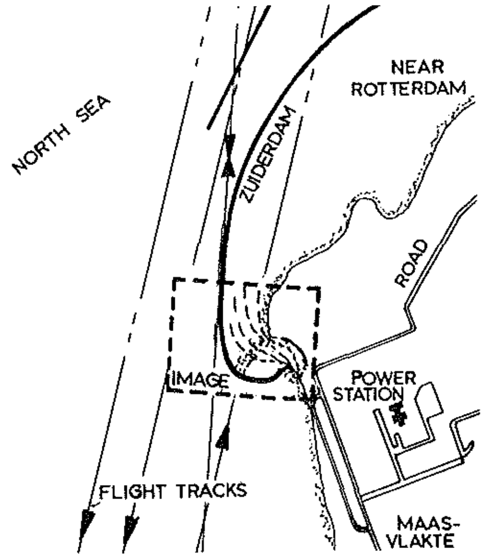


Figure 6. Flight tracks over the North Sea area near the power station - Maasvlakte. Flight 1191 - Project Rijkswaterstaat.

Figure 7 gives an example of the color-coded image on TV display.

Unfortunately, time did not permit the inclusion of color.

Figure 7. Color-coded image on TV display of the thermal infrared radiation pattern.

This image in the thermal infrared has been recorded by remote sensing the square area indicated in figure 6. The flight altitude of 300 meters results for this system in a spatial resolution with $5 \times 5\ m^2$ pixels. The accuracy of the infrared scanner is 0.1 ^{o}C and the recorded range of temperatures is 8 ^{o}C (relative). This temperature range corresponds to the color bar which is available for calibration purposes.

6. CONCLUSIONS

The application of line-addressable CCD's is straightforward in the case of a system with a linescan orientation of sensing and display. The CCD's are organized as serial shift registers operating at video rates. This organization involves a minimum of support circuitry required to operate the CCD image memory.

7. REFERENCES

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