Radiation Tolerance Constraints on CCD Application

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Abstract

Charge-coupled devices have been shown to be sensitive to both neutron and ionizing radiation effects. They are also very susceptible to transient radiation induced loss of stored information. Unhardened devices are usually severely degraded for doses greater than 5×10^4 rads (Si). A total ionizing dose radiation hard technology has been developed which enables the devices to tolerate 10^6 rads (Si). CCD use in 77°K radiation environments, in common with all MOS devices, is presently severely restricted due to accelerated oxide charge buildup during irradiation. The neutron induced degradation of transfer efficiency in surface channel CCD's is typically more than an order of magnitude smaller than that observed in buried channel structures.

Introduction

Charge-Coupled Devices (CCD's) have potentially extensive applications in optical imaging, signal processing, and serial memories. They have small size, low power consumption, and high reliability. Such characteristics make CCD's attractive for certain space and military missions provided the devices can satisfy the radiation hardness requirements. The CCD radiation tolerance required will of course be dependent on the radiation environment and the amount of shielding available. An unshielded device in certain earth orbits can receive a dose in excess of 10^6 rads (Si) per year from electrons and protons trapped in the Van Allen Belts. Nuclear weapons environments may subject a device to neutron fluences in the 10^{11} to $10^{13} n/cm^2$ (1 MeV equivalent) range and gamma ray doses from 10^4 to 10^6 rads (Si).

The purpose of this paper is to aid the systems design engineer by providing information concerning the nature and magnitude of radiation induced degradation of CCD parameters. In addition, techniques for obtaining the maximum dose tolerance from a given device structure are presented along with the optimized CCD structural design for radiation environments. The increased total ionizing dose tolerance of CCD's fabricated with a radiation hard oxide is described and the more rapid positive charge build-up in silicon dioxide during 77°K irradiation is discussed.

Radiation Effects in Semiconductor Devices

The basic effects of radiation on semiconductor devices have been described by Gregory.(1) The salient features of that review will be briefly outlined here as a background for the discussion of expected radiation effects in CCD's.

High energy radiation deposits energy in semiconductor materials via two mechanisms, atomic collisions and electronic ionization. The relative importance of these two mechanisms depends both on the type of radiation and the nature of the device. Electrons, protons, and gamma rays deposit most of their energy via the ionization process, while fast neutrons deposit up to 50% of their energy in atomic displacement damage. MOS devices are more sensitive to ionizing radiation (surface damage), while the characteristics of bulk-effect devices such as bipolar transistors, are usually degraded by displacement damage. However, CCD's

are sensitive to both surface and bulk displacement damage effects. They are also very susceptible to transient-radiation induced loss of stored information.

Numerous studies have shown that ionizing radiation causes failure of MOSFET devices due to two mechanisms: 1) trapped charge buildup in the silicon dioxide layer and 2) an increase in the density of trapping states at the silicon-silicon dioxide interface. Ionizing radiation generates electron-hole pairs in the silicon dioxide. The electrons are swept out of the oxide but some of the holes are trapped permanently producing a negative threshold voltage shift. The size of the threshold voltage shift varies with the magnitude and polarity of the applied gate bias during irradiation. Positive gate-substrate bias results in a greater threshold voltage shift since the holes are trapped near the silicon surface where they will exert maximum influence on the semiconductor. The absolute magnitude of the oxide charge and interface state buildup is also greatly dependent on the details of the fabrication process.

In addition to these permanent degradation mechanisms, ionizing radiation produces electron-hole pairs in the silicon substrate during irradiation. Carriers produced in device depletion regions, or within a diffusion length of these regions, can produce photocurrent at the device terminals. These photocurrents can cause large transients in linear circuits, and can cause error in the information stored by logic circuits.

Fast neutron irradiation produces displacement damage in the silicon which leads to significant decreases in carrier concentration, carrier mobility, and minority carrier lifetime. Decrease in carrier concentration and minority carrier lifetime reduction are the dominant failure mechanisms in most neutron irradiated bulk semiconductor devices. Mobility degradation does not become severe in silicon until neutron fluence exceeds 10^{15} neutrons/cm^2.

Surface Damage Effects

Since CCD's are MOS devices, ionizing radiation causes a buildup of positive space charge in the gate oxide and an increase in trapping states at the silicon-silicon dioxide interface. The resulting negative flat-band voltage shift changes the CCD operating bias while the interface state density increase reduces the charge transfer inefficiency in surface channel devices and increases the dark current density in both surface and buried channel structures. Consequently, non-hardened devices are unsuitable for most room temperature applications requiring a dose tolerance greater than 5×10^4 rads (Si). The details of these radiation induced failure mechanisms are presented in the following paragraphs.

Charge Buildup in the Oxide

For a given oxide technology, the smallest flatband voltage shifts are observed in n-buried channel and p-surface devices since the gate voltage in these structures is negative with respect to the channel potential. The effects of positive space charge buildup in the oxide on CCD operation will be discussed separately for the CCD input, charge transfer section and the output of the CCD shift register shown in Figure 1.

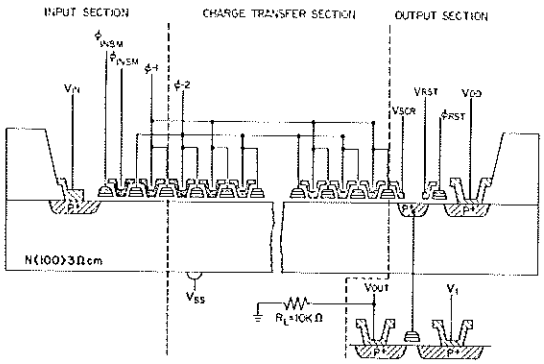

Fig. 1 Cross-section of a two phase p-surface channel CCD shift register. The device is shown separated into three sections: input, charge transfer section, and output.

The CCD input structure is the most radiation sensitive section of the device unless a threshold insensitive input is employed. MOSFET input techniques such as dynamic injection[2] which operate by leaking charge into a CCD potential well over the barrier formed by the input

transfer gates, ϕ_{INBM} and ϕ_{INSM}, typically tolerate only 10^3 rads (Si) before requiring adjustment. However, threshold voltage shifts up to -5 volts have been accomodated by the input structure when the potential equilibration input, a threshold insensitive technique, was employed.(3)

The charge transfer process in a properly designed charge-coupled shift register is fairly insensitive to uniform transfer gate flatband voltage shifts.(4) However, gate to gate nonuniformities of the space charge buildup may distort the potential profile in the CCD channel with increased signal charge trapping as a result.

Unequal flatband voltage shifts on adjacent gates has also lead to severe loss in CCD signal handling capacity.(5) The difference in flatband voltage shifts between the aluminum and polysilicon CCD gates, shown in Figure 2, reduced the full well capacity to 20% of the irradiation value after $3x10^5$ rad (Si).

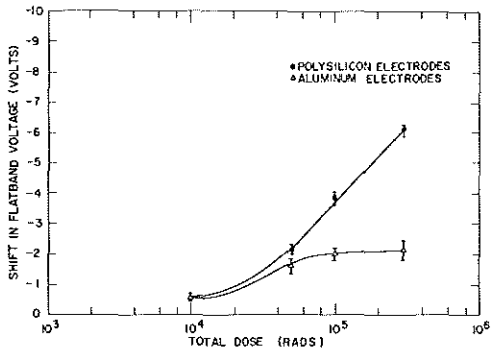

Fig. 2 Difference in flatband voltage shift for polysilicon (1,000 A° oxide) and aluminum (2,400 A° oxide) CCD gates as a function of total dose.

The radiation induced negative flatband voltage shift will cause the potential energy profile in the CCD channel to change in both surface and buried channel structures. Eventually the channel will be driven out of depletion in p-surface and n-buried channel devices. A few volts of flatband voltage shift accomodation can be obtained in an n-buried channel structure simply by applying a reverse bias to the reset drain voltage, V_{DD}, several volts in excess of the pre-irradiation value required to deplete the channel. The flatband voltage shift tolerance of a p-surface channel device can be increased by either applying a positive substrate bias or a negative clock offset voltage.

The CCD output is the least radiation sensitive section of the device. The input and charge transfer sections will usually be severely degraded before the output becomes inoperable. The reduced radiation sensitivity of the CCD output can be attributed to the following: (1) The output MOSFET threshold voltage shift is smaller than the shift on the other CCD gates due to the reduced electric field strength in that oxide. (2) The output signal is AC coupled. Hence, small shifts in the DC operating point of the output transistor are of little consequence. (3) The output MOSFET is operated as a source follower. Therefore, the output gain will be relatively insensitive to radiation induced change of the transconductance.

Interface State Density Increase

The irradiation produced increase of trapping states at the silicon-silicon dioxide interface reduces the charge transfer efficiency in surface channel devices and increases the surface component of the dark current density in both surface and buried channel CCD structures. The increase in charge transfer inefficiency due to interface state trapping in surface channel devices renders them unsuitable for most applications after 10^5 rads (Si). Surface state trapping effects do not occur in a buried channel since the charge packet is transferred in the bulk of the silicon rather than at the silicon-silicon dioxide interface. A comparison of the transfer inefficiency as a function of dose for surface and buried channel devices is shown in Figure 3.(6) The small degradation of the transfer efficiency observed in the buried channel device after large doses is probably due to gamma induced bulk trapping effects.

Interface states also act as generation recombination centers for the surface component of the dark current. The linear relation between the dark current and the interface state density for an irradiated device is illustrated in Figure 4.(4)

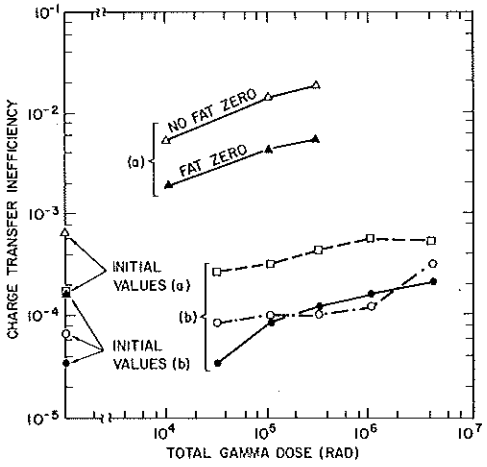

Fig. 3 Charge transfer inefficiency as a function of total gamma dose (a) for surface channel CCD's, (b) for buried-channel CCD's, illustrating the larger degradation observed in surface channel devices after ionizing radiation.

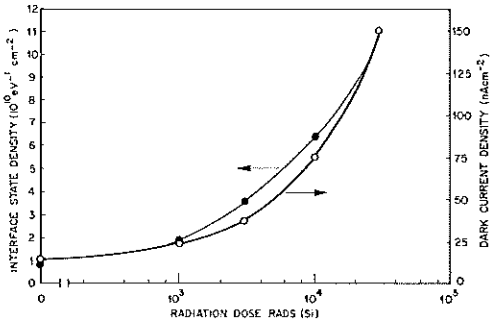

Fig. 4 Increase in interface state density and dark current density in a surface channel CCD as a function of dose. The data illustrate the linear relation between interface state density increase and dark current increase.

Dark current densities of 1,000nA/cm^2 have been measured after 10^6 rads in devices having a pre-irradiation value of 2nA/cm^2. Increases of this magnitude usually prohibit room temperature applications of unhardened devices after doses of 10^5 rads (Si).(6)

Transient Ionization Effects

Charge-coupled devices are extremely sensitive to transient-radiation induced loss of stored information since they are very sensitive photosensors. The CCD potential wells are observed to fill with charge after a radiation pulse which deposits a dose on the order of one rad (Si) in a period which is smaller than the time a given potential well exists in the silicon.(7) The well saturation dose can be increased approximately an order of magnitude by reducing the thickness of the collection volume associated with each CCD bit.

In some applications the amount of time required to recover normal device operation after a radiation pulse is important. It has been observed that the excess charge generated in a CCD is removed at a rate which is a function of the CCD clock frequency, f_c, for a given dose.(8) Additional analysis indicates a recovery time dependence on CCD well capacity, N_{FW}, since the quantity of charge carriers transported out of a CCD during a clock period is limited by the well capacity. Hence, the CCD recovery time, T_R, after a pulse of ionizing radiation can be approximated by

$$T_R \simeq \frac{g_\gamma V_{coll}}{N_{FW} f_c}$$

where V_{coll} is the collection volume of one CCD bit and g_γ is the electron-hole pair generation rate constant for ionizing radiation in silicon.

Bulk Damage Effects

Fast neutrons create bulk trapping centers in silicon which cause a decrease in transfer efficiency primarily in buried channel devices and an increase in bulk component of the dark current density in both surface and buried channel structures. Increased trapping effects in neutron irradiated n-buried channel CCD's are usually insignificant for fluences less than 10^{11}n/cm^2 ($\sim$ 15 MeV average).(9) The linear transfer inefficiency increase in the 10^{11} to 10^{13}n/cm^2 fluence range is shown in Figure 5. After 10^{13}n/cm^2 ($\sim$ 15 MeV average) the transfer efficiency at 295°K was reduced to 0.992, making the devices unsuitable for most applications. The degradation observed after 15 MeV neutron bombardment is expected to be 2.5 to 3 times greater than the value for a

1 MeV equivalent neutron fluence.[10]

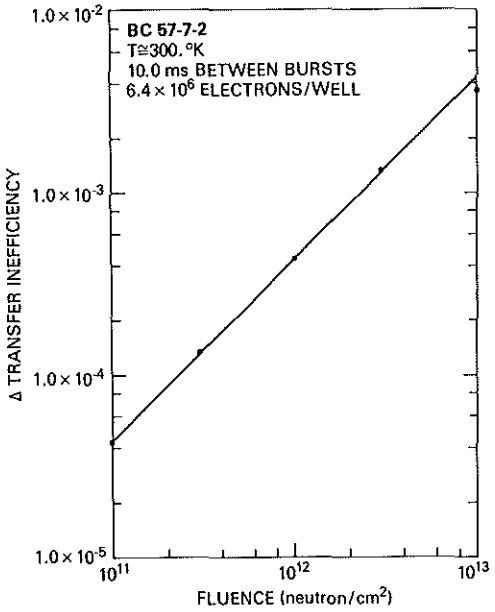

Fig. 5 Change in transfer inefficiency at 300°K as a function of 15 MeV (average) neutron fluence, illustrating the linear relation between the increase in transfer inefficiency due to bulk trapping and the neutron fluence.

Bulk traps are created during neutron bombardment in both surface and buried channel CCD structures. However, the volume occupied by a charge packet in a surface channel device is more than an order of magnitude smaller than the volume in a buried channel structure. Consequently, the transfer efficiency in a surface channel is less sensitive to increases in bulk trap density since the charge packets interact with fewer bulk traps. See Figure 6.[6]

Neutron irradiation produces several trapping levels of unequal density in silicon. Three distinct trap levels have been observed from 77°K to 300°K by use of the double pulse technique.[11] The energy level, (E_c-E_t), and the creation rate, $(\frac{\Delta N_t}{\Delta \phi})$, of the bulk traps are given in Table I. Similar trapping levels have been observed in other types of irradiated silicon devices.[12]

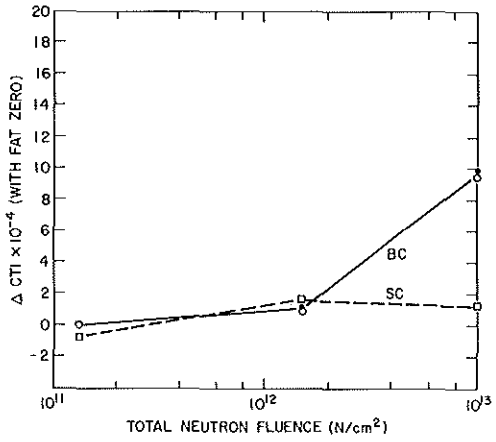

Fig. 6 Change in charge transfer inefficiency (CTI) with neutron fluence (1 MeV equivalent) for typical surface and buried-channel CCD's.

TABLE I

Bulk Trap Energy Levels and Creation Rates (15 MeV Neutron)

Level	(E_c-E_t) eV	$\Delta N_t/\Delta\phi$ cm^{-1}
N-1	0.14	1.1
N-2	0.23	~ 0.8
N-3	0.41	7.0

The bulk trap level located near mid gap, E_c-E_t = 0.41 eV, acts as a bulk recombination generation center for dark current in both surface and buried channel devices. An approximate linear increase in dark current density in the 10^{11} to 10^{13} n/cm^2 range is shown in Figure 7 for an n-buried channel device.[9] The surface component of the dark current density did not increase since the total dose equivalence of the $10^{13}n/cm^2$ fluence was only approximately 10^4 rads (Si).[13]

While 50% of the fast neutron energy is deposited in silicon via displacement damage, the fraction for gamma rays is much smaller. The bulk trap creation rate

for 1 MeV photon per cm^2 is only $1x10^{-3}$ cm^{-1}.[14] Hence, bulk damage effects due to gamma irradiation are not significant for doses less than 10^6 rads (Si) ($2x10^{15}$ 1 MeV gammas/cm^2). The carrier removal rates for 1.7 MeV electrons is in the 0.2 to 1.0 cm^{-1} range.[15]

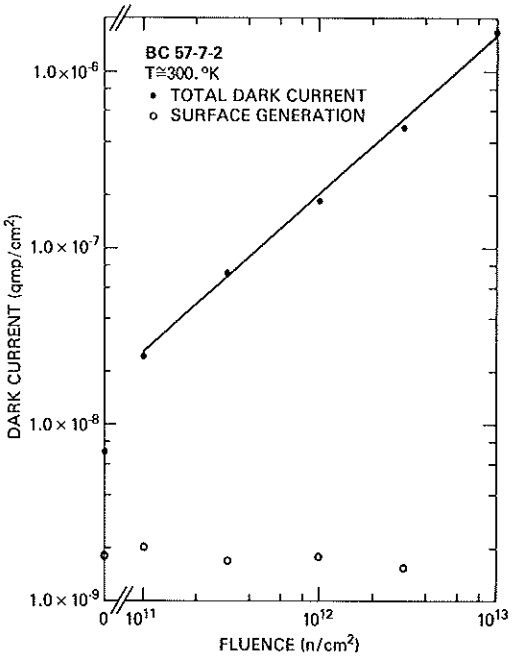

Fig. 7 Dark current density at 300°K as a function of neutron fluence, illustrating the linear relation between J_D and neutron fluence.

Little progress has been made in the area of neutron hardening of buried channel CCD's. An obvious technique would be to fabricate a thinner but more heavily doped buried channel so that the signal charge packet would interact with a small number of bulk traps, thereby reducing the transfer efficiency degradation. Another approach would be to fabricate the devices on Czochralski wafers since the neutron damage in oxygen rich silicon is smaller than the damage in float zone material.

CCD Surface Damage Hardening

Structural Optimization

The earliest work on total dose irradiation effects in CCD's identified the major failure mechanisms peculiar to several device structures so that the optimum design for total dose radiation hard CCD's could be determined.[4] In particular it was found that:

1. A buried channel structure should be used. The charge transfer efficiency in a buried channel device, contrary to surface channel CCD's, is not degraded by an increase in the interface state trap density after irradiation.

2. An n-buried channel CCD structure is preferred. The flat-band voltage shift for a given oxide structure during irradiation is minimized when the gate electrodes are negative with respect to the channel potential.

3. The n-buried channel CCD output diode should be capable of being reversed biased to a voltage which will allow the channel to remain depleted after irradiation. The negative flat-band voltage shift in an n-buried channel structure causes the buried channel to be driven out of depletion. A few volts of flat-band shift can be automatically accommodated by biasing the output diode to a value several volts in excess of pre-irradiation bias required to deplete the buried channel.

4. The design should use a planar channel insulator (no stepped oxide) and only one type of electrode material. This is necessary to eliminate differences in the flatband voltage shift under adjacent electrodes, since such differences can reduce or eliminate potential barriers which can result in reduced well capacity and increased charge transfer inefficiency.

5. The use of undoped polysilicon for interelectrode isolation should be avoided. Experience on two different types of device has shown that total doses of 1 to $3x10^4$ rads (Si) cause channeling in the isolation regions with resulting deterioration in device performance.

6. The input structure should be compatible with the operation of a threshold insensitive input technique.

Hard Oxide Technology

Structural optimization alone is not sufficient to enable CCD's fabricated using standard gate oxide techniques to

satisfy the total dose radiation requirements for most space and strategic applications. The approach taken in the development of a radiation hard insulator for CCD's was to modify the process used in the fabrication of radiation hard CMOS devices.[16,17]

Both p-surface and n-buried channel shift registers have been fabricated using the CCD hard oxide process.[18] These devices can be operated after 10^6 rads (Si) with the pre-irradiation clock and bias voltages. The post-irradiation values for the n-buried channel device parameters, listed in Table II, are acceptable for most radiation environment applications.

TABLE II

Radiation Hard n-Buried Channel CCD Parameters

	Pre-Irradiation	$1x10^6$ rads (Si)
CTE	0.99999	0.9999
J_D	$5nA/cm^2$	$140nA/cm^2$
Well capacity	$3x10^6$ e^-	$2.25x10^6e^-$
Threshold shift	-	-1.8V

The transfer efficiency in surface channel devices fabricated with this radiation hard oxide was seriously degraded for doses greater than 10^5 rad (Si).[17] A severe increase in interface state trapping required the use of a 50% bias charge to obtain a transfer efficiency of 0.992 after 10^6 rads (Si). The dark current density and threshold voltage shift after 10^6 rads (Si) were approximately equal to the values observed in the buried channel structure.

It should be noted that the pyrogenic CCD hard oxide process described above is insensitive to total dose radiation effects only for negative gate to channel bias (i.e., p-surface channel and n-buried channel). The flatband shift for positive gate to channel bias can be quite large.

Bulk silicon damage effects in neutron irradiated radiation hard devices do not differ from those in unhardened structures.

Irradiation Effects at Cryogenic Temperatures

CCD's are being considered for use in space and infrared imaging systems both as infrared detectors and as signal processors for IR focal plane arrays at low-temperatures. However, several studies have shown that charge build-up in SiO_2 is more rapid in devices irradiated at low-temperatures.[19,20] Large flatband voltage shifts, are also observed during 77°K irradiation, in oxides which are radiation hard at room temperature.[21] The increased charge trapping effects at low-temperatures in the CCD radiation hard oxide, shown in Figure 8, make these devices unsuitable for most 77°K applications after a dose of $5x10^4$ rads (Si).[22] Several techniques (alternate insulators, metal nitride oxide structures, and aluminum implanted oxides)[23] have been suggested for improving the low-temperature radiation behavior of MIS structures, but their use in CCD fabrication has not been reported.

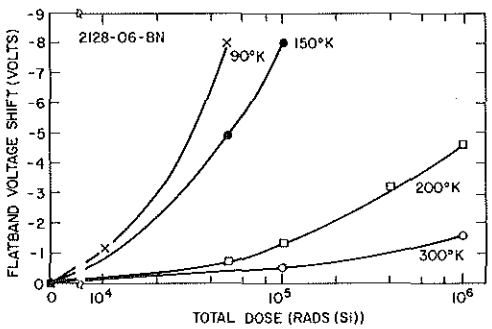

Fig. 8 Flatband voltage shift for the CCD radiation hard oxide as a function of dose at several temperatures, illustrating the increased oxide charge trapping effects at low-temperatures.

The holes generated in the oxide during a liquid nitrogen temperature irradiation are trapped almost immediately producing a nearly uniform density of positive charge in the oxide. The resultant flatband voltage shift is proportional to the oxide thickness squared and has a value of -2.0V per 10^4 rad (Si) for a 1,000 A° oxide if all the generated holes are trapped uniformly.[24] The fraction of the

holes trapped is independent of gate voltage polarity for small doses but is a function of the electric field strength in the oxide.[25]

Several techniques have been employed to anneal the excess flatband voltage shift observed in devices irradiated at low-temperatures. These include: photo-depopulation of the traps, field-aided emission of holes from traps and thermal annealing.[26] Room temperature radiation hard oxides show some recovery even at 85°K but the annealing process is accelerated at temperatures greater than 125°K.[27]

The excess low-temperature irradiation threshold voltage shift observed in the room temperature radiation hard CCD was annealed by warming the device to room temperature. After recooling to 85°K the CCD threshold voltage shift was approximately equal to the shift which would have been observed if the devices had been irradiated at 300°K and then cooled. The input gate threshold voltage shift for several irradiation-anneal cycles is shown in Fig. 9. Normal CCD clock and bias voltages were applied to the device during the irradiation-annealing sequence. The residual shift at liquid nitrogen temperatures increased to -0.5V after 1.3×10^5 rads as expected from 300°K irradiation results. A residual shift of ~ -5 volts might be expected for a typical non-hardened oxide subjected to the same irradiation-annealing cycle.

The flatband voltage shift in the CCD hard oxide during irradiation at 4.2°K has recently been found to be identical to the shift for 77°K irradiation.[28] Also, it has been shown that the MNOS approach offers considerable improvement in the radiation hardness of capacitors irradiated at 77°K.[29] This technique may be useful for radiation hard devices at 4.2°K.

The limited amount of experimental data available suggest that the permanent bulk silicon damage caused by fast neutrons in CCD's irradiated at 80°K and 294°K is similar.[9] The density and the energy of the N-1 bulk trap level created by the neutron bombardment was independent of irradiation temperature (80°K or 294°K) and irradiation bias for the particular devices tested. However, the transfer inefficiency in a buried channel device will change as the temperature is varied since the particular bulk levels responsible for signal charge trapping is a function of temperature. At 80°K the bulk level (N-1) dominating the transfer loss has an order of magnitude lower density than the level important for trapping at 300°K (N-3). Hence, the charge transfer inefficiency at 80°K after neutron irradiation is approximately an order of magnitude smaller than the values for 300°K that are shown in Fig. 5.

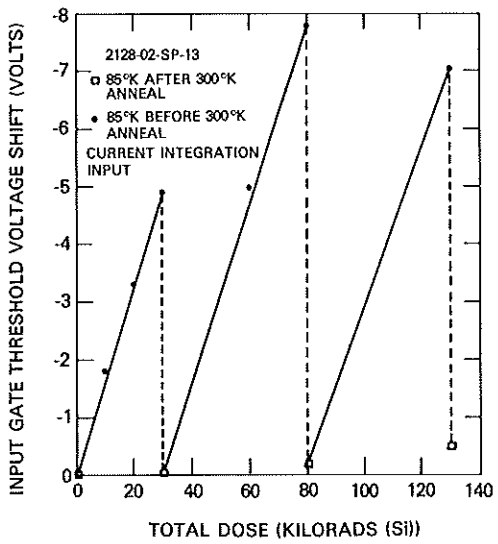

Fig. 9 Room temperature radiation hard CCD input gate threshold voltage shift at 85°K as a function of dose and 300°K annealing.

Summary

The previous sections of this paper have presented an overview of the current state-of-the-art of radiation effects and hardening techniques. The key points presented are listed below.

1. CCD's are sensitive to both surface and bulk damage effects due to radiation. Devices fabricated using standard commercial gate oxide technologies are unable to satisfy the total dose requirements for most space and strategic requirements.

2. An n-buried channel device is the least radiation sensitive structure for total ionizing dose effects.

3. The neutron induced degradation of the charge transfer efficiency is greater in buried channel devices than in surface channel devices.

4. Only a limited increase in the total dose radiation tolerance of CCD's can be achieved by means of structural and operational considerations alone. A radiation hard oxide technology is required to satisfy system radiation requirements.

5. CCD's are extremely sensitive to transient upset effects. Increased tolerance can be achieved by thinning. Device burnout is prevented by current limiting the power supplies.

6. An megarad-hardened n-buried channel hard CCD technology has been developed and simple linear radiation hard shift registers have been fabricated with the optimized structure.

7. Total ionizing dose effects are more severe for irradiation at 77°K. Ordinary room temperature radiation hardening techniques do not apply for irradiation at liquid nitrogen temperatures. However, several techniques have been proposed to solve this problem.

8. The degradation of CCD parameters in neutron irradiated buried channel CCD's are less severe at 77°K than at 300°K.

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References

1. B. L. Gregory and C. W. Gwyn, "Radiation Effects on Semiconductor Devices," Proc. IEEE 62, 1264 (1974).

2. C. H. Sequin, and A. M. Mohsen, "Linearity of Electrical Charge Injection into Charge-Coupled Devices," IEEE J. Solid-State Circuits, SC-10, 81 (1975).

3. J. M. Killiany and W. D. Baker, "Limitations of a Threshold Insensitive CCD Input Technique in a Total Dose Radiation Environment," Proc. International Conf. on the Appl. of CCD's, 369 (1975).

4. J. M. Killiany, W. D. Baker, N. S. Saks, and D. F. Barbe, "Effects of Ionizing Radiation on Charge-Coupled Device Structures," IEEE Trans. Nuc. Sci., NS-21, No. 6, 193 (1974).

5. D. F. Barbe, J. M. Killiany, and H. L. Hughes, "Effects of Gamma Radiation in Charge-Coupled Devices," Appl. Phys. Lett., 23, 400 (1973).

6. G. A. Hartsell, "Radiation Hardness of Surface and Buried Channel CCD's," Proc. International Conf. on the Appl. of CCD's, 375 (1975).

7. R. A. Williams, and R. D. Nelson, "Radiation Effects on Charge-Coupled Devices," IEEE Trans. Nuclear Science NS-22, pp. 2639-2644, (1975).

8. W. Shedd and B. Buchanan, "Transient Radiation Effects in CCD's," IEEE Trans. Nuc. Sci. NS-23, 1636 (1976).

9. N. S. Saks, J. M. Killiany, and W. D. Baker, "Effects of Neutron Irradiation on the Characteristics of a Buried Channel CCD at 80°K and 295°K," Proc. NASA-JPL Conf. CCD Tech. and Applications, Washington, D. C., Dec. 1976.

10. E. C. Smith, D. Binder, P. A. Compton, and R. I. Wilbur, "Theoretical and Experimental Determinations of Neutron Energy Deposition in Silicon," IEEE Trans. Nuc. Sci., NS-13, No. 6, 11 (1966).

11. N. S. Saks, "Investigation of Bulk Electron Traps Created by Fast Neutrons Irradiation in a Buried Channel CCD," IEEE Trans. Nuc. Sci. NS-24, 2153 (1977).

12. J. W. Walker and C. T. Sah, "Properties of 1.0 MeV Electron-Irradiated Defect Centers in Silicon," Phy. Rev. B, 7, p. 4587, May 1973.

13. R. A. Poll, "Electronic System Hardening Approaches", IEEE Trans. Nucl. Sci., NS-18, pp. 100-103, Dec. 1971.

14. O. L. Curtis, and J. R. Srour, "Recombination Within Disordered Regions: Influence of Barrier Height on Recombination Rate and Injection Level Effects", IEEE Trans. Nuc. Sci. NS-20, No. 6, 193 (1973).

15. H. J. Stein and R. Gereth, "Introduction Rates of Electrically Active Defects in n- and p-type Silicon by Electron and Neutron Irradiation, J. Appl. Phys. 31, 2890 (1968).

16. G. F. Derbenwick and B. L. Gregory, "Process Optimization of Radiation-Hardened CMOS Integrated Circuits," IEEE Trans. Nuc. Sci. NS-22, 2151, (1975).

17. C. P. Chang, "Radiation Hardened Surface Channel CCD's," IEEE Trans. Nuc. Sci. NS-23, 1639 (1976).

18. C. P. Chang, "Radiation Effects in N Buried Channel CCD's Fabricated with a Hardened Process," IEEE Trans. Nuc. Sci. NS-24, 2190 (1977).

19. R. L. Nielsen and D. K. Nichols, "Total Dose Effects of Ionizing Radiation on MOS Structures at 90°K", IEEE Nuc. Sci., NS-20, No. 6, 319 (1973).

20. R. C. Hughes, "Hole Mobility and Transport in Thin SiO_2 Films, Appl. Phys. Lett. 26, No. 8, (1975).

21. H. E. Boesch, Jr., F. B. McLean, J. M. McGarrity, G. A. Ausman, Jr., "Hole Transport and Charge Relaxation in Irradiated SiO_2 MOS Capacitors", IEEE Trans. Nuc. Sci., NS-22, 2163 (1975).

22. J. M. Killiany, "Low Temperature Radiation Damage Effects in a Room Temperature Radiation Hard Surface Channel CCD," IEEE Trans. Nuc. Sci., NS-24, 2194 (1977).

23. J. R. Srour, S. Othmer, O. L. Curtis, Jr., and K. Y. Chin, "Radiation-Induced Charge Transport and Charge Buildup in SiO_2 Films at Low Temperatures", IEEE Trans. Nuc. Sci. NS-23, 1513 (1976).

24. H. H. Sander and B. L. Gregory, "Unified Model of Damage Annealing in CMOS from Freeze-In to Transient Annealing", IEEE Trans. Nuc. Sci., NS-22, 2157 (1975).

25. J. R. Srour and K. Y. Chiu, "MOS Hardening Approaches for Low Temperature Applications," IEEE Trans. Nuc. Sci. NS-24, 2141 (1977).

26. E. Harari, S. Wang, and B.S.H. Royce, "Low Temperature Irradiation Effects in SiO_2 Insulated MIS Devices," J. Appl. Phys. 46, 1310 (1975).

27. F. B. McLean, H. E. Boesch, Jr., and J. M. McGarrity, "Hole Transport and Recovery Characteristics of SiO_2 Gate Insulators", IEEE Trans. Nuc. Sci., NS-23, 1506 (1976).

28. S. Othmer and J. R. Srour, "Charge Buildup in Irradiated SiO_2 Films at 4°K", presented at the IEEE Annual Conf. on Nuclear and Space Radiation Effects, Albuquerque, N. M., July 18-21, 1978.

29. N. S. Saks, "Response of MNOS Capacitors to Ionizing Radiation at 80°K," presented at the IEEE Annual Conf. on Nuclear and Space Radiation Effects, Albuquerque, N. M., July 18-21, 1978.