A CCD TWO DIMENSIONAL TRANSFORM

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ABSTRACT. The two-dimensional transform is recognized as a valuable tool for processing two dimensional signals. It has applications in bandwidth reduction systems, image enhancement systems, correlation trackers, seismic array processors, and radar and sonar systems. A 32 x 32 point discrete Fourier transform has been built using two low power CCD integrated circuits - a 32 point DFT IC and a 32 x 32 point reformatting CCD memory. The detailed design and operation of this two dimensional transform breadboard are described.

I. INTRODUCTION

Since the introduction of the charge-coupled device (CCD) in 1970[1], the CCD has become an important element for implementing many signal processing functions, one of which is spectral analysis via the chirp Z transform (CZT) algorithm.[2-3] This algorithm for obtaining the discrete Fourier transform (DFT) is ideally suited to CCD implementation as the bulk of the computation may be performed in CCD transversal filters. In 1977, a monolithic 32 point CCD DFT IC which implements the chirp Z transform algorithm was designed and fabricated.[4] With this chip a 32 point one-dimensional DFT may be obtained in 64 μs with a power dissipation of 600 mW. Although the one-dimensional DFT has many applications, there are a variety of applications which require the processing of two dimensional signals such as obtained from images, seismic arrays, and sonar and radar systems. The two-dimensional DFT may be realized via the one dimensional DFT by first transforming the rows of a two dimensional array and then transforming the columns of the resulting two dimensional array.[5] To implement this, the data output of the first transformation must be reformatted to become the input data for the second transformation. In 1978 a 32x 32 point corner turning memory (CTM) using a novel two dimensional charge transfer structure was designed and fabricated. This CCD CTM is ideally suited to perform the reformatting operation.

This paper describes the implementation of a 32 x 32 point two dimensional discrete Fourier transform using the 32 point CZT IC and the 32 x 32 point corner turning memory. Section II reviews how the two dimensional DFT may be implemented with one dimensional DFTs. Sections III and IV describe in detail the 32 point CCD CZT IC and the 32 x 32 point CCD corner turning memory. Section V presents the results of implementing the two dimensional DFT with these two CCD ICs.

II. THE TWO DIMENSIONAL DFT

The DFT of a finite area sequence f(m,n) is

$$F(k,\ell)=\sum_{m=o}^{M-1}\sum_{n=o}^{N-1} f(m,n)\, e^{-j2\pi\left(\frac{km}{M}+\frac{\ell n}{N}\right)} \qquad (1)$$

The two dimensional DFT can be interpreted in terms of the one dimensional DFT by expressing Equation (1) as

$$F(k,\ell)=\sum_{m=o}^{M-1} G(m,\ell)\, e^{-j2\pi\frac{km}{M}} \qquad (2)$$

where

$$G(m,\ell)=\sum_{n=o}^{N-1} f(m,n)\, e^{-j2\pi\frac{\ell n}{N}} \qquad (3)$$

The function G(m,ℓ) corresponds to an N-point one dimensional DFT for each value of m, i.e, it consists of M one dimensional transforms, one for each row of f(m,n). The two dimensional DFT F(k,ℓ) is then obtained by performing N one dimensional transforms, one for each column of the sequence G(m,ℓ). Thus, the two dimensional transform can be implemented as shown in Figure 1.

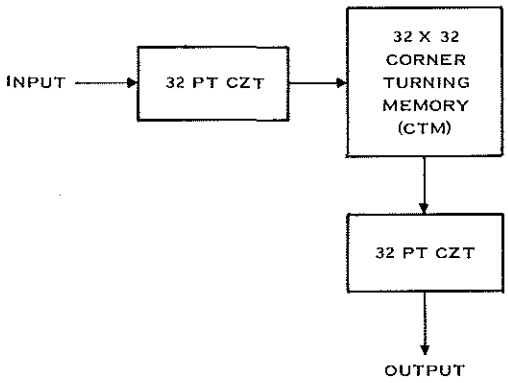


Figure 1. Implementation of Two Dimensional Discrete Fourier Transform.

A one dimensional transform is performed on the rows of the signal using a CCD CZT IC. The resulting complex Fourier coefficients are stored row by row in two CCD corner turning memories. Next these coefficients are read out column by column into a second CCD CZT IC which completes the calculations for the two dimensional transform.

III. 32 POINT CCD CZT IC

A monolithic 32 point DFT using the chirp Z transform algorithm has been designed and fabricated using an N channel, two level polysilicon coplanar electrode process. Goals of the design included the elimination of all external support components and operation of the transform IC at a 1 MHz data rate. Small size, low weight, low power, and high speed are achieved with total integration.

The chirp z transform algorithm is derived by starting with the definition of the discrete Fourier transform:

$$F_k = \sum_{n=o}^{N-1} f_n e^{-j\frac{2\pi kn}{N}} \qquad (4)$$

and making the substitution:

$$2nk = n^2 + k^2 - (n-k)^2 \qquad (5)$$

The chirp Z transform equation results:

$$F_k = e^{-j\frac{\pi k^2}{N}} \left[\sum_{n=o}^{N-1} \left(f_n e^{-j\frac{\pi n^2}{N}} \right) e^{j\frac{\pi (k-n)^2}{N}} \right] \qquad (6)$$

Equation 6 has been factored to emphasize the three operations which make up the CZT algorithm: (1) premultiplying the time signal with a chirp (linear FM) waveform, (2) filtering in a chirp convolution filter, and (3) postmultiplying the Fourier output by a chirp waveform. This is illustrated in Figure 2.

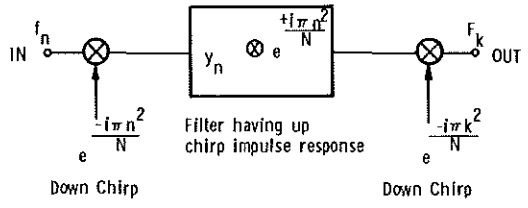


Figure 2. Schematic of Chirp Z Transform Algorithm.

The chirp Z transform IC is divided into two sections. The first section contains the multipliers which are implemented using multiplying digital-to-analog converters (MDACs). Analog input signals applied to the MDAC reference terminals are multiplied by binary coded chirp waveforms stored in a ROM. External digital inputs are provided to bypass the ROM for multiplicaton by other waveforms. Differential MDAC analog inputs, and uncommitted outputs allow maximum flexibility in total system configuration.

The second portion of the chip performs the chirp filtering operation. Four 63 stage transversal filters are needed to implement the complex chirp convoluton required by the CZT algorithm. The weighting coefficients for the sine and cosine chirp filters are:

$$h_k^{\cos} = \cos \frac{\pi k^2}{32} \qquad k = 0, 62$$

$$h_k^{\sin} = \sin \frac{\pi k^2}{32} \qquad k = 0, 62 \qquad (7)$$

The coefficients are realized using the split-electrode technique.[6] The CCD filters are two phase, coplanar electrode structures with ion implant wells.[7] Operational amplifiers provide differential inputs and outputs for the CCD filters, again for the purpose of versatility. In practice, the filters are loaded with 32 time domain data samples, and then the input is blanked while the convolution is performed. Thus, a single chip yields a DFT output with a 50% duty cycle. In this mode of operation, the 4 MDAC's provided can be multiplexed to do both pre- and post-multiplication. If 100% duty cycle output is required, two chips are used, and the 8 MDAC's included are sufficient for the needed multiplications.

All clock waveforms are generated on chip from a two phase master clock, and the system timing is such that it is possible to cascade CZT's for the purpose of multi-dimensional transforms, or for performing correlation by multiplication in the frequency domain.

A block diagram of the CZT chip is shown in Figure 3, and a photomicrograph of the IC is shown in Figure 4. The IC measures 6.04 x 5.69 mm^2 (238 x 224 mil^2). Details relating the performance of the 32 point CZT IC have been described elsewhere.[4]

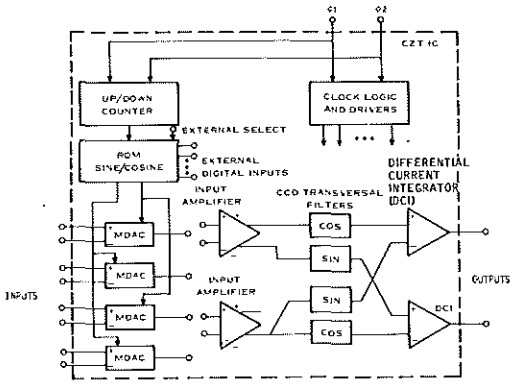


Figure 3. Block Diagram of 32 Point CCD CZT IC

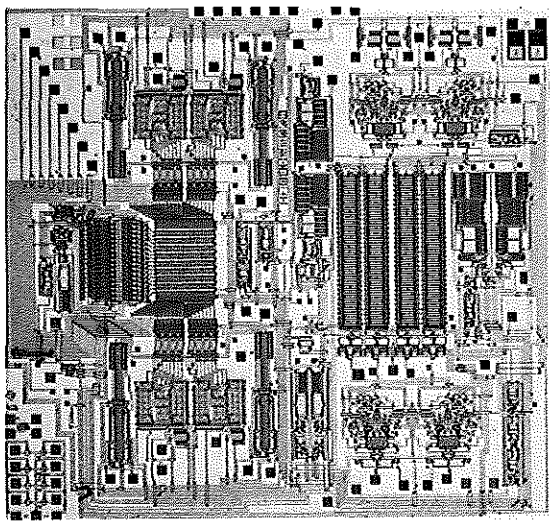


Figure 4. Photomicrograph of 32 Point CCD CZT IC.

IV. 32 X 32 CCD CTM

Analog CCD reformatting memories have been recently applied in high speed processors for pulse doppler radar in conjunction with surface acoustic wave device chirp transform units. [8-12] These memories are predominantly line-addressable CCD delay line structures which exhibit line-to-line offset and gain variations due to fluctuations in MOS transistor threshold voltages at the multiple input and output ports. Since the doppler information is typically used on a line-by-line basis, these variations can be tolerated to some extent. However, in the application described here, the information content of an entire frame must be preserved, and the line-to-line variations constitute a serious dynamic range limitation.

The reformatting or "corner turning" operation can be visualized as loading a square memory array in a row-by-row fashion, then reading it column-by-column. The most direct realization involves the use of a memory structure in which charge can be transferred either horizontally or vertically.[13] This realilzation is further enhanced with the addition of a CCD multiplexer and demultiplexer which results in a single input port and output port, thereby minimizing the number of voltage-charge and charge-voltage conversions, and their troublesome threshold dependence.

A block diagram illustrating the operation of this two dimensional CCD memory appears in Figure 5. The input demultiplexer performs a serial to parallel conversion and loads the memory array row-by-row. During the load cycle charge is transferred vertically in the memory array. When all rows have been loaded, the array is switched to a horizontal transfer mode, and the output multiplexer performs the requisite parallel to serial conversion of the data stored in each column.

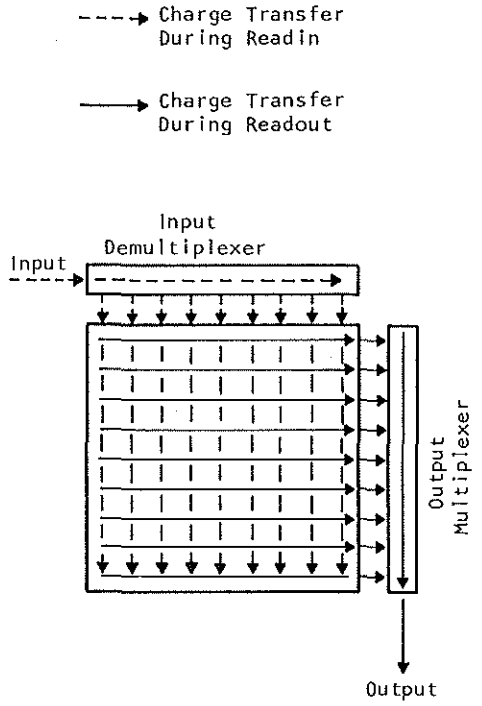


Figure 5. Block Diagram of the Corner Turning Memory (CTM)

A 32 x 32 element CCD memory based on this architecture has been designed and fabricated using the same process utilized for the 32 point CZT IC. A photomicrograph of the chip appears in Figure 6. In order to permit 100% duty cycle in other applications, an additional multiplexer and demultiplexer were included at the bottom and right of the memory array. The memory array is composed of 1024 three-phase two dimensional charge transfer cells placed on 2.0 mil centers. It operates as two interleaved two-phase structures with one common phase. The multiplexer and demultiplexer are four phase structures in order to match the pitch of the memory array and maintain short transfer lengths for good CTE. The structure is buried channel, with the exception of the demultiplexer input circuitry.

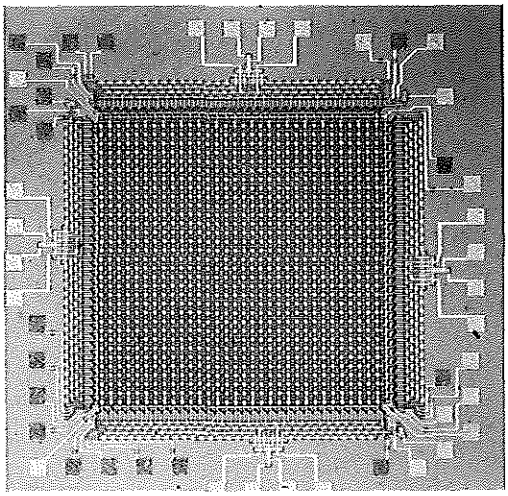


Figure 6. Photomicrograph of Corner Turning Memory (CTM)

The chip has been successfully operated at data rates in excess of 5 MHz. Dynamic range is still dictated by threshold variations in the multiplexer and demultiplexer channels which result in "fixed pattern" noise components. However, nearly 40 dB dynamic range (peak signal to peak noise) is achieved across the entire frame as compared to less than 20 dB observed in a previous line addressable design.[10]

V. EVALUATION OF CCD TWO DIMENSIONAL TRANSFORM

Implementation

A detailed block diagram of the CCD two dimensional transform is shown in Figure 7. A one dimensional DFT is performed on the rows of a real input signal, f(m,n), using the 32 point CZT IC. The real and imaginary Fourier coefficients, $G_R(m,\ell)$ and $G_I(m,\ell)$ are reformatted in two CCD CTMs resulting in transposed matrices $G_R^T(m,\ell)$ and $G_I^T(m,\ell)$. A second one dimensional transform is performed on the transposed data from the CTMs. The final postmultiply operation has been replaced by a magnituding operation.

All timing pulses needed for the CTM operation are generated externally using standard TTL circuits and TTL-MOS drivers. This control circuitry also provides the two phase clocks and synchronization pulses needed for the CCD CZT ICs. Due to a photomask error, the tapweights of the CCD filters on the CZT IC were shifted one stage thereby shifting the output sequence of the Fourier coefficients by one position. This also precludes use of the on chip MDACs for postmultiplication operations.[4] Therefore the MDACs of another CZT IC using a delayed sync pulse were used to perform the postmultiplication needed in the first one dimensional transform.

In order to facilitate interfacing the analog circuitry and to simplify system timing and synchronization, evaluation of this demonstration unit was performed at a 100 kHz data rate.

Experimental Results

A simple two dimensional input test signal was generated by multiplying two analog signals together in a 4 quadrant analog multiplier. One signal provides variations along the horizontal axis and corresponds to the rows of f(m,n). The second signal is sampled once per row and amplitude modulates the first signal to provide variations along the vertical axis and thus along the columns of f(m,n). An example of the two dimensional input signal is shown in Figure 8 for sinusoidal signals. The signals are synchronized by the master timing to provide phase lock for the photographs. Figure 8a shows the input signal for a complete frame, i.e., 32 rows and 32 columns. Figure 8b is an expanded view of the input for one row. In addition, a DC offset was added to the two dimensional test signal in order to mark the origin F(1,1) of the two dimensional transform. Figures 9 through 12 illustrate the operation of the two dimensional transform with the input signal of Figure 8.

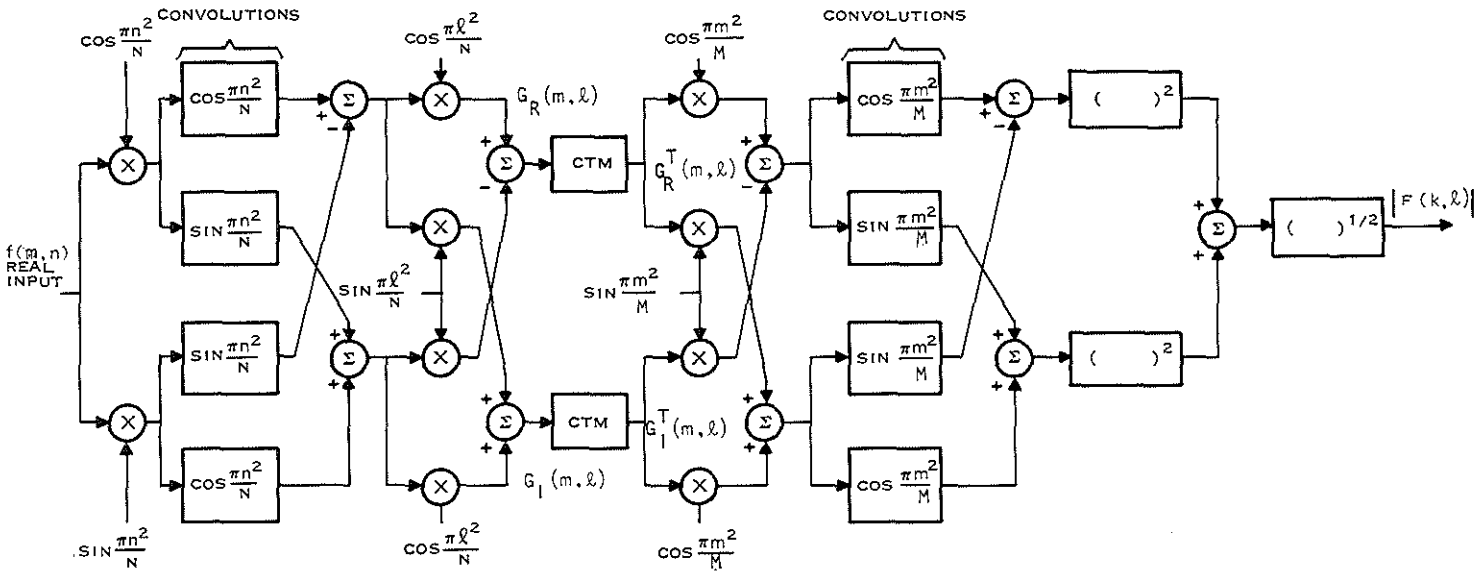
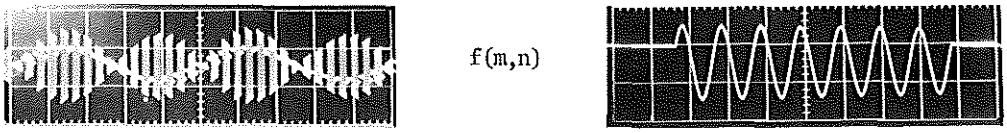
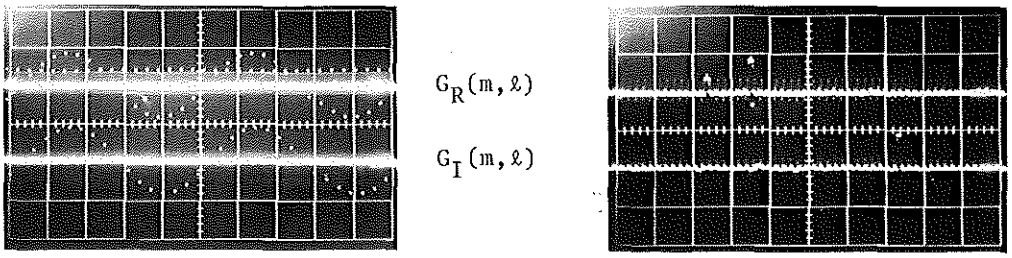


Figure 7 Implementation of the Two Dimensional Discrete Fourier Transform



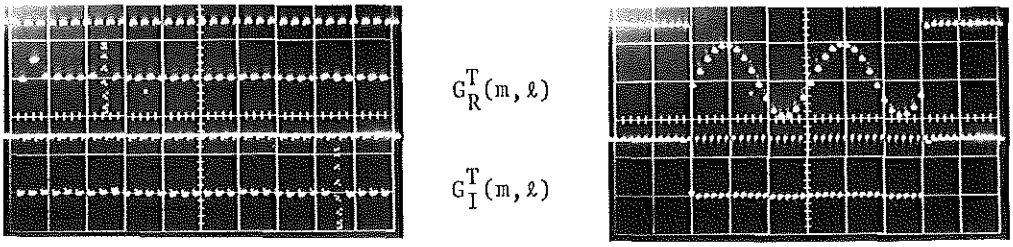
(a) 1 Frame (2ms/cm) (b) 1 Row (50μs/cm)

Figure 8. Input to Two Dimensional DFT



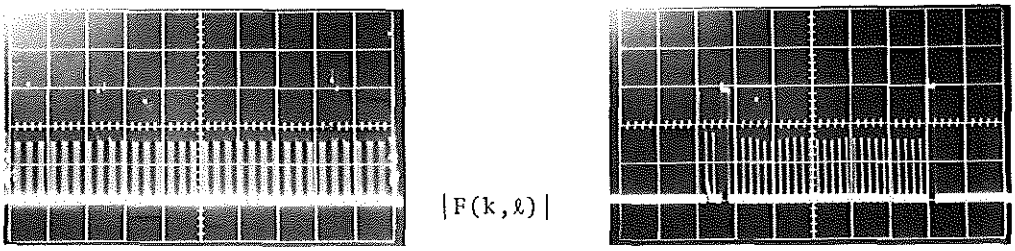
(a) 1 Frame (2ms/cm) (b) 1 Row (50μs/cm)

Figure 9. Output of First One Dimensional Transform $G(m,\ell)$



(a) 1 Frame (2ms/cm) (b) 1 Row (50μs/cm)

Figure 10. Output of Corner Turning Memory $G^T(m,\ell)$



(a) 1 Frame (2ms/cm) (b) 1 Row (50μs/cm)

Figure 11. Output of Second One Dimensional Transform

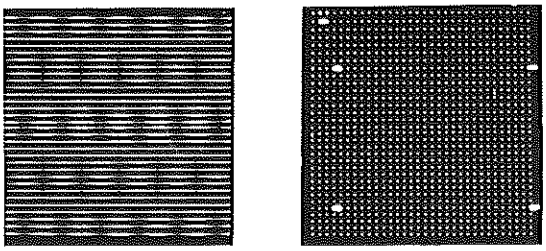
The real and imaginary Fourier coefficients, $G_R(m,\ell)$ and $G_I(m,\ell)$ from the first one dimensional transform are shown in Figure 9 for both the entire frame and for one row. The output of this one dimensional transform for one frame consists of 32 groups of 32 Fourier coefficients, one group for each row of the input signal f(m,n). The Fourier coefficients in each group appear in the order 32, 1, 2, 3, ..., 31 due to the photomask error previously mentioned. The horizontal input signal consists of six cycles of a sinusoid. Therefore the transform of a row results in non zero values for the 7th and 27th Fourier coefficients as shown in Figure 9b. The real and imaginary outputs are 90° out of phase, thus one is at its peak value when the other is zero. Also seen in Figure 9b is a non zero value for the first Fourier coefficient of the real output due to the DC offset of the input signal. Note that with the exception of the DC coefficient the non zero Fourier coefficients are modulated by the vertical signal as seen in Figure 9a.

Figure 10 illustrates the output of the corner turning memory $G^T(m,\ell)$. The corner turning operation transposes the coefficients previously stored, $G(m,\ell)$, thus each consecutive group of 32 points from the CTM consists of the data in one column of $G(m,\ell)$, i.e., the 32 values of a single Fourier coefficient previously obtained by transforming the rows of f(m,n). This matrix transpose operation is confirmed by comparing the CTM outputs in Figure 10 to the CTM inputs in Figure 9. Figure 10a shows a complete frame of transposed data. Figure 10b is an expanded view of the 8th group of 32 points from the CTM. This corresponds to the 32 values of the 7th Fourier coefficient which is the 8th column of $G(m,\ell)$.

The final output of the two dimensional transform unit is the magnitude $|F(k,\ell)|$ which is seen in Figure 11. This is obtained by generating the one dimensional DFT of each of the 32 groups of 32 points from the CTM. This corresponds to obtaining the transform of each column of the matrix $G(m,\ell)$. From Figure 10a it can be seen that only the 2nd, 8th, and 28th groups from the CTM contain non zero coefficient These are due to the input DC offset and the horizontal sinusoid. Thus the second DFT yields non zero coefficients only in the 1st, 7th, and 27th rows of $F(k,\ell)$. The second group from the CTM represents the unmodulated DC offset. The DFT of this group yields only a non zero DC coefficient F(1,1). The The 8th and 28th groups have been modulated by the vertical input signal which consists of two cycles of a sinusoid. The DFT of each of these groups yields non zero values for the 3rd and 31st Fourier coefficients in rows 7 and 27 of $F(k,\ell)$, i.e., F(7,3), F(7,31), F(27,3), and F(27,31). Figure 11b is an expanded view of the DFT of the 8th group from the CTM showing $|F(7,3)|$ and $|F(7,31)|$.

In order to conveniently demonstrate the operation of the two dimensional transform, a display circuit was employed to apply the desired signal to the Z axis of an oscilloscope. The X axis sweep was triggered by a row synchronization pulse and a frame synchronized staircase waveform was applied to the Y axis. A short pulse added to $|F(k,\ell)|$ before each coefficient output displays a two dimensional grid. Each value of $|F(k,\ell)|$ appears as a line after its corresponding grid point. Figure 12 shows the display of the input signal used in Figures 8 through 11 and its two dimensional transform. The input signal is the product of six cycles of a sinusoid in the horizontal direction and two cycles of a sinusoid in the vertical direction with a DC offset added to the product. The display of the two dimensional transform magnitude shows the DC coefficient F(1,1) in the upper left corner at position (2,2) of the 32 x 32 array. The Fourier coefficient F(7,3) due to the input product can be seen at position (8,4) of the array. (Remember that all outputs are shifted by one bit in both directions due to the C%T photomask error.) The three aliased outputs

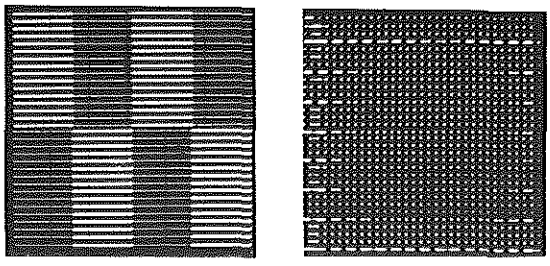
F(7,31), F(27,3), and F(27,31) can also be seen.



(a) Sinusoidal Inputs f(m,n) (b) Output |F(k,ℓ)|

Figure 12. Two Dimensional Display of the DFT Output for Sinusoidal Inputs.

Figure 13 shows the operation of the two dimensional DFT with a square wave product input. The horizontal input seen in Figure 13a is two cycles of a square wave and the vertical signal is one cycle. A DC offset has been added. The DFT output seen in Figure 13b clearly shows the fundamental and odd harmonic components due to each input. The aliased fundamental from the vertical square wave appears in the first column of the display due to the CZT photomask error. The DC components from the 2nd CZT seen in column two of the display are due to the -36 dB fixed pattern noise in the CTM. Figure 14 shows |F(k,ℓ)| for k=3, i.e, the 4th row of the display. An imbalance in the output magnituding circuit used causes the nonuniformity seen in the harmonics.



(a) Square Wave Inputs f(m,n) (b) Output |F(k,ℓ)|

Figure 13. Two Dimensional Display of the DFT Output for Square Wave Inputs.

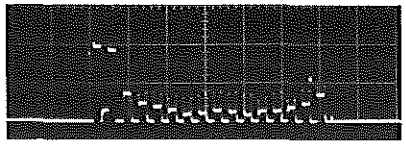


Figure 14. One Row of the DFT Output

The dynamic range of the two dimensional transform is presently limited by the corner turning memory which exhibits 36 dB dynamic range due to a fixed pattern noise component discussed earlier. The dynamic range of the CCD CZT IC has been demonstrated to be 50 dB.[4] The power required for the complete two dimensional transform breadboard was 10 watts. This includes all timing circuitry, external amplifiers, drivers, MDACs, etc. Improvements to the CZT and CTM IC and further integration can be expected to reduce the power requirements and increase dynamic range.

CONCLUSIONS

Preliminary results from a two dimensional DFT breadboard demonstrated the potential in applying analog CCD technology to the implementation of low power, high speed complex two dimensional signal processing algorithms. Although 100 kHz is not an aggressive data rate for CCD circuits, it results in computation of the 32 x 32 point two dimensional DFT (1024 total points) in 40 msec. It is anticipated that CCD two dimensional transforms can be performed at clock rates of several magahertz with a moderate increase in system complexity. This would result in computation times on the order of one millisecond.

ACKNOWLEDGEMENT

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