A PROGRAMMABLE CCD TRANSVERSAL FILTER; DESIGN AND APPLICATION

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ABSTRACT

A CCD-based programmable transversal filter is described. The filter incorporates analogue weighting coefficients and multipliers in an economic structure, suitable for high-density integration. The performance of a monolithic, 64-point prototype device is discussed, and a 256-point chip, which is currently in development, is reported. The limitations of this structure are considered with regard to several potential application areas.

I. INTRODUCTION

State-of-the-art CCD and linear MOS circuit techniques now permit the realisation of electrically programmable analogue filter elements in monolithic form (1). These low-power, light-weight devices have broad application in sonar, radar and communication equipment, where one such filter element may be programmed to perform a variety of matched-, frequency- and statistical-filtering functions. The economic advantage of a single, programmable design over dedicated-function filters is a clear incentive to development. However the possibility of a simple interface to a digital processor, able to intelligently control the filter function in real time, adds a new dimension and makes these devices uniquely attractive in many applications requiring filter adaptability. It is the purpose of this paper to describe a particular realisation of this important filter type.

One plausible filter architecture, capable of monolithic realisation, is shown in Figure 1. This structure is a direct realisation of a Transversal Filter (2) with alterable weighting coefficients. A CCD element forms a tapped-delay line *signal* register which gives a parallel output of a time sequence of signal samples. These are multiplied by a set of weighting coefficients, stored as voltages in a register of MOS capacitors, the multiplication being performed by a single MOS transistor at each filter point. All products are simultaneously summed to produce the filter output, {o}. It is easily shown that

$$o(nT) = \sum_{m=1}^{N} s(nT - mT) r_m \qquad (I.1)$$

where {r} represents the reference (or weighting) sequence and {s} is the sampled input (or signal) sequence. Equation (I.1) is often referred to as the convolution sum, since it represents the convolution of the signal {s} with the reference {r} , which itself defines the impulse response of the filter.

This sequence of reference voltages may be most easily programmed from a common analogue input bus, under the control of a digital selector. Naturally information stored on the capacitors is volatile and must be refreshed periodically, implying the use of an additional non-volatile (digital) memory. Despite the requirement for two levels of memory however, this parallel structure is favourably compact because of the smallness of the analogue multiplying elements in comparison with digital components.

The CCD signal delay line may be implemented using any non-destructive tapping technique. We have used the Floating Gate Reset (FGR) (3) configuration with encouraging success. Charge packets are sensed capacitively, via an isolated (floating) CCD electrode, followed by a high input-impedance MOST buffer amplifier. FGR tapping may be combined with a feedback linearisation scheme at the input (3), employing a dummy tap and a single operational amplifier to linearise the overall transfer function, and automatically achieve unity gain.

The advantages of this simple filter structure are that it is extremely compact (allowing many filter points to be integrated on a single chip), and that identical stages (and devices) may be directly cascaded through the CCD signal register to form much larger filters.

II. MULTIPLICATION

The performance of previous filter realisations has suffered largely because of poor stability and accuracy in the multiplication elements. We describe here 4- and 2- quadrant multiplication techniques based upon a single MOS transistor which are both more stable and more accurate than previously reported matched transistor circuits (4,5).

We begin with an MOS transistor operating in the triode region with a virtually grounded source, at a potential V_{r_o}, as shown in Figure 2. Now apply one multiplicand voltage V_r to the drain, with respect to the source, and apply also a voltage V_{s_o} (equivalent to a signal zero) to the gate. Then, from simple MOS theory,

$$I_{D_o} = \beta_m([V_{s_o} - V_T]\, V_r - \frac{V_r 2}{2}) \quad (II.1)$$

where β_m is a process dependant gain constant and V_T is the transistor threshold voltage. If we now *change* the gate voltage by the second multiplicand, V_S , the *change* in drain current, ΔI_D, is simply :

$$\Delta I_D = \beta_m V_r V_s \quad (II.2)$$

It is easy to show that this product is valid for all sign combinations, thus realising 4-quadrant multiplication.

An output circuit is shown in Figure 3 which may be used to sum the currents from all multiplier transistors, and to detect the absolute change in current, ΔI_D. The circuit is time multiplexed, using two phases. During the first phase, signal zeros are switched into the multiplier gates and the output voltage is zeroed via a feedback loop, which bleeds the current I_{D_o} from the summing bus, through resistor R_B. During the second phase, the desired signal values are switched onto the multiplier gates, and the output from the current summing amplifier is the sum-of-products term required. Within the filter realisation, signal-zero switching is easily achieved through the floating-gate-tap reset transistor, whilst the reference voltages are applied to the multiplying transistor drains.

If signal information at d.c. (0 Hz) is not required (as is often the case in practice) then 2-quadrant multiplication is sufficient, we may remove the time-multiplex requirement and simply a.c. couple the output from the current summing amplifier, to detect the required output changes about an arbitrary zero. This arrangement is clearly much simpler and requires no switching operation, which in practice implies a faster realisation. The current summing amplifier itself may be a simple common-base bipolar transistor stage (off-chip). The single-transistor, time-multiplexed multiplying technique described here has been used with considerable practical success in a prototype programmable filter realisation, to be described. It is notably stable, easy to implement, and more accurate than a matched-transistor realisation.

III. DEVICE REALISATION

We have used these filter techniques to realise a prototype 64-point programmable transversal filter, and to design an improved 256-point filter, currently in development. Circuit details of the prototype filter cell are shown in Figure 4. A 3-phase CCD structure in metal-gate technology (6) was used, with two CCD stages between taps, on a pitch of 56 μm. Selection of reference update points is achieved via a NOR gate at each point, which decodes an externally-supplied reference address. Provision is also made for feedback linearisation of the reference

coefficients via a multiplexed feedback bus. Power dissipation is approximately 5 mW per cell (320 mW per chip) and speed is limited in practice, by complex timing waveforms, to sampling up to 100 kHz. All peripheral circuits (such as linearising amplifiers and clock drivers) are off-chip. Figure 5 shows a drawing of this prototype device, which measures 184 mils by 136 mils and practical results are reported in Section IV.

A new filter design is currently in development and includes several major improvements. A 2-phase CCD structure in double-level polysilicon technology (7) is to be used, with taps at every CCD stage on a new pitch of 28 μm (exactly half that used previously). This small pitch is made possible in part because of the self-aligning property of the MOS transistors fabricated on this process. Reference points are now updated serially, using a digital shift register selector, in order to reduce the pin-count. Power dissipation is cut to 1 mW per cell and a signal bandwidth of 10 MHz (sampling at 20 MHz) appears feasible from simulations. This should be more readily achieved in practice due to greatly simplified drive requirements. The active layout area of a 256-point block measures 144 by 124 mils, and is configured as 2 x 128 point filters, which may be cascaded, or run in parallel as quadrature channels. Input and output operational amplifiers are to be included on-chip in the signal channel, so that cascading is by means of a single wire.

The amplifiers are based on the switched-capacitor differential stage (8), including a single high-gain invertor to meet the following specifications :

Open loop gain	40 dB
Power dissipation	6 mW
Max clock frequency	2 MHz
Layout area	20 $mils^2$ (24,000 μm^2)

This form of operational amplifier is most suitable in these applications, in that it is automatically chopper-stabilised and requires no external compensation or adjustment. The additional layout area involved is minimal.

IV. RESULTS

The following results relate to a characterisation programme carried out on the prototype 64-point filter, using the time-multiplexed, 4-quadrant multiplication technique.

A suitable guide to noise performance may be obtained by examination of the impulse-response, of which a typical example is given in Figure 6. Under these conditions only one filter point is active at any time, whilst all points constantly contribute noise. From this example, the impulse response is found to have a dynamic range of 34 dB. Since this result must vary according to the number of filter points, a more meaningful figure may be obtained by referring it to a filter with a single point, which in this case gives a value ; $D_{f_p} = 52$ dB.

It is possible to use this parameter to derive the dynamic range of the complete filter with any arbitrary reference. For example, the best condition occurs for the matched filtering of two square waves, when all points contribute maximum power at the output. The corresponding dynamic range for matched square-waves using the 64-point device is thus 70 dB, which we have verified independently by measurement.

A good indication of filter accuracy is given by the stop-band performance of the device in a frequency-filtering mode. Figure 7(a) shows the frequency response of the filter having the impulse response shown in Figure 8, ideally a Hamming-weighted low-pass filter with stop-band suppression around -50 dB. The average stop-band attenuation achieved in practice is approximately -34 dB and indicates an equivalent multiplier accuracy (9) of approximately 2%. Figure 7(b) demonstrates improved stop-band performance, by a factor of 6 dB and was achieved by adjusting the reference coefficients to correct the observed impulse response, as described in Section V.

Use of the device in matched-filter mode is demonstrated in Figure 8 , where the centre trace shows a reference 'chirp' and the upper trace shows a corresponding signal chirp (from the

64th CCD tap, available for cascading). The output (lower trace) is clearly close to the ideal sinc form. A more testing (higher time-bandwidth) matched chirp result has been obtained from a 256-point filter shown in Figure 9 (a). This filter dissipates 3W and is constructed on a printed-circuit board measuring 6.3 x 9.2 ins, using 4 cascaded 64-point devices. Figure 9 (b) shows the correlation peak obtained by matching chirps of full Nyquist bandwidth (TB = 128), the output peak being a single impulse in this instance. Charge transfer inefficiency ultimately limits the maximum TB that may be processed. Independant simulations (10) of this effect show that correlation peaks remain usefully uncorrupted for TB up to 1000 with c.t.i. at 10^{-3} per tap.

V. ADAPTIVE FILTERING

We present in this section two circuit techniques which allow the filter to automatically achieve an optimal response, regardless of any inherent errors. The first technique, which we have called *iterative reference adaptation*, is used to achieve exactly, a specified impulse response. The control loop, shown in Figure 10, is formed around a microprocessor, which is used to monitor the filter output and apply a correction to the reference coefficients held in digital memory. The impulse response of the filter is monitored and compared to the existing reference coefficients, which are corrected if they deviate from the ideal value. Thus any ideal impulse response may be realised to a specified accuracy, regardless of multiplier and other circuit imperfections (11). The filter architecture described, with a static reference register, is ideally suited to this adaptation technique which can permanently trim out all coefficient weighting errors. It has been computed that an adaptation time of 1 second is sufficient to correct the impulse response of the 64-point filter to an equivalent accuracy of 8 bits.

Once corrected, the new reference values might be transferred to a PROM module on a dedicated filter board, to realise a stand-alone, accurately programmed filter. The microprocessor adaptation system would remain as a single laboratory facility for servicing these modules.

The second adaptive system is a realisation of the Widrow LMS algorithm (12), which may be used to force a desired filter output from an arbitrary input by rejecting all other signal components. A block diagram of the system is shown in Figure 11. The filter is supplied with two inputs, the signal input, s(t), and the desired filter response to this input, d(t). The objective is to force the filter output, r(t), to resemble d(t) as closely as possible, by adapting the reference weight vector $\underline{H}$ using the algorithm :

$$h_k(T + 1) = h_k(T) + 2\mu\varepsilon(T)\, s(T - k)$$

where μ is a selected convergence factor, and $\varepsilon(t) = d(t) - r(t)$;
the subscript k denotes tap position and the term in brackets is the time index;
T is normalised in units of one delay time.

This filter has been implemented using the 64-point prototype programmable device (13) and Figure 12 demonstrates its response to a sinusoidal wave at 1 kHz, contaminated by another signal at 5.4 kHz. The desired output is the 1 kHz sine and it can be seen that considerable rejection (35 dB) of the interfering signal takes place at the output (Figure 14(b)). The weight vector is shown in Figure 14(c) and forms the expected sinusoid.

In other performance tests this filter is found to compare well with published simulation results. Although the filter architecture is not optimised for the implementation of this algorithm, the device principles could be applied to a dedicated, adaptive chip design.

VI. CONCLUSIONS

We have shown how novel, linear MOS design techniques may be combined with state-of-the-art CCD technology to realise a monolithic programmable filter with great application potential. A prototype 64-point filter has been fabricated and has demonstrated useful performance characteristics in both frequency- and matched-filter configurations, and in adaptive modes. An improved 256-point filter chip is now in development which promises reduced power consumption (1 mW per point) and increased processing band-width

(possibly 1 MHz). The devices are relatively simple to drive and may be directly cascaded for matched filter applications up to time-bandwidth products of 1000.

ACKNOWLEDGEMENTS

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REFERENCES

1. P B Denyer, J W Arthur and J Mavor, "Monolithic, Programmable Analogue CCD Transversal Filter", Elect Lett, Vol 13, pp 373-374, Nov 1977.

2. J H Whitehouse, R W Means and J M Speiser, "Signal Processing Architectures using Transversal Filter Technology", IEEE International Symposium on Circuits and Systems, April 1975.

3. P B Denyer, and J Mavor, "Design of CCD Delay Lines with Floating Gate Taps", IEE J Solid-State and Electron Devices, 1977, Vol 1, pp 121-129.

4. J G Harp, G F Vanstone, D J MacLennan and J Mavor, "Analogue Correlators using Charge Coupled Devices", Proc CCD 75, pp 229-235.

5. P Bosshart, "An Integrated Analogue Correlator using Charge-Coupled Devices", in Proc IEEE ISSCC, 1976, pp 198-199.

6. K D Perkins and V A Browne, "Sub-Micron Gap Metal Gate Technology for CCD's", Microelectronics Journal, 1975, Vol 7.

7. V A Browne, "Performance Limitations of Two Phase CCD's", AGARD Conference on "Impact of CCD and SAW on Signal Processing and Imagery in Advanced Systems", Ottawa, October 1977.

8. P B Denyer and J Mavor, "Novel MOS Differential Amplifier for Sampled Data Applications", Elect Lett, Vol 14, pp 1-2, Jan 1978.

9. C M Puckette, W J Butler and D A Smith, "Bucket-Brigade Transversal Filters", IEE Trans on Communications, Vol 22, pp 926-934, July 1974.

10. P B Denyer, "The Effect of Charge Transfer Inefficiency on the Matched Filter Detection of Chirp Waveforms", Internal Report.

11. P B Denyer, J Mavor and J W Arthur, "Miniature Programmable Transversal Filter using CCD/MOS Technology", Proc IEEE Special Issue on Miniature Filters, to be published, Jan 1979.

12. B Widrow et al, "Adaptive Noise Cancelling : Principles and Applications", Proc IEEE, 1975, 63, (12), pp 1692-1716.

13. C F N Cowan, J Mavor and J W Arthur, "Implementation of a 64-Point Adaptive Filter Using an Analogue CCD Programmable Filter", Elect Lett, Vol 14, No 17, Aug 1978.

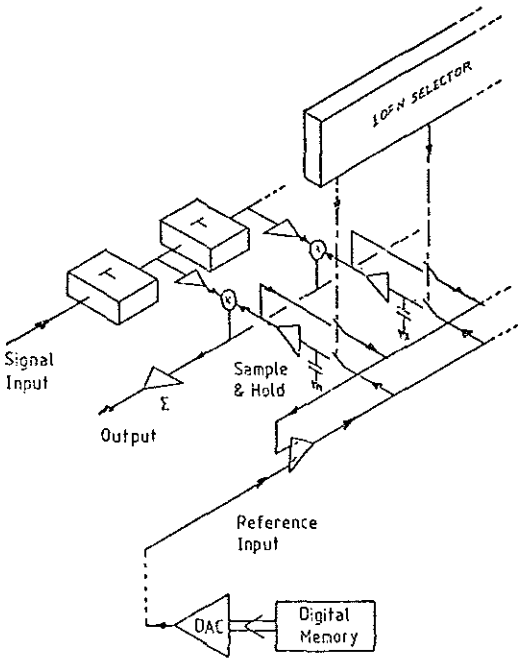

Figure 1 Block Diagram of Programmable Filter Architecture

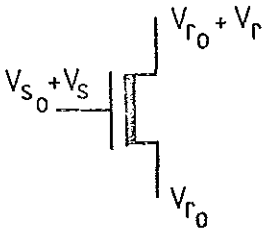

Figure 2 MOS Multiplier Transistor Nomenclature

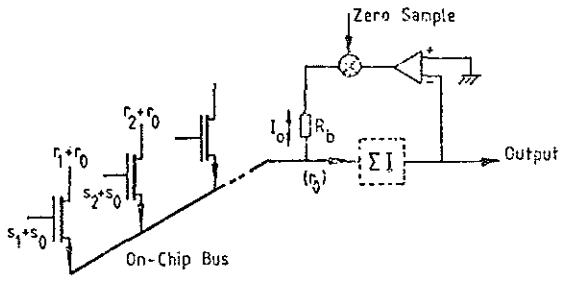

Figure 3 Multiplication and Summing Circuitry

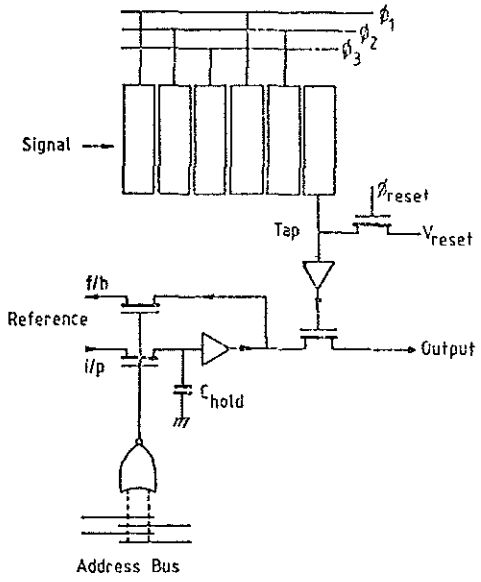

Figure 4 Circuit Diagram of Prototype Filter Cell, 3-Phase Metal Gate CCD.

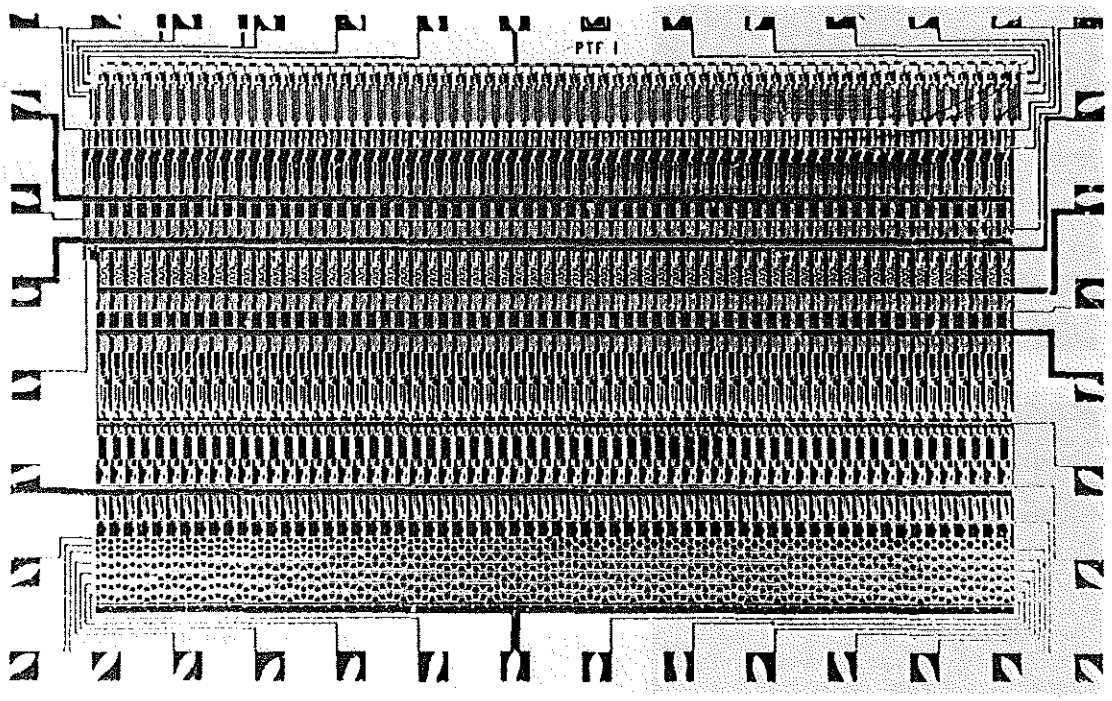

Figure 5 Prototype 64-Point Programmable Filter, Die Size 184 x 134 mils

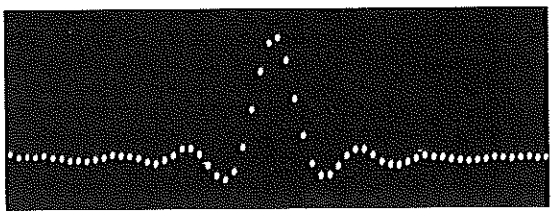

Figure 6 Impulse Response, Hamming Weighted Low Pass Filter, Pass-Band 0 - $f_c/8$ Hz

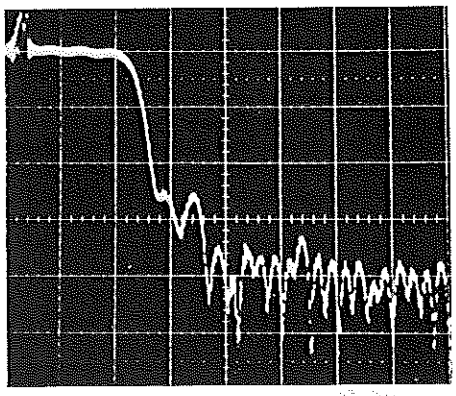

Figure 7(a) Frequency Response of Hamming Weighted Low Pass Filter; Reference Directly Applied.

Horizontal : 1 kHz/cm
Vertical : 10 dB/cm
f_c = 16 kHz

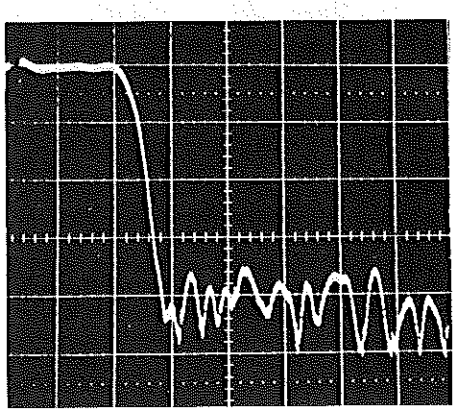

Figure 7(b) Frequency Response as Above but With (Visually) Corrected Impulse Response

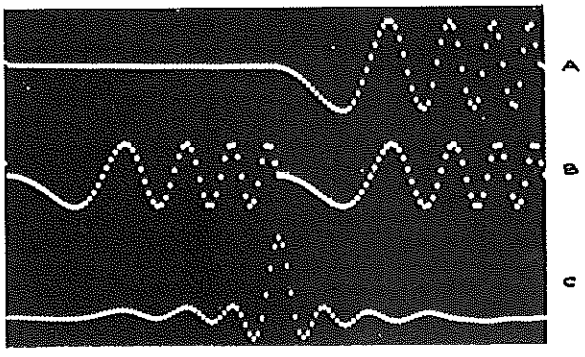

Figure 8 Matched Filtering of a 64-Point Chirp Waveform 0 - $f_c/8$ Hz.

(a) Signal at 64th CCD Tap 1V/cm
(b) Reference Waveform 5V/cm
(c) Filter Output 5V/cm

Horizontal : 2 ms/cm

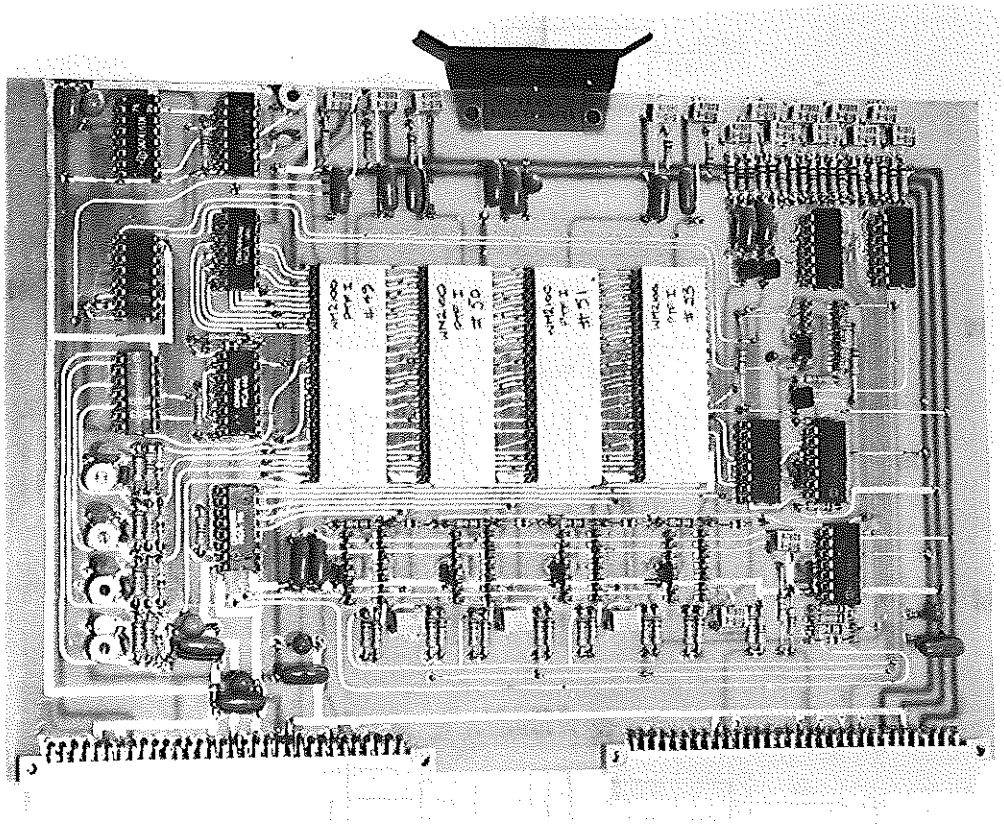

Figure 9(a) 256-Point Programmable Filter Board Containing 4 Cascaded 64-Point Prototype Devices with Drive Electronics

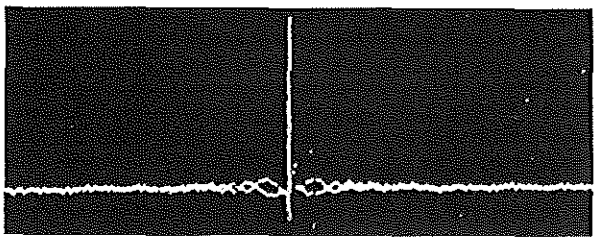

Figure 9(b) Matched Filter Response to 256-Point Chirp Waveform 0 - $f_c/2$ Hz (TB = 128)

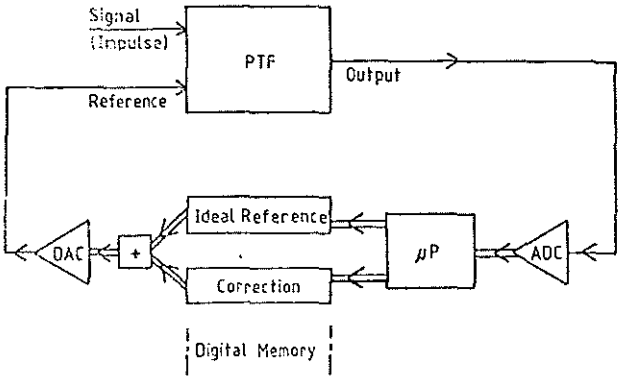

Figure 10 Block Diagram of Control Loop for Adaptive Correction of Reference Coefficients

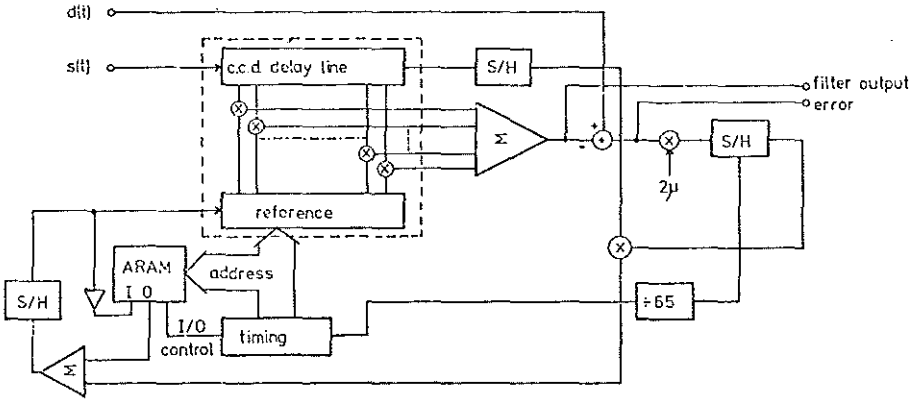

Figure 11 Block Diagram of Adaptive Filter, Based on Widrow LMS Algorithm

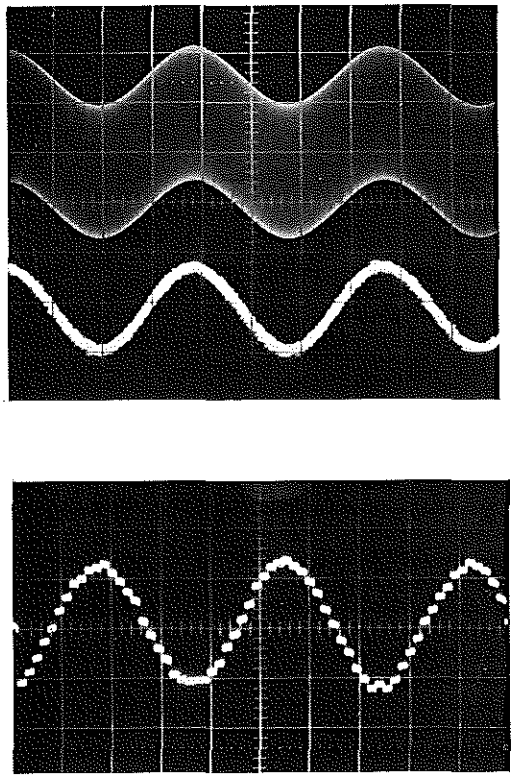

Figure 12 Adaptive Filter Response to 1 kHz Sinewave with 5 kHz Interference.

(a) Contaminated Input Signal
(b) Output Signal
(c) Adapted Tap Weight Vector