APPLICATION OF CHARGE-COUPLED DEVICE TECHNOLOGY TO TWO-DIMENSIONAL IMAGE PROCESSING*

G.R. Nudd
Hughes Research Laboratories
Malibu, CA 90265

P.A. Nygaard
Industrial Products Division
Carlsbad, CA 92008

C.L. Jiang
Hughes Aircraft Company
Culver City, CA 90230

Abstract

This paper describes the application of charge-coupled device (CCD) technology to two-dimensional image processing. The processing operations discussed are widely used as preprocessing functions for more complex image understanding techniques. Algorithms such as edge detection, local averaging, and unsharp masking[1,2] have been implemented directly in the charge domain using extensions of the analog transversal filtering techniques previously demonstrated. The design concepts and circuit layouts are discussed together with the performance data on test imagery and "real-time" video.

1. Introduction

In the past several years, there has been a significantly increased interest in image enhancement and image understanding both for commercial systems (such as industrial inspection) and for military sensors. The processing algorithms and techniques developed have generally been implemented on general-purpose digital computers, and, in general, the processing times required to perform even relatively simple operations, such as local edge detection, have limited their use to non-real-time applications. The Sobel edge-detection scheme[3] described here, for example, requires approximately 5×10^6 operations per frame and might take 5 to 10 sec on a PDP-10 machine. This is two to three orders of magnitude slower than is required for "real-time" video (≈ 7.5 MHz).

Since low-level or preprocessing operations typically require the greatest computation time, one would generally want to use the preprocessor to dramatically reduce the data rate. This would allow the higher level operations (such as the so-called syntactic operations) to be performed at much lower throughput. The aim of this work is to investigate the feasibility of performing several commonly used preprocessing operations in CCD circuitry and thereby to increase the processing speed to allow real-time operation. CCDs were choosen both because they have inherently low power-delay products (which allow very high circuit densities) and because many modern sensors are themselves CCDs. In this way, the preprocessing functions might be incorporated directly into the sensor as options. This is the basis of the so-called "smart sensor" philosophy. The functions described here are edge detection, local averaging, adaptive stretch, binarization, and unsharp masking. The formulations of each of these algorithms is given in Section 2. Where appropriate, we have tried to structure the processing in the form of analog transversal filters to achieve optimal-speed and circuit density. This has required the development of two-dimensional filtering operations and novel circuit techniques to perform operations, such as absolute value determination, directly in the charge

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domain. This should provide optimal dynamic range and linearity.

2. Definition of Processing Algorithms

Five preprocessing operations have been implemented. Each is based on a kernel of 3 x 3 pixels, shown in Figure 1. The first test circuit is a CCD implementation of the Sobel edge-detection algorithm.[3] This circuit was chosen because it demonstrates two operations important to image processing: (1) the possibility of achieving a two-dimensional convolution with arbitrary weightings and (2) the ability to perform nonlinear functions such as the absolute magnitude operation.

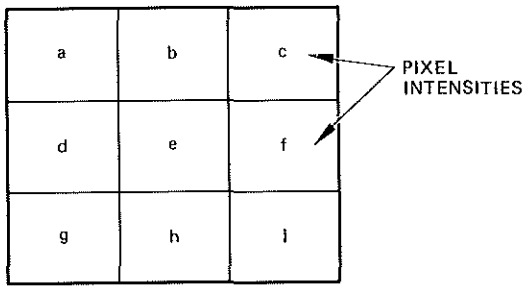


Figure 1. Schematic of the basic 3 x 3 kernel.

The Sobel algorithm operates on the full array and evaluates

$$S(e) = 1/8\ [|(a + 2b + c) - (g + 2h + i)| + |(a + 2d + g) - (c + 2f + i)|] \quad (1)$$

for each picture element. This output is a measure of the edge components passing through the kernel and is independent of both the polarity of the edge and, to a large extent, its orientation. The other operations are

Local averaging:

$$f_m(e) = 1/9\ [a + b + c + d + e + f + g + h + i] \quad (2)$$

Unsharp masking:

$$S_u(e) = (1 - \alpha)e - \alpha\, f_m(e) \quad (3)$$

Adaptive binarization:

$$S_b(e) = \begin{cases} 1 \text{ for } f_m(e) \le e \\ 0 \text{ for } f_m(e) > e \end{cases} \quad (4)$$

Adaptive stretch:

$$S_a(e) = \begin{cases} 2 \text{ Min } \{e, r/2\} & \text{for } f_m(e) \le r/2 \\ 2 \text{ Max } \{(e, r/2), 0\} & \text{for } f_m(e) > r/2, \end{cases} \quad (5)$$

where r is the maximum pixel intensity.

All of the above operations can be obtained by combinations of three basic functions: the local means $f_m(e)$, the edges $S(e)$, and the center pixel intensity. Each of these functions can be obtained directly from the CCD analog transversal operations described below.

3. Device Descriptions

The CCD implementation of two-dimensional edge detection and local mean algorithm is an important aspect of many real-time image-processing applications. Further, since the functions discussed in Section 2 can be derived from combinations of center pixel intensities, local means, and edges, only the CCD edge detection and local mean circuits will be described in detail.

The CCD Sobel circuit consists of a 3 x 3 two-dimensional transversal filter, an absolute value operator, and a summing circuit. Figure 2 is a functional block diagram for the circuit. Three lines of analog video signal are fed into the 3 x 3 CCD Sobel transversal filter. Two differential outputs are obtained and amplified before taking their absolute values and summing. The final output $|a+2b+c - (g+2h+i)| + |a+2d+g - (c+2f+i)|$ provides edge information about the image (as is shown in Section 4). Other input and output points are also available for individual circuit tests, as indicated in Figure 2.

The CCD Sobel circuit has three parallel signal channels for the three analog video lines of the image. The inputs are of the Tompsett fill-and-spill type. The two-dimensional processing results from the appropriate inter-connection of the eight

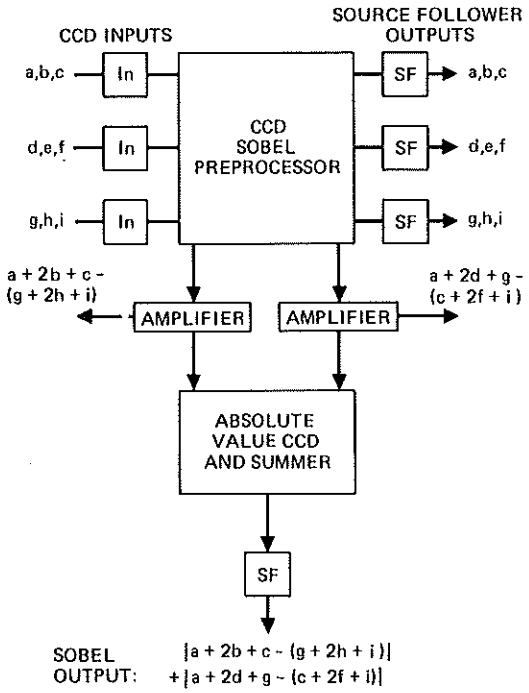


Figure 2. Block diagram for CCD Sobel operator.

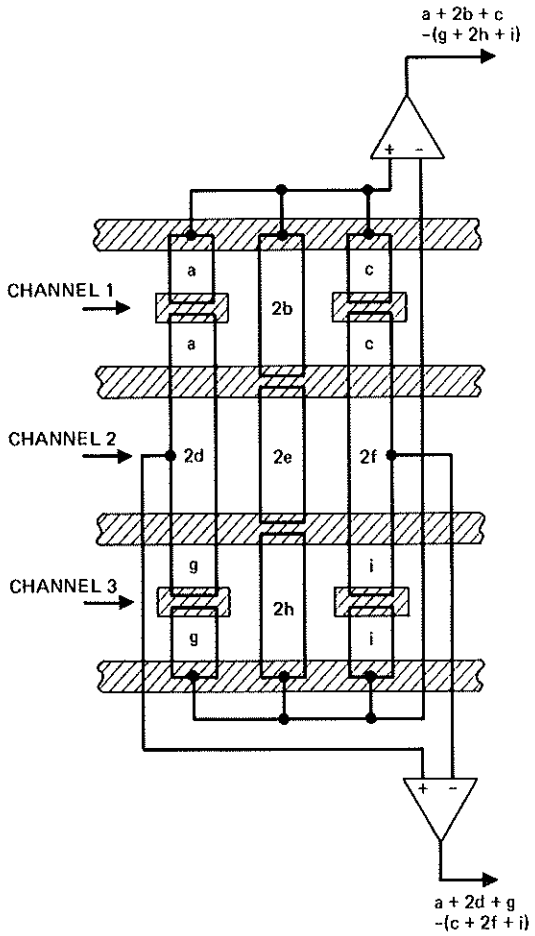


Figure 3. CCD Sobel preprocessor.

floating gates of the three-channel split-electrode transversal filter. Figure 3 shows that the output in each of the four bus lines is proportional to the charges under the connected gates (a, b, c, etc.). The necessary weightings (1, 2, 1, etc.) are achieved by varing the floating gate area. The differences between the weighted sums are obtained through the output differential amplifiers. Each output, therefore, represents an orthogonal edge component. These components then act as inputs to the gates of the CCD absolute value circuit shown in Figure 4 to achieve the two-dimensional Sobel output.

The CCD absolute value circuit operates using a novel technique that allows a charge storage that is equivalent only to the input signal magnitude and is independent of signal polarity. During the input phase, ϕ_{INA} is pulsed low first (high surface electron potential in an n-channel CCD) and then settles high (low surface electron potential). When the signal voltage V_{SIG} is less than the reference voltage V_{REF} set by the REF gate, the electrons will fill the potential well under the gates B2 and FZ, as shown in Figure 4(a). During the output phase, ϕ_{OUTA} is pulsed high and the charge packet is transferred to the summing output. This charge is proportional to

$$\left\{\left(V_{FZ} - V_{REF}\right)\left(A_{FZ} + A_{B2}\right) + \left(V_{REF} - V_{SIG}\right)\left(A_{FZ} + A_{B2}\right)\right\} ,$$

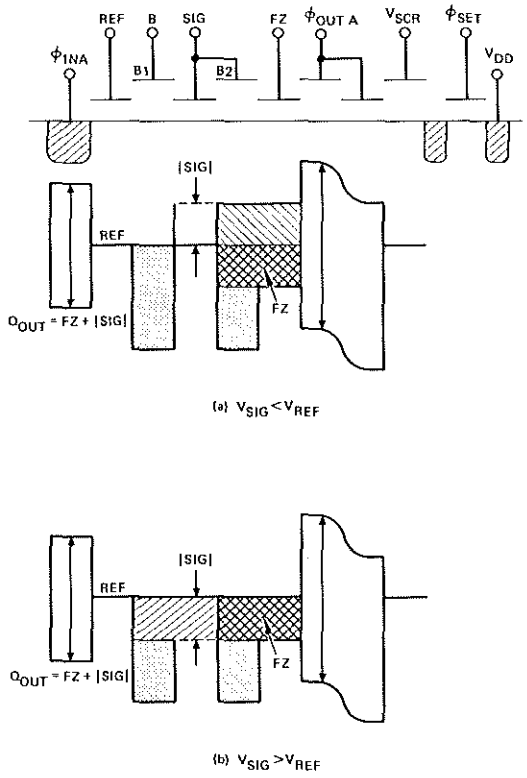


Figure 4. CCD absolute value circuit.

where A_{FZ} is the rate of the gate FZ, etc. The first term corresponds to the fat zero charge and the second to the signal charge referred to the reference level. However, if V_{SIG} is higher than V_{REF}, the potential well under B1, SIG, B2, and FZ will be filled, as shown in Figure 4(b). The output charge is proportional to

$$\left\{\left(V_{FZ} - V_{REF}\right)\left(A_{FZ} + A_{B2}\right) + \left(V_{SIG} - V_{REF}\right)\left(A_{SIG} + A_{B1}\right)\right\}$$

If the gate areas are fabricated such that $A_{SIG} + A_{N1} = A_{FZ} + A_{B2}$, then the output charge will always be a fat zero plus the charge proportional to the magnitude of the signal with V_{REF} as reference point. That is, a charge output corresponding to the absolute value of the input signal is obtained. After the absolute values of the differences are obtained, they are summed in the charge domain and the Sobel operation is completed. The CCD local mean circuit shown in Figure 5 consists of 3 x 3 cells with nine floating gates connected together to yield an output proportional to a+b+c+d+e+f+g+h+i.

The gate interconnect of the 3 x 3 CCD two-dimensional filtering circuit has to be laid out carefully to minimize the stray capacitance and to balance the positive and negative input to the differential amplifiers. In the CCD absolute value circuit, speed and accuracy are, in the case of $V_{SIG} > V_{REF}$, limited by the transfer inefficiency.

The CCDs are N channel and are fabricated with a two-layer polysilicon process. This process requires nine masks and two ion implantations. The CCDs have a bit

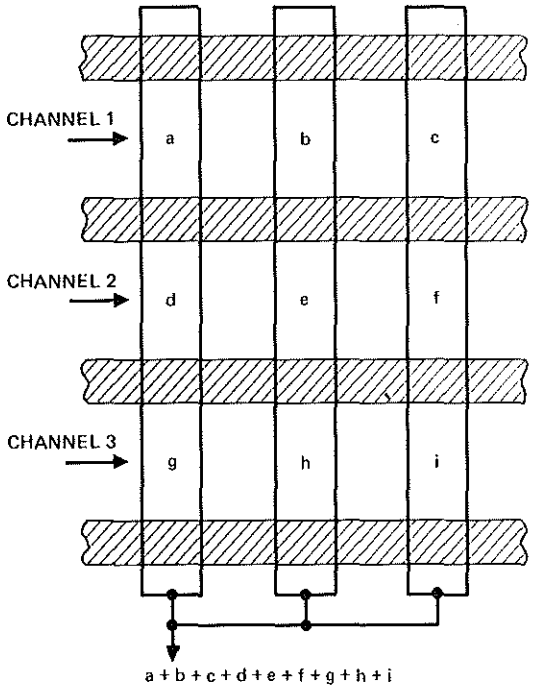
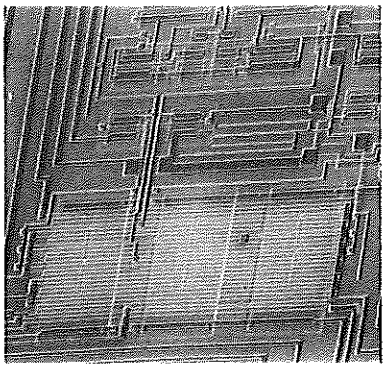


Figure 5. CCD local mean circuit.

length of 27 μm, and the minimum feature size is 2.5 μm. This results in a total area of 0.7 mm^2 for the Sobel (see Figure 6(a)), of which 0.15 mm^2 is the transversal filter. This compares with a total area of 0.6 mm^2 for the mean filter (Figure 6(b)). To achieve the necessary capacitance balance between the two difference outputs, additional metal was added, as Figure 6 shows.

(a)



(b)

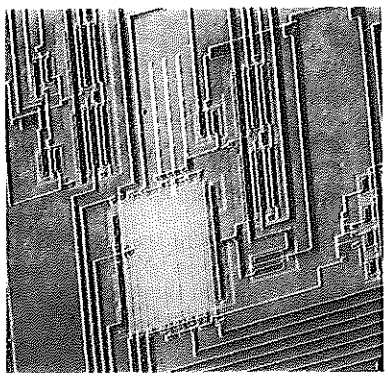


Figure 6. Photomicrographs of (a) the edge detection circuit and (b) the local mean filter.

4. Test Results

a. Measurement of Electrical Characteristics.

The two basic functions of the CCD circuits, arithmetic operations (such as absolute magnitude determination and summation) and transversal filtering, have been tested independently and the transfer characteristics measured. The weighting functions of the transversal filters for the Sobel edge detection and local mean evaluation, for example, can be written as:

$$S_x = 1/8 \begin{bmatrix} 1 & 2 & 1 \\ 0 & 0 & 0 \\ -1 & -2 & -1 \end{bmatrix}$$

$$S_y = 1/8 \begin{bmatrix} 1 & 0 & -1 \\ 2 & 0 & -2 \\ 1 & 0 & -1 \end{bmatrix}$$

$$W_m = 1/9 \begin{bmatrix} 1 & 1 & 1 \\ 1 & 1 & 1 \\ 1 & 1 & 1 \end{bmatrix}$$

where S_x and S_y provide the x and y components of the edge values, and W_m provides the mean. Both the impulse response and the linearity of these operations have been determined using the microcomputer-based test set-up shown in Figure 7.

Here the microcomputer is used to provide flexible and programmed data inputs to the CCD circuits. These data are then clocked through the devices, and the output is stored in the computer memory. This provides an accurate and rapid means of characterizing the device performance as a function of the various input parameters. The speed and accuracy of this system are basically determined by the computer cycle time and the analog-to-digital converters. The machine described here has a basic cycle time of ≈ 2 μsec and can provide an 8-bit quantization, resulting in a maximum CCD clock speed of ≈ 30 kHz.

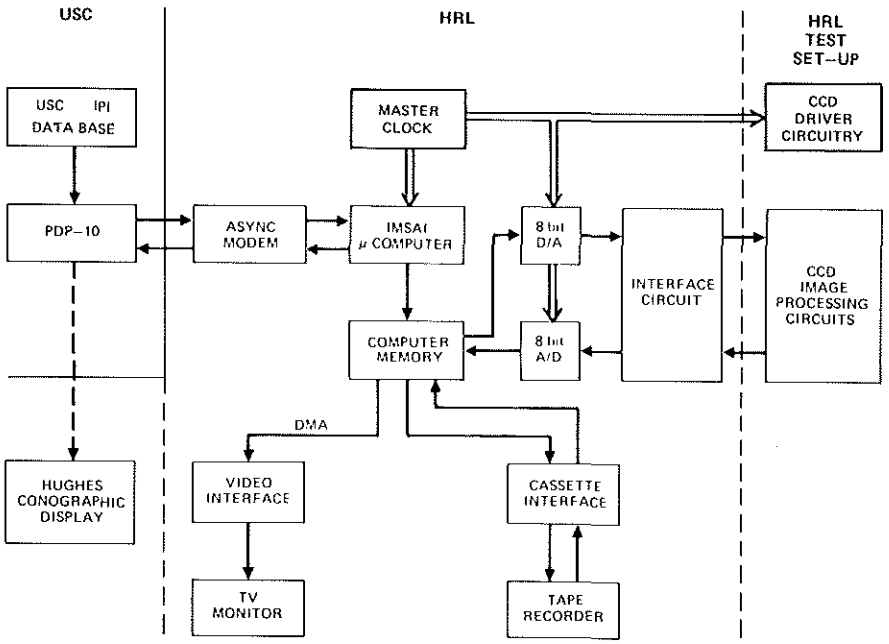


Figure 7. Microcomputer-based test facilities.

When a single input pulse with a duration of less than one-half clock cycle is used as the input, the output is equivalent to the impulse response of each component of the filters. Examples of this for the Sobel operation are shown in Figure 8.

An additional benefit of this test set-up is that a unique pattern of either analog or digital data can be generated and used as the input to the CCD circuit and the output data gated so as to uniquely determine the operation of any tap within the array. For example, if an input that linearly increases with time is clocked into the array and the output is gated so as to measure only the nth output pulse in each cycle, the weighting W_n of the nth floating electrode in the array can be uniquely determined. Measurements made in this way are shown in Figure 9, which shows the output voltage directly as a function of the input for each of the nine floating gates in the Sobel filter. The slope of each input/output characteristic gives the tap weighting for each tap. From this, inputs can be shown to be linear over approximately a 3-V range. This translates to an accuracy and dynamic range equivalent to approximately 16 gray levels.

The absolute value circuit described in Section 3 was tested using a similar technique; the results are shown in Figure 10. Here the input voltage on the gate SIG has been swept over a range of 0 V to 10 V, and the characteristic can be explained with reference to Figure 4. Initially, as the signal voltage is increased, charge flows over the input gate and is stored under gates FZ and B1. This charge is then clocked out as the clock phase changes. However, as the input voltage is increased beyond V_{in1} (Figure 9), the bucket size decreases linearly, resulting in the linear change in voltage out (AB). When the input voltage reaches V_{REF}, the bucket size is a minimum equivalent only to the fat zero. Increasing the input further causes some of the charge previously trapped under B1 to be clocked out. Thus, the output characteristic again changes linearly from B to C. Hence, when the input signal is operated about V_{REF}, the output changes linearly in proportion to $|V_{SIG} - V_{REF}|$, the output polarity being

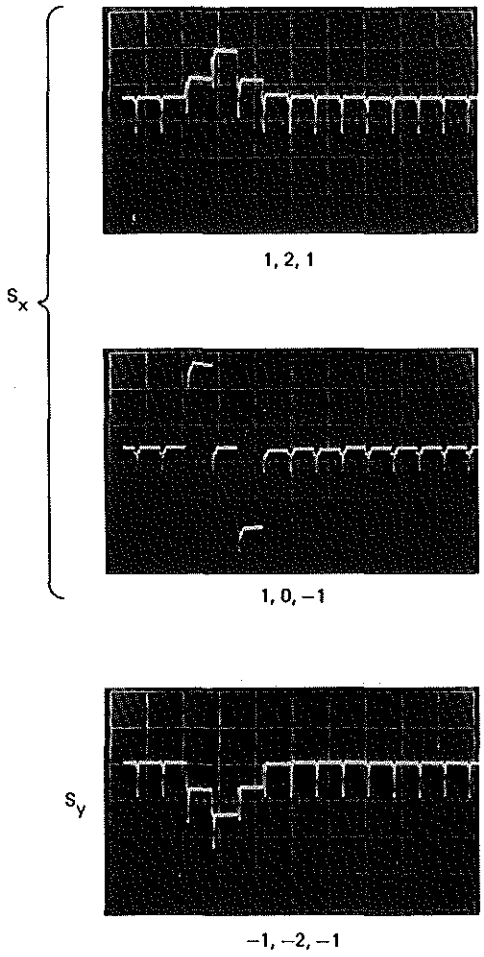


Figure 8. Measured impulse response of CCD Sobel filter.

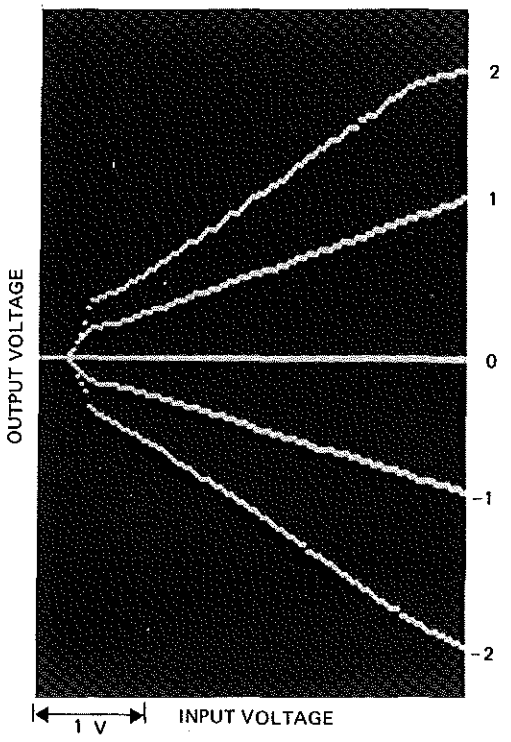


Figure 9. Measurement of the weighting functions for Sobel operators.

independent of V_{SIG}. The input voltage swing, as shown in Figure 10, is approximately ± 2 V, resulting in an output change of some 400 mV. This is again equivalent to an accuracy of approximately 4 bits.

b. Performance Evaluation of the Processor.

The processor has been tested on true two-dimensional imagery using both a stored data base and a real-time input from a commercial vidicon. The use of a stored data base allows most of the problems associated with

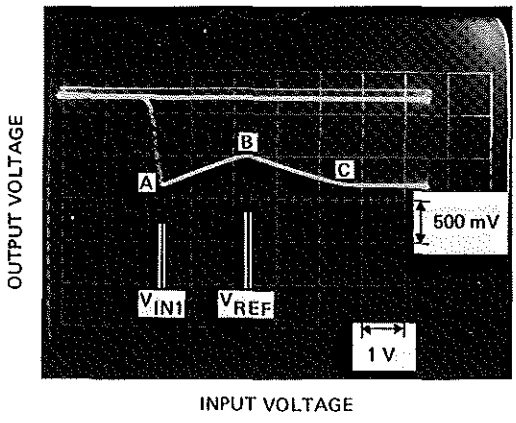


Figure 10. Transfer characteristic of absolute value circuit.

the sensor, such as illumination, resolution, and signal-to-noise ratio, to be separated from the evaluation of processor performance. The maximum data rate of this system, however, is limited to about 30 kHz. In this mode, the imagery to be processed is first digitized and stored in the computer memory, as shown in Figure 7. (In practice, a very large data base is available on magnetic tape and has been used extensively in the performance evaluation.) The stored data are then clocked out of the random access memory in synchronism with the CCD clocks and converted to analog data before entering the processor. The processed data from the CCD are converted again to digital format and stored in the computer memory in the form of 128 x 128 four bit words. Direct memory address is then used to refresh a standard video monitor.

An example of this is shown in Figure 11 for a two-dimensional test pattern. A comparison of the output (Figure 11(b)) with the computer simulation (Figure 11(c)) shows that an accuracy of approximately four bits is preserved. An example of its operation on a real image is shown in Figure 12.

In addition to the tests on stored data, we have interfaced the processor directly with a commercial vidicon camera. The standard operating frequency of this "real-time" video is ≈ 7 MHz, providing 525 x 525 picture elements at 30 frames/sec. At present, we have operated our CCD processor at a maximum clock rate of 4 MHz, which provides the full 525 vertical resolution elements but about a three-to-one resolution loss in the horizontal direction. An example of the performance in both the local-averaging and the edge-detection modes is shown in Figure 13. Two other functions, unsharp masking and binarization (both of which are performed in real-time by our CCD processor), are also shown.

5. Conclusions

The concepts and design details of a CCD image processor that performs two-dimensional linear and nonlinear operations are discussed. Our results indicate that it is feasibile to use a CCD integrated circuit approach for the image preprocessor. The operations described are used as the basis for higher-level syntactic type of image processing, which is becoming

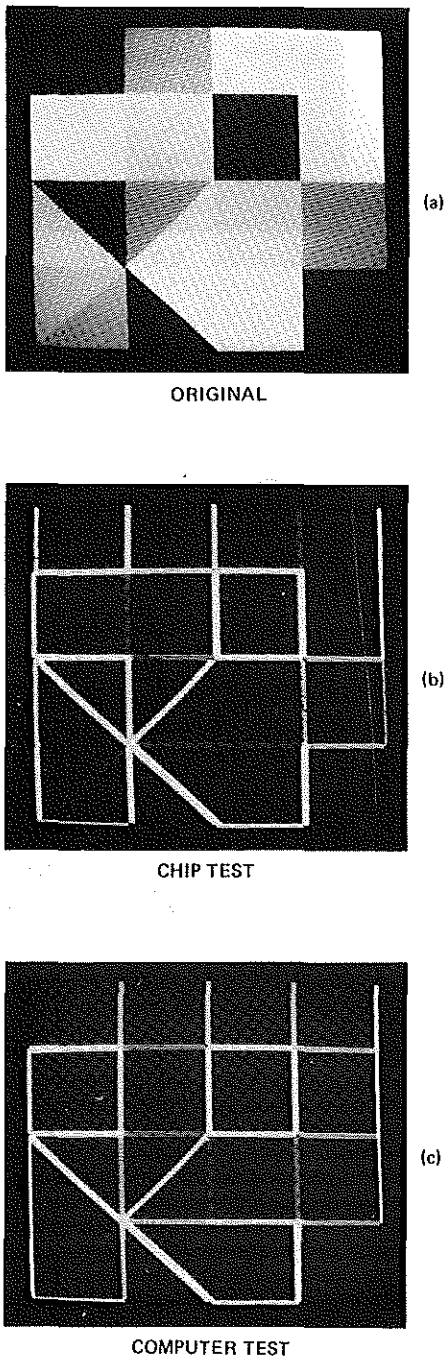


Figure 11. Example of processor operation on stored test data (at 30 kHz).

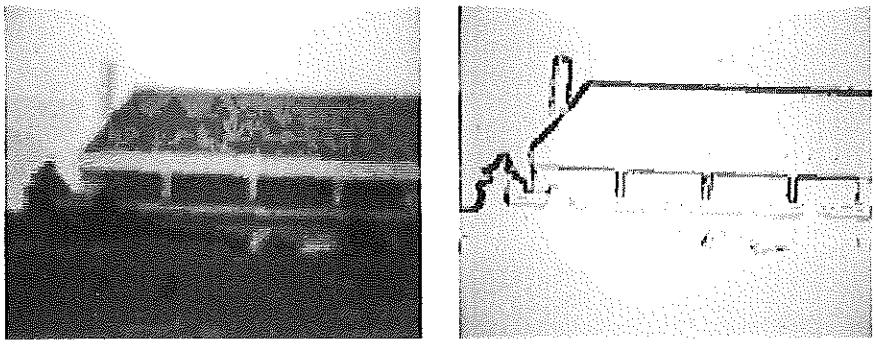


Figure 12. Example of processor performance operating on stored imagery.

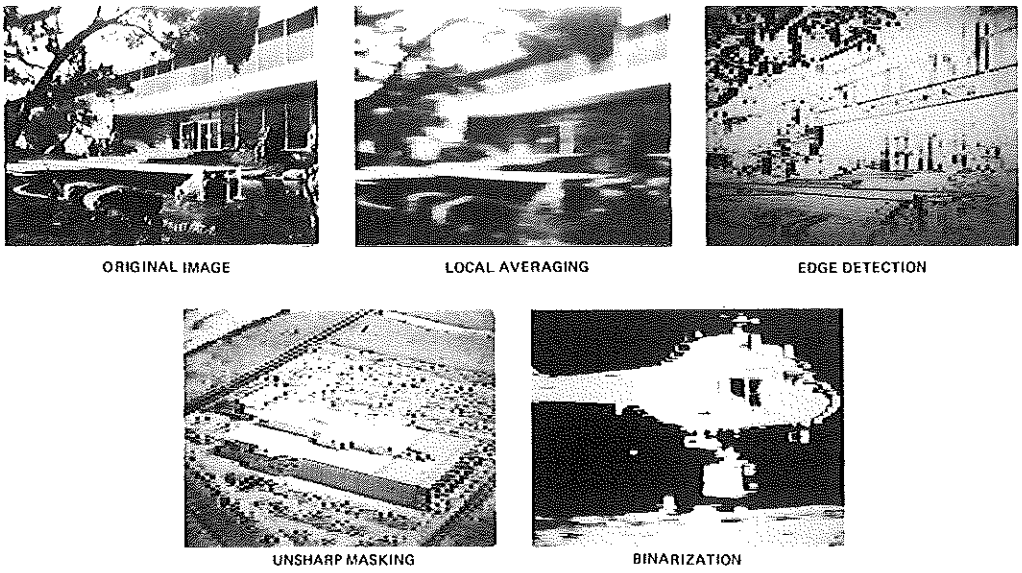


Figure 13. Performance of processor at real-time data rates.

increasingly important in military systems for target acquisition and tracking. Typically, however, most of the processing time is taken up in the "preprocessing" type operations, and our present indications are that the CCD techniques are able to operate with at least 4-bit accuracy at speeds 100 to 300 times faster than the conventional general-purpose processor used to date.

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