Digitally controlled adaptive CCD filter

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Abstract

The computation and setting of the coefficients of adaptive CCD transversal filters can be delegated to a microprocessor. The information required for setting the filter coefficients is put out in digital form. For the adaptive CCD transversal filters known so far, D/A converters have to be used to convert this information into analog values by which the input signal can be multiplied.

Thus a new adaptive filter was implemented using a CCD transversal filter with parallel-in/serial-out configuration in combination with a digitally controlled weighting scheme for the various filter coefficients. At each input stage a charge packet proportional to the input signal is transferred n times to the collecting CCD electrode, where the number n of transfers determines the tap weighting of each coefficient. With this configuration a combination of analog and digital multiplication was realized. This filter can thus be advantageously combined with microprocessors.

The concept for a novel solution of this type, the realized configuration and the mode of operation of the D/A converter in the input stages of the CCD will be described below. Measurements on an implemented filter network with 25 digitally controlled coefficients are reported and discussed.

1. Introduction

Whereas for many applications it is possible to specify a fixed frequency response for a filter network, it is in other cases more practical not to adapt the filter unless it is to be used for a specific problem and then if necessary to adapt it again if the input parameters change. Such requirements are encountered for instance with modems if the data signals transmitted over the telephone line have to be equalized /1,2/. Whereas with small systems it is still possible to adapt the filters by hand, this would no longer appear practical for fast and complex filter networks. In such cases a filter can only be meaningfully used in conjunction with a main processor capable of executing the algorithm for the filter calculations at sufficient speed.

For electrically controllable filters such as those known from the literature /3/ the digital information of the main processor has to be converted by D/A converters /4/ to allow multiplication with the signal value. If however a CCD transversal filter with parallel-in/serial-out configuration is used, the digital information can be used for directly controlling the input stages. The required D/A conversion is here delegated to the CCD in the sense that a charge packet proportional to the signal value is read repeat-

edly into the CCD channel from each input stage in correspondence with the digital information for the respective input.

2. Overall system

The various circuit elements required for an adaptive filter system are shown in Figure 1. The overall system is controlled by a microprocessor. A first approximation for the filter coefficients is created by the microprocessor and then written into the various storage registers. During this process the various registers are individually accessed via the address bus and the decoder, and the value of the respective filter coefficient, e.g. an 8-bit value, is read in over the data bus. The information stored in the registers is now compared by comparators with the count of a counter which counts during the time interval between two sensed values of the input signal up to a specified number 2^m. This number determines the maximum possible number of read-in pulses per read-in cycle. If the count is greater than the actual value in one of the register, the output of the respective comparator is cut off, thereby blocking the connected CCD input. The value of this coefficient is in this way determined by the clock pulses before the comparator is disabled.

This allows a close connection between the microprocessor and the adaptive filter. The only connecting links required are the decoder, the storage register and the comparators. A rough estimate of the real estate required for an integrated implementation of these connecting elements for a filter with 50 coefficients is 2 mm^2. In order to be able to read the information required for the optimization into the microprocessor, a link has to be established between the filter and the microprocessor by way of an A/D converter. The microprocessor must have a suitable algorithm allowing the fast computation of the optimum coefficients for a given problem. The computation only requires weighting with "+1" and "-1" and additions /2/, i.e. arithmetic operations which are relatively fast in comparison with digital multiplications.

For improving the filter characteristics the value of one or more coefficients supplied by the microprocessor can be read selectively into the register and the result of this alteration recorded at the filter output and evaluated anew.

3. Realized configuration

Realization of the proposed adaptive filter system is based on the assumption of the availability of a large variety of suitable microprosessors. Decoder, register and comparators can be in form of discrete devices or integrated on the chip according to available solutions. Thus only the CCD transversal filter with parallel input stages in which D/A conversion takes place (Figure 2) was implemented. The filter is controlled via external comparators, a register and a counter.

A CCD for 4-phase operation with 43 elements was implemented in two-layer Poly-Si gate technology on a real estate area of about 2 x 3 mm^2. The CCD electrodes have a lenght of 10 μm; on both sides of every fourth CCD electrode there is an input stage with an electrode area of 5 x 5 μm^2. Two parallel input stages are required in the implemented system to allow the positive or negative weighting of the input signal according to need. To simplify the control of the system the coefficients were interconnected symmetrically with reference to the center. This results in filters with a constant group delay. The output signal of the filter can be sensed either as a charge packet or, via a source follower, as a voltage. An external amplifier has been added behind the source follower so that the signal can be amplified accor-

ding to need.

4. Structure of input stage

4.1 Realized input stage

The realized form of the input stage is shown in Figure 3. The charge is applied by the fill-and-spill method /5/. Each input stage consists of an input diode I_D, two gate electrodes G1 and G2 (see Figure 4) at which there is either the signal or a bias voltage, and the gate electrode G3 with which the number of charge packets to be applied is determined. To realize a positive or negative sign /6/ for the various coefficients one of the two different bias voltages B1 or B2 can be applied to the bias line, which for inputs associated with a CCD electrode is connected on one side of the channel to G1 and on the other side to G2. When the bias voltage B1, which is smaller than the minimum voltage of the input signal, is applied, no charge is able to flow into the input seen on the right in Figure 3b. On the left however a charge packet builds up and is transferred in the CCD channel, which is proportional to the signal, with the result that a positive sign is obtained. If the bias voltage B2, which is larger than the maximum voltage of the input signal, is applied to the bias line, no charge will flow into the input on the left in Figure 3c, whereas a charge packet builds up on the right that is inversely proportional to the input signal, with the result that a negative sign is obtained.

4.2 Input stage with positive and negative weighting

As an extension of the realized solution it would appear practical to realize the input such that both positive and negative coefficients can be realized with one input stage so that each register can store not only the value of the respective coefficient but also its sign with a single bit. A simple logic configuration (Figure 4) can then be used for applying either the signal or one of the two bias voltages B1 and B2 to the gate G1 or G2 in order to obtain the desired sign.

5. D/A converter

5.1 Mode of operation of D/A converter

Multiplication of the input signal by the values supplied by the microprocessor takes place in the parallel input stages of the CCD. The input signal is sensed at the beginning of the read-in cycle and its value determined. Charge packets proportional to the value of the sensed signal build up in the various input stages and are shifted into the CCD channel. The time required for reading in a charge packet depends on the geometry of the input stage. For the chosen input stage with an electrode lenght of 5 µm it is, according to /7/, theoretically possible to realize a read-in frequency of the order of 8 MHz with an accuracy of 8 bit. Measurements showed however the amplitude of the output signal to diminish at read-in frequencies above 2 MHz. This effect is mainly due to the clock voltages showing up distortions at these high frequencies.

5.2 Calculation of accuracy of D/A converter

The quality of the D/A converter depends not only on its read-in time, which is given by its geometry, but also on the time of the read-in cycle. This time is determined by the CCD clock frequency. The accuracy of the D/A converter can be determined on the basis of the knowledge that if an asymmetrical CCD clock program is chosen about 80 % of a clock cycle will be available for read-in. To realize a D/A converter with 8 bit accuracy, for instance, the CCD clock frequency for a read-in frequency of 8 MHz can not be above 30 kHz.

Measurements with our test circuit

were unable to show this result because the input frequency was limited to 2 MHz and, as the coefficients were externally controlled, no more than a hundred read-in pulses could be set.

6. Linearity of input stage

For investigating the linearity of the input stage of the realized configuration both the amplitude and the dc voltage component of the input signal were varied and the number of charge packets read into an input stage was altered.

6.1 Linearity as a function of the input signal

For investigating the linearity of the input stage as a function of the input signal, the output signal was measured as a function of the value of the input signal for both positive and negative coefficients. Figure 5 shows linearity to exist in the region between the two bias voltages B1 = 1 V and B2 = 3 V.

For obtaining a precise measurement of the linearity a sinewave signal with an amplitude of 0.25 V was applied and the dc voltage superposed on the sinewave was varied between 1 and 3 V. The measured separation between the fundamental (f_1) and the second (f_2) and third (f_3) harmonics is shown in Figure 5b, c for both a positive and a negative input stage. The maximum seperation between the fundamental and the second harmonic for both the positive and the negative input stage was measured to be 42 dB. It is felt that this is mainly due to the minimum geometry of the input stages.

6.2 Linearity as a function of the number of read-in pulses

The relation between the value of the output signal and the number of charge packets transferred from an input stage into the CCD channel per read-in cycle was also measured. For this purpose a dc voltage of 2 V was applied to the input and the number of read-in pulses varied between 0 and 99 (Figure 6). These measured points fit the transfer characteristic of the output stage - measured with a seperate method - very well.

7. Realization of a lowpass filter

To demonstrate the applicability of our circuit concept to filters a lowpass filter was realized. The required filter coefficients were determined with the aid of a computer program /8/ and then rounded off to integral values between -99 and +99. To simply control of the filter only 25 of the 43 realized coefficients were used. The filter was operated with a clock frequency of 10 kHz. According to the calculations (Figure 7a) the deviations in the passband of 0 to 1 kHz should be smaller than $\pm$ 0.1 dB and an attenuation of at least 32 dB should be present in the stopband starting at 2 kHz.

The recorded curves in Figure 7b show this response to have been satisfactorily realized in the passband. Although the attenuation in the stopband agrees with the calculations, a discrepancy is to be noted between the computed and the recorded curves. This discrepancy is probably influenced by inaccuracy of the filter coefficients and by transfer inefficiency within the CCD.

The agreement between the recorded and the computed curve can be demonstrated more clearly by choosing an example in which the attenuation in the stopband is smaller. A corresponding frequency response was calculated by increasing the absolute value of all the coefficients by three read-in pulses per cycle. The choice of these non-optimum coefficients leads to variations in the passband of $\pm$ 1 dB and the attenuation in the stopband is now no more than 22 dB. This may be seen from both the calculated frequency response (Figure 8) and the recorded curve, which is consistent with the calculated values.

To measure the linearity and random noise of the adapted filter a sine-wave signal with an amplitude of 0.5 V on which a dc voltage of 2 V was superposed was applied to the input of the filter, whose frequency response is shown in Figure 7. A separation of about 40 dB between the fundamental and the second and third harmonics was measured (Figure 9). The random noise was measured with only the dc voltage of 2 V at the input; for a window of Δf = 300 Hz the random noise was 64 dB below the signal amplitude.

8. Concluding remarks

The described digitally controlled filter is a transversal filter that is particularly suitable for combination with the microprocessor. According to the theoretical calculations it is possible, assuming a clock frequency of 30 kHz, to realize a D/A converter with 8 bits in the input stages of the configuration. Using this configuration a lowpass filter with an attenuation of more than 42 dB was implemented. In order to expand the configuration into an adaptive filter system the possibility of integrating the required connecting links such as the decoder, the register and the comparators on a single chip is being contemplated as the next step.

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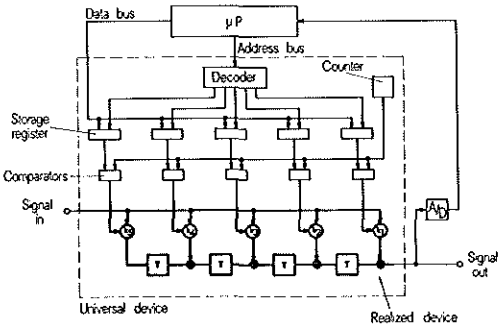

Fig. 1 Overall system of an adaptive filter network

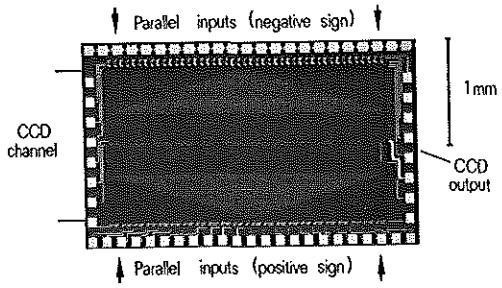

Fig. 2 Digitally-controlled CCD transversal filter as test device with 43 coefficients

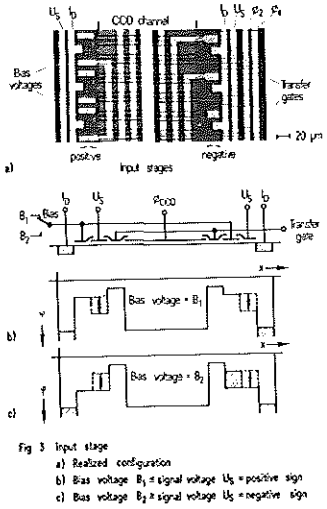

Fig. 3 Input stage
a) Realized configuration
b) Bias voltage B_1 = signal voltage U_S = positive sign
c) Bias voltage B_2 = signal voltage U_S = negative sign

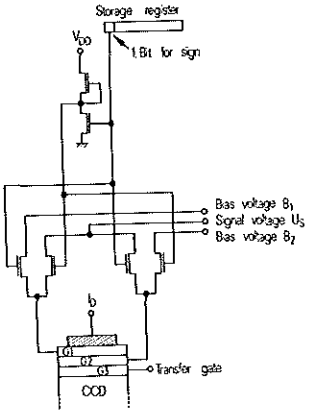

Fig. 4 Drive circuit for input stage with positive or negative sign

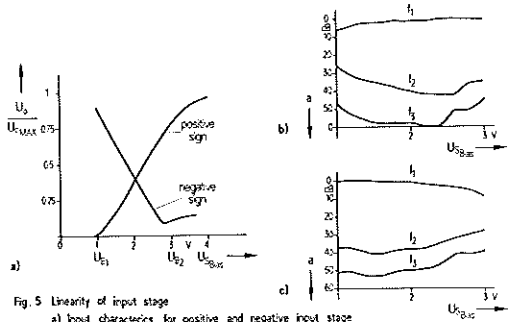

Fig. 5 Linearity of input stage
a) Input characterics for positive and negative input stage
b) Linearity of positive input stage $\hat{U}_S$=0.25 V
c) Linearity of negative input stage $\hat{U}_S$=0.25 V

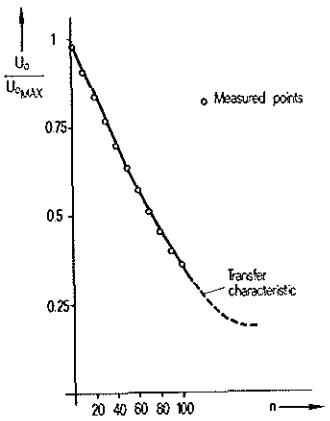

Fig. 6 Measured output voltage as function of the number of read-in pulses

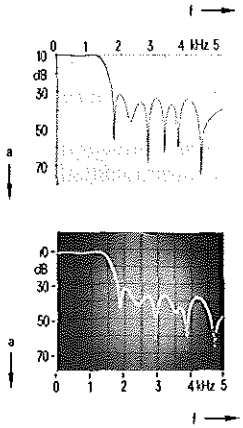

Fig. 8 Calculated and measured frequency response of a filter with non-ideal coefficients

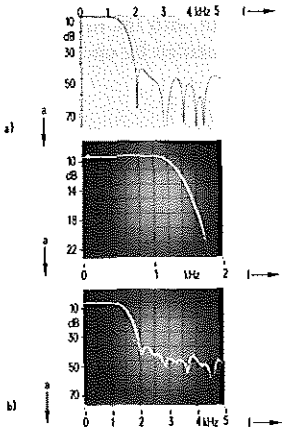

Fig 7 Realized lowpass filter
a) Calculated frequency response
b) Measured frequency response in passband and stopband

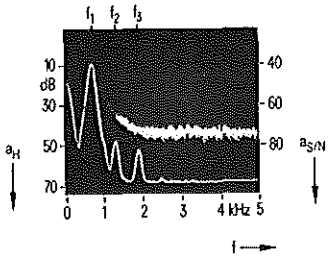

Fig. 9 Harmonic attenuation a_H and signal to noise ratio $a_{S/N}$ (noise per 300 Hz) of a realized lowpass filter