# A CCD/NMOS CHANNEL VOCODER*

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## ABSTRACT

The need for security in voice communication is met by converting voice to digital form so that sophisticated digital encryption is possible. Of course, it is very desirable that the digital voice signal be compatible with conventional 3 kHz analog voice transmission bands, hence the vocoder which converts analog voice signals to digital form must employ some form of bandwidth compression to yield data rates down to 2.4 kbits/sec. Linear prediction techniques are commonly used to implement vocoders in essentially all-digital systems, but with current technology such systems are expensive, fairly large, and consume large amounts of power. This paper concerns the application of CCD technology to the vocoder problem using a second much older approach, the channel vocoder. The objective is to demonstrate the potential of analog CCD technology to achieve a low cost, low power vocoder system. Two custom design CCD/NMOS integrated circuits are the key to this approach and the design of these circuits will be reviewed in this paper.

## I. INTRODUCTION

Speech signals are well matched to the capabilities of both CCDs and switched capacitor filters. The applications of speech processing systems are presently expanding very rapidly and include such areas as vocoders, speaker verification systems, word recognition, computer generated speech, and many others. The compatibility of CCD and switched capacitor filters with large scale integration promises to have significant impact in lowering the cost and in accelerating the uses of complex speech processing systems. This paper concerns the development of two speech processing ICs utilizing analog CCDs and switched capacitor filters. These ICs are intended for use in a 2.4 kBPS channel vocoder although the devices are compatible with other uses as well.

The function of this vocoder system is to reduce the data rate of speech transmission to 2.4 kBPS while maintaining high quality and intelligibility in the reconstructed speech signal at the receiver. The block diagram of the system is depicted in Figure 1. This integrated system is a channel vocoder based on a system and algorithm developed in the UK.[1] The two portions of the system which are enclosed in the dashed lines in the figure are being implemented with two custom designed CCD/

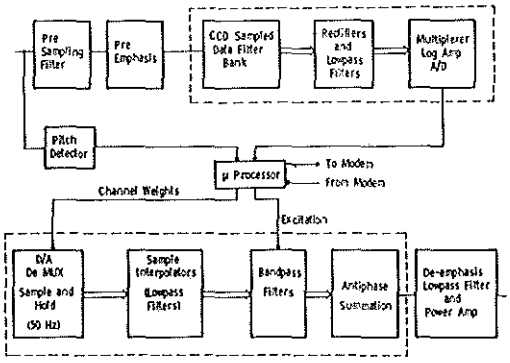


Figure 1. Block diagram of a channel vocoder based on two custom IC functions enclosed in dashed lines.

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NMOS integrated circuits, while the remaining functions are implemented with a few simple analog components and five TMS 9940 microcomputer circuits. One of these two special circuits is used for speech analysis and the other for synthesis. Three of the TMS 9940 microcomputers are used to implement a modified Gold-Rabiner pitch tracker.[2] The other two TMS 9940s control the analyzer and synthesizer and interface the modem.

The basic operation of the channel vocoder is to determine periodically (every 20 msec) the spectral envelope of the speech using a filter bank. The nature of the excitation of the speaker's voice (either a periodic pulse train for voiced sounds or a random noise source for unvoiced sounds) is determined by a pitch tracker. These parameters are encoded into a compact digital code and transmitted to the receiver which then synthesizes a signal having approximately the same spectral envelope. The synthesizer uses a filter bank excited by either a periodic pulse train or random noise where the gain parameters of the filter bank, the selection of the excitation, and the pulse period are controlled by the information from the transmitted signal. The vocoder takes advantage of the fact that phase information is relatively unimportant in man's perception of speech sounds.

In the next section of this paper the voice analysis IC will be described. Several of the key circuit techniques used will also be discussed. In Section 3, the voice synthesis IC will be described. A summary appears in Section 4.

## 2. VOICE ANALYSIS IC

### 2.1 Functional Description

A simplified block diagram of the analyzer IC is shown in Figure 2. The chip contains a bank of 19 channels. Each of the channels consists of a bandpass filter followed by a half wave rectifier and lowpass filter. The 19 bandpass filters span the frequency spectrum from 180 Hz to 4.1 kHz. The ideal frequency response of the analyzer filter bank is plotted in Figure 3. Each channel output is thus a measure of the energy in the corresponding spectral range. The 19 channels are sampled once every 20 msec and then sequentially multiplexed into an A/D converter having a logarithmic response. A 5-bit digital code with 1.5 dB steps is thus generated for each of the 19 segments of the spectrum. The chip also contains the necessary clocks and timing circuitry to interface the microprocessor system.

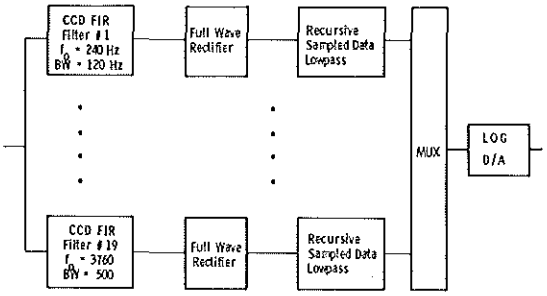


Figure 2. Block diagram of the channel vocoder speech analysis IC

The bandpass filters of the analyzer chip are implemented with 100 stage CCD transversal filters employing the split electrode charge sensing scheme.[3,4] The transfer function of the CCD was designed to approximate that of a second order Butterworth bandpass filter shown in Figure 3.

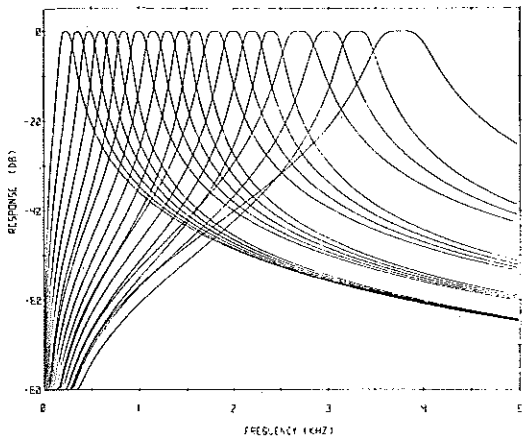


Figure 3. Frequency response of the 19 channels of the speech analyzer filter bank.

The Butterworth characteristic and the expected CCD response are plotted in Figure 4 for one of the channels. A slightly modified version of the Parks, McClellan, Rabiner design program [5] was used to compute the CCD coefficients. It is interesting to note that while the desired transfer function in this case can be implemented with only two complex pole pairs, it takes 100 zeros in the transversal filter to achieve a good approximation. Yet the 100 stage CCD filters and their associated output amplifiers require only one op amp each while second order switched capacitor bandpass filters require two to four amplifiers and thus more power.

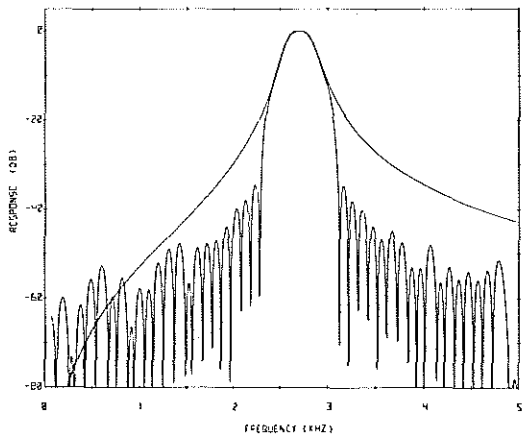


Figure 4. CCD filter response for a typical channel in the vocoder analyzer with a second order Butterworth characteristic superimposed. The band center is 2700 Hz and the 3 dB bandwidth is 330 Hz.

## 2.2 Circuit Implementation

### 2.2.1 Analyzer CCD Filters

The CCD filters are fabricated using a four phase, double poly, co-planar electrode structure. The clocking scheme [6] is illustrated in Figure 5. Two of the electrodes $\phi_1$ and $\phi_2$ are clocked with overlapping 15V clock wave forms at a 10 kHz rate while $\phi_3$ is used as a barrier biased at 2V DC and the split electrode sense lines are biased at 8V by the output circuit. The output sensing circuit is shown in Figure 6. An operational amplifier having differential outputs is used along with two feedback capacitors $C_f$ to perform the differential current integration function required for split electrode CCD filters. The gain of the CCD filter is controlled by the size of the poly-poly feedback capacitors along with the weighting coefficients of the filter. The capacitor size in each of the 19 filters was adjusted for the same in-band gain.

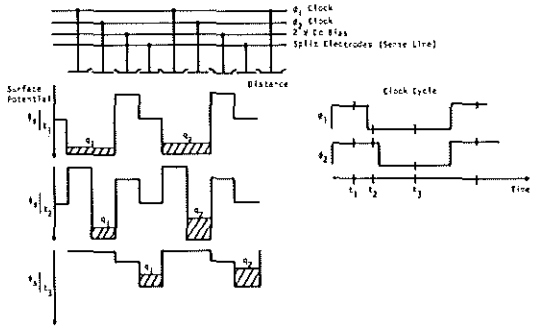


Figure 5. Schematic diagram of the CCD charge transfer process & clock timing.

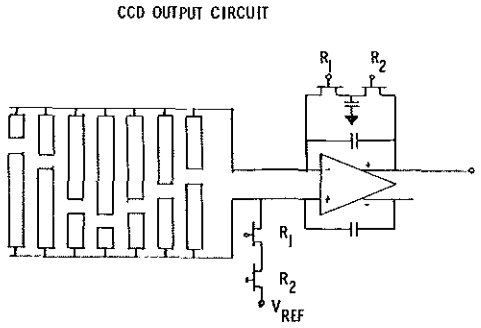


Figure 6. CCD filter output circuit.

### 2.2.2. Analyzer Rectifiers

The bandpass filtered signals are rectified by the half wave rectifier circuit shown in Figure 7. This circuit takes advantage of the sampled data nature of the CCD output signal in order to establish a reference level with low offset. The rectifying action is obtained by using the MOS transistor M8 to charge capacitor $C_2$ to the cutoff point of the transistor. The differential amplifier formed by $M_3$ - $M_7$ and the associated depletion load current sources $M_{11}$ - $M_{13}$ is used as a comparator to achieve sharper

cutoff characteristics. Once each cycle the reset clocks $R_1$, $R_2$ and $R_3$ are turned on.

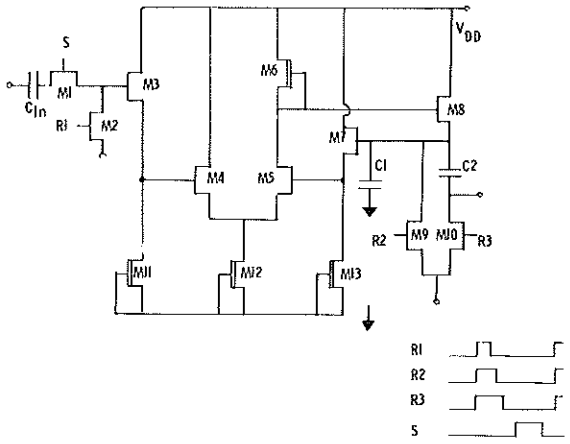


Figure 7. MOS half wave rectifier

This connects the input to a fixed reference and also discharges the output capacitors $C_1$ and $C_2$. The turnoff edges of the clocks are staggered in time with the result that offsets due to the turnoff of the reset clocks are stored on the capacitors. After the reset cycle the sample pulse S is turned on and the input is applied through the coupling capacitor $C_{IN}$. The stray capacitance on the gate of $M_3$ and the alternate switching of $M_1$ and $M_2$ forms a switched capacitor resistor.[7,8] This resistor and capacitor $C_{IN}$ effectively AC couple the input signal. If the input voltage is positive with respect to the reference level the output node will be pulled up by $M_8$ through capacitor $C_2$. If the input sample is negative with respect to $V_{ref}$ $M_8$ remains cutoff and the output remains unchanged. Experimentally we find that the circuit has approximately 10 mV offset which is adequate for this application.

### 2.2.3 Analyzer Lowpass Filters

After the signal for each channel is rectified, it is lowpass filtered with three pole Butterworth filters having a 35 Hz bandwidth. In this case the area advantage was clearly in favor of the switched capacitor filter approach rather than CCD filters, so these filters are implemented with switches, capacitors, and simple source follower circuits. The filter is shown in Figure 8, where the source followers are indicated by gain blocks with gain of 0.9 and the MOS transistors used in the switched resistors are indicated as switches. The real axis pole is implemented with the capacitor $C_1$ and $C_2$ and buffered by the first gain stage. This part of the filter is operated at the same 10 kHz clock rate as the CCD bandpass filters. In order to save area the second stage of the lowpass filter which provides a complex pole pair is clocked at 1 kHz and uses the first stage as an antialiasing filter. In order to eliminate dc offsets in the lowpass filter, the energy storage elements of the filter are periodically disconnected from the source followers and other switches (not shown) are used to allow the followers to be cascaded with the reference voltage applied at the input. During this time interval the offsets of the followers are sampled and stored on a coupling capacitor at the filter output.

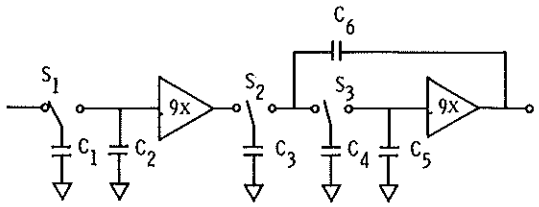


Figure 8. Schematic diagram of a 3 pole lowpass filter implemented with switched capacitors. The capacitor values are: $C_1$ = 0.50 pF, $C_2$ = 22.4 pF, $C_3$ = 1.53 pF, $C_4$ = 1.00 pF, and $C_6$ = 15.0 pF.

### 2.2.4 Logarithmic A/D Converter

The signals from the 19 channels are sequentially multiplexed into the logarithmic A/D converter which provides a 5 bit code at a 1 msec rate. The step size in the converter is 1.5 dB. A simplified schematic of the converter is shown in Figure 9. The operating principle of the device is similar to the charge redistributor A/D converter.[9] A binary weighted capacitor array made of poly-poly capacitors is used to obtain 6dB increments while a polysilicon resistive

divider is used for the 1.5 dB steps. The cycle of the converter is initiated with all switches at the reference position. During this interval the switched resistor is clocked with two nonoverlapping clocks R and S which provide DC feedback around the comparator and stores the comparator offset on the capacitor array. Subsequently the input capacitor $C_{IN} = 2Co$ is switched from the signal reference to the input signal which causes a negative going charge in the common node of the capacitor array. Then using a successive approximation algorithm the other capacitor switches are selectively switched to the reference voltage line (node A in the figure) causing positive going steps on the common node. After the nearest 6 dB increment is found using the capacitor switches node A is switched to the nearest 1.5 dB increment on the resistive reference divider. Where a conversion cycle is completed the 5-bit code is latched into TTL output buffers and held until the output for the next channel is ready. A data ready pulse is also provided to synchronize the microprocessor.

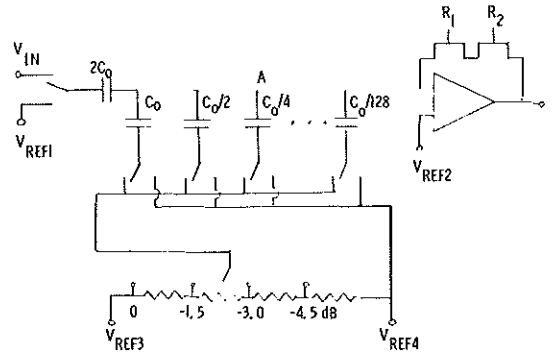


Figure 9. Simplified schematic of the logarithmic A/D converter

## 3. Voice Synthesis IC

### 3.1 Functional Description

A block diagram of the speech synthesizer IC is shown in Figure 10. The input to this chip is a sequence of 20 8-bit digital words at a rate of one per msec. One of these words controls the selection of voiced or unvoiced V/U excitation on the chip which is either a pseudorandom sequence or a pulse generator whose period is controlled by the data in the excitation word. This excitation word is recognized by nonzero bits in the three MSB positions and it also serves the function of speech frame synchronization. The remaining 19 words of input data all have zeros in the three MSB positions and the five LSB lines are directed to an anti-logarithmic D/A converter. The output of the D/A is demultiplexed to 19 sample and hold circuits, one for each of the synthesis channels. Each of the synthesis channels consists of a three pole lowpass filter, a modulator, and a bandpass filter. The lowpass filter provides interpolation between the speech frames, and its output is used to modulate the amplitude of the excitation pulses which are applied to the bandpass filter of the corresponding channel. The outputs of the 19 channels are then summed together with every other channel having the opposite polarity in the sum. The reason for the anti-phase summation is to avoid large output pulses which could result from coherent responses of all of the channels and would require a larger dynamic range in the output amplifier. As we noted earlier, the relative phase of the different parts of the speech spectrum is not important in speech perception.

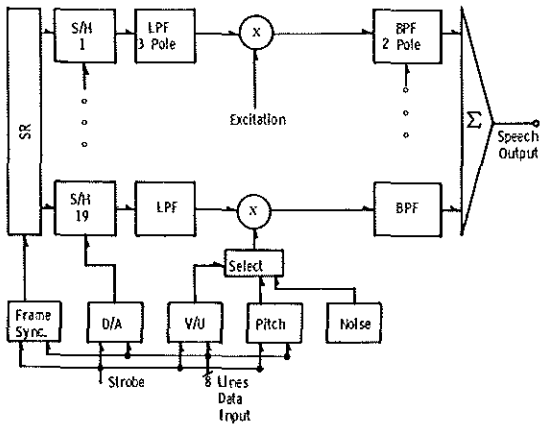


Figure 10. Block diagram of a channel vocoder speech synthesis IC.

### 3.2 Synthesizer Circuit Implementation

#### 3.2.1 Logic Circuits

All of the logic functions shown in the block diagram of the synthesizer in Figure 10 are implemented with standard NMOS 5V de-

pletion load circuits. For the excitation, either a pitch word is loaded into an eight stage counter which provides periodic pulses with 100 μsec resolution in the period, or a 16 stage shift register is used to provide a $(2^{16}-1)$ length pseudorandom sequence. A 40 kHz single phase clock signal is input to the chip and all other clocks are derived from it.

### 3.2.2. Demultiplexer, Anti-logarithmic D/A, and Lowpass Filters

The sample and hold circuits and demultiplexing were implemented using MOS switches as gates and using MOS capacitors for storage. Precision gain is not required so buffer amplifiers in the sample and hold circuits are simply source followers. The lowpass filters employed are similar to those used in the speech analyzer described above. The lowpass filtered envelope is modulated by a bank of switches controlled by the excitation. These switches simply connect the bandpass filter inputs to the lowpass filter outputs when a pulse is desired and otherwise leave the bandpass inputs connected to a reference dc level.

### 3.2.3 Bandpass Filters

In the synthesizer the bandpass filter characteristics are simpler than those in the analyzer. They are simple complex pole pairs resulting in high Q resonant circuits with the same center frequencies as the corresponding analyzer channels. These characteristics would require approximately 150 stages in CCD transversal filters, but can be implemented with only two operational amplifiers and switched capacitors. Each filter implemented this way occupies only .48 $mm^2$ of silicon making it possible to build the entire synthesizer IC in approximately 32 $mm^2$, including all clocks, the D/A, the excitation pitch counter and noise generator, the filters and the summing output amplifier.

In order to understand the switched capacitor bandpass filter operation we examine first a conventional integrator, then a sampled data integrator and its z-transform, and finally a second order section will be described. Following the analysis of reference 7, a conventional analog integrator is shown in Figure 11a. Its transfer function is

$$H(\omega) = -\frac{1}{j\omega R_1 C_2} \qquad (1)$$

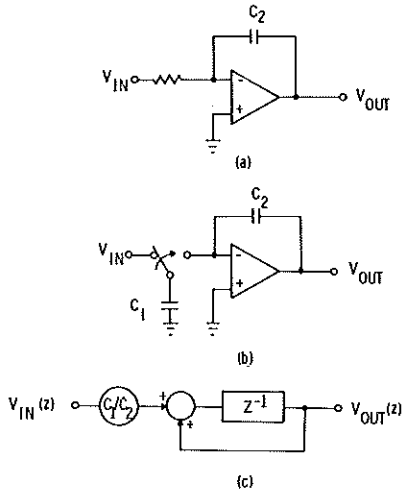


Figure 11. a) Conventional RC integrator, b) Sampled data integrator, c) Z-transform of integrator in (b).

In Figure 11b we have replaced $R_1$ with a double throw switch and capacitor $C_1$. This circuit operates in a sampled data mode with the switch alternating at a clock period $T_c$ between the left hand position shown in Figure 11b to the right hand position. In the nth clock cycle, the capacitor $C_1$ is first charged to the voltage $v_{in}(n\,T_c)$ is effectively transferred to capacitor $C_2$. The following difference equation describes the process.

$$C_2\, v_{out}[nT_c] = C_2\, v_{out}[(n-1)T_c] - C_1 v_{in}[(n-1)T_c] \qquad (2)$$

The z-transform for this circuit can be written in the form

$$H(z) = -\frac{(C_1/C_2)\, z^{-1}}{1-z^{-1}} \qquad (3)$$

which can be recognized as the equivalent of a digital integrator.

This integrator forms the basis of many possible filter configurations. [7, 10] The one selected for this application is shown in Figure 12. Two integrators can be seen in the figure. One is formed with the capacitors $\alpha_L C_L$ and $C_L$ and the other by $\alpha_c C_c$ and $C_c$. A sign inversion is accomplished by adding a second switch to the bottom plate of capacitor so that the polarity can be reversed

when discharging this capacitor into its corresponding integrator. The z-transform of this circuit can be written as

$$\frac{V_{out}(z)}{V_{in}(z)} = \frac{-\alpha_I \alpha_C (z-1)}{z^2 - (2-\alpha_C\alpha_T-\alpha_C\alpha_L)z+(1-\alpha_C\alpha_T)} \quad (4)$$

We can see from the z-transform that the frequency response is independent of the absolute values of either $C_C$ or $C_L$, but depends only on the capacitor ratios $\alpha_C$, $\alpha_L$, and $\alpha_T$. MOS fabrication techniques allow the control of such capacitor ratios to a precision on the order of 0.1% which is adequate for many filtering problems including the one described here.

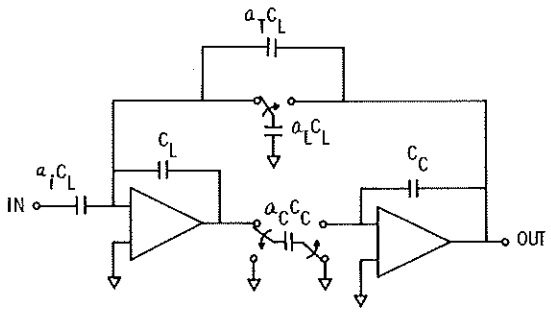


Figure 12. Two pole bandpass filter using switched capacitor integrators.

### 3.3.4 Operational Amplifiers

The key to successful switched capacitor filters is an NMOS operational amplifier with low power and small silicon area. Recently various NMOS amplifier designs have been reported [11, 12] and the design of the amplifier used in the bandpass filter has incorporated ideas from the previous designs. However, this amplifier was optimized for small silicon area and low power. The amplifier circuit topology is shown in Figure 13. The principle specifications are listed in Table I. There are 41 of these amplifiers on the speech synthesizer IC.

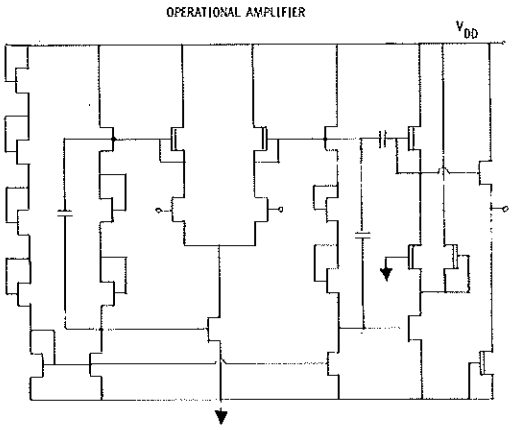


Figure 13. NMOS Operational Amplifier

TABLE I

Operation Amplifier Characteristics

| | |
|---|---|
| Power | 4.3 mW |
| Gain open loop | 1800 |
| Bandwidth | 1.6 MHz |
| Slew rate | 2.2V/μsec |
| Load | 10 pF |
| Phase Margin | 56° |
| Silicon Area | .09 $mm^2$ |

## 4.0 Summary

CCDs and the complementary and compatible switched capacitor filter technology show promise in lowering system size, cost, and power. The two custom analog LSI circuits described in this paper make possible a highly integrated, potentially low cost solution to the vocoder problem. There are many other system problems utilizing speech analysis and/or synthesis in which these ICs could find application, thus further lowering costs. Speech signals are well matched to the dynamic range and speed capabilities of this technology. In this case it is possible to perform much of the signal processing required for the intrinsically analog speech signal while it remains in analog form. This technology can achieve very high density for such functions.

In the future we can expect to see further refinement of analog LSI techniques using this technology for speech and many other applications. Digital systems will of course never be entirely replaced by analog systems, however, the optimal interface boundary between digital and analog approaches may become more flexible as these developments are realized.

## 5.0 References


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