GaAs CCD WITH HIGH TRANSFER EFFICIENCY

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ABSTRACT. A Schottky barrier gate GaAs CCD has been successfully operated with high transfer efficiency. This CCD structure in GaAs offers the potential of ultra high speed signal processing devices as well as near-infrared and visible imaging CCD's.

1. INTRODUCTION

Over the past few years, vigorous development effort has brought silicon charge coupled device (CCD) technology to the point where widespread applications in signal processing and imaging have become practical. The technological maturation of Si CCD's has also brought the realization that there are certain limitations, particularly in speed and charge storage time, that could not be overcome. GaAs and related III-V compound semiconductors show promise for overcoming the fundamental limitations on CCD performance imposed by silicon material properties. Research on GaAs CCDs has, however, been hampered by the persistently high surface state densities and instability in GaAs MIS (metal-insulator-semiconductor) structures. Non-MIS gate CCDs have been previously proposed[1]. A new GaAs CCD structure employing Schottky barrier gates has recently been demonstrated.[2,3] Charge transfer efficiency in excess of 0.999 per transfer has been measured on this device,[4] making it the first CCD in a material other than silicon in shich high transfer efficiency has been demonstrated. Improved performance in GaAs based CCD is expected because of better material properties and greater flexibility in device design.

The 4 to 5 times larger low-field mobility of electrons in n-type GaAs over silicon is the principle contributor to higher speed GaAs devices. In a buried channel CCD (such as the Schottky gate GaAs CCD) which is designed for the "peristaltic" mode of operation, the higher GaAs electron mobility results in higher speed transfer from one gate to the next. High transfer efficiency at speeds well in excess of 1 GHz is possible. A second consequence of the high mobility for high speed CCDs is the bandwidth of the on-chip read-out amplifier. In order to operate a CCD at sample rates approaching 1 GHz, the bandwidth of the on-chip amplifier must be several GHz. This is the principle reason that silicon CCDs have not been operated at much more than about 200 MHz. The bandwidth (or f_T) of on-chip silicon FETs (N-MOS) is about 500 MHz. Reduced geometry N-MOS or D-MOS devices exhibit $f_T \simeq 1$ GHz. Compare this with a typical Schottky gate GaAs FET for which $f_T = 15$ GHz.

An additional subtle, but highly important, advantage in favor of GaAs for high speed devices is the availability of semi-insulating GaAs which can be used as the substrate in a GaAs CCD. Incorporation of this material into the CCD design reduces power dissipation at high frequency, thus making the device more practical and reducing the design problem of on-chip clock drivers. It reduces the output-node capacitance, thus increasing charge detection sensitivity. Furthermore, since there is no p-n junction between the active charge transport layer and substrate, a "natural" channel-stop is formed by extending the CCD gates beyond the active layer onto the substrate. This feature can be seen in the photograph of the device (Fig. 1).

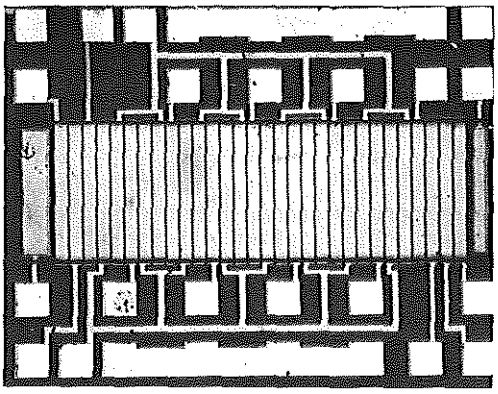

Fig. 1 Ten-cell, 3-phase Schottky gate GaAs CCD

The availability of heterojunction technology in III-V compounds makes possible another related class of devices with significant performance advantages. The ability to choose the material energy gap (by the alloy composition) permits selection of the desired optical response in imaging devices. Forming a heterojunction of this optical absorber and a wide bandgap alloy in which charge transport takes place results in a CCD with exceptionally low dark current. Low dark current results from low intrinsic carrier concentration (n_i) in wide bandgap alloys. Since intrinsic carrier concentration and energy gap are related exponentially, a few tenths of an electron volt difference in energy gap results in orders of magnitude difference in intrinsic carrier concentration. For example, GaAlAs with Eg = 1.7 to 1.9 eV will have 10^6 to 10^7 times smaller intrinsic carrier concentration than silicon (Eg = 1.1 eV). This results in imaging devices or memory devices with room temperature charge integration/storage times of hours rather than fractions of a second.

Still further advantages accrue from the insuator-free (non-MIS) device structure. These devices are a naturally antiblooming structure since charge in excess of a full well is removed as a gate current and does not overflow into adjacent wells. In addition, GaAs Schottky gate CCDs are much more radiation resistant than Si-CCDs, both in terms of photocurrent (because the depletion region and diffusion lengths are small) and permanent degradation, since there is no oxide to charge up.

Finally, a highly desirable feature in a high speed CCD technology is availability of a compatible high speed integrated circuit (IC) technology, so that not only the read-out amplifier, but clock drivers and ancillary electronics can be integrated on chip. Such compatibility does not exist in silicon technology. For example, Si-high speed technology (bipolar-ECL) and CCD technology (N-MOS) are not compatible processes, while GaAs Schottky barrier gate CCD and IC technologies are completely compatible.

2. OPERATING PRINCIPLES

The basic structure of the device is shown in Fig. 1. The spacing between the gates is of the order of one micron. Three gates are required to handle one packet of charge. The energy band diagram for a cross-section of the device under a gate is shown in Fig. 2. The operation of the device can be understood by a study of this figure. Initially (at thermal equilibrium), with no bias applied, the n-layer is partially depleted from both sides due to the built-in junction potentials. When the maximum (negative) "push-clock" voltage is applied to the gate, the minimum potential in the channel is raised so that all the mobile electrons are removed to the adjacent gate. Biasing the output ohmic contact to the layer positively, results in the mobile charges being quickly "pumped" out of the device. As the push-clock bias is reduced to zero, the potential maximum returns to a large positive value which corresponds to an empty well. This well is then ready to store charge created by photogeneration, injection or thermally generated dark current. The potential distribution for a well partially filled by any of these means is also shown. The completely filled well is indistinguishable from the thermal equilibrium condition. The device will remain in a state of non-equilibrium until the thermal gen-