

THEORETICAL LIMITATIONS OF NARROW BANDGAP SEMICONDUCTOR MIS DEVICES USED AS IR IMAGING DETECTORS.

D.ESTEVE\* J.J. SIMONNE\* J. FARRE\* M. SIRIEIX\*\*

\*Laboratoire d'Automatique et d'Analyse des Systèmes du CNRS  
7, avenue du Colonel Roche, 31400 Toulouse, FRANCE.

\*\*Société Anonyme de Télécommunications  
41, rue Cantagrel, 75624 Paris Cédex, FRANCE.

Abstract : The silicon example has been a useful approach to IRCCD and CID processing, but specific limitations due to the nature of narrow bandgap semiconductors have emerged progressively. This paper will consider, via the elementary MIS cell, the effect on key parameters of the system of the following physical phenomena : the tunnel current on the magnitude of stored charge, dark current on storage time, insulator traps on stability and reproducibility, interface states on transfer and noise. The results show that the performance is strongly dependent on process improvement.

INTRODUCTION

Among the different approaches available for the development of infrared-optical imaging and detection systems, monolithic IRCCD and CID processing techniques have received the most particular attention in the past few years. As a result, a tremendous effort of investigation on materials like doped wide bandgap and narrow bandgap semiconductors has been necessary.

Even if the doped silicon could appear as the most attractive choice due to the advantage of the well skilled silicon technology, III-V and II-VI compound devices, in spite of their novelty, became rapidly brought to a high state of development. In that case, the silicon example has been certainly useful to set up the first step of a new procedure ; but specific limitations due to the nature of these narrow bandgap semiconductors have emerged progressively. Some of them have been already studied extensively ; others need additionnal work to be explained. The aim of this paper is to analyse their impact on MIS devices used as IR imaging detectors. In table I are shown the physical limitations facing the performances of narrow bandgap CCD or CID systems :

OPERATION PARAMETERS	PHYSICAL LIMITATIONS
magnitude of stored charge	tunnel current
storage time	thermal generation current (dark current)
stability and reproducibility	insulator traps
transfer	interface states
noise	

TABLE I

TUNNEL CURRENT INFLUENCE

One of the system performances arises from the maximum photonic charge quantity to be stored in the MIS detector. This quantity depends on the incident photon absorption in the semiconductor

and is also limited by the thermal carrier generation which is directly related to the depth of the transient depleted zone and to the minority carrier surface lifetime. In narrow bandgap semiconductors, J. FARRE et al [1] were the first to focus the attention on a third limiting phenomenon, a band to band tunnel current which restricts the dynamic of the structure, while W.W. Anderson [2] proposed a theoretical treatment of interband tunneling based on the WKB approximation to evaluate the corresponding current.

The effect of this current is easily observed in the transient capacitance versus voltage measurement when deeper and deeper depleting voltage steps are applied to the structure. As shown in figure 1, the transient depletion zone width keeps constant beyond the apparition point of the tunnel current.

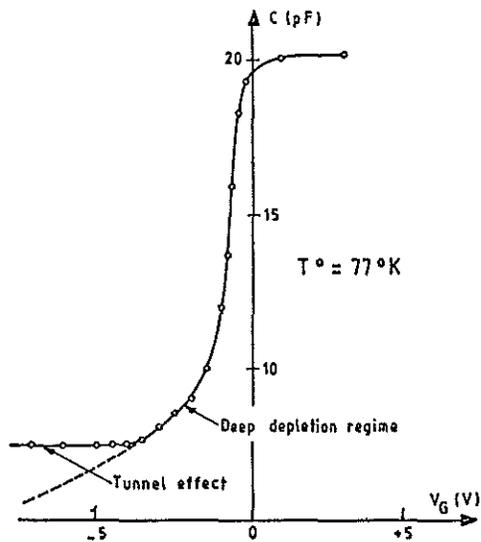


Figure 1 - Pulsed C-V plot of an elementary N-type InSb MIS cell.

One of the main conclusions was to predict the upper performance of the device as a function of the cut off wavelength of the material considered. As shown in figure 2, [1] the shortest the bandgap width is, the lowest is the maximum surface potential which can be reached in a deep depletion mode of operation of the MIS, the best conditions being obtained at low doping densities.

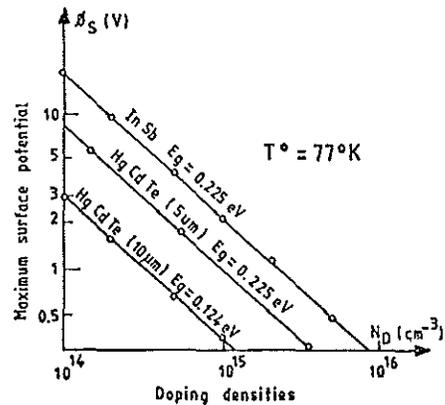


Figure 2

Notice that crystals presenting a carrier concentration below  $10^{14} \text{cm}^{-3}$  are not up to now available on the market. Another direct consequence of the tunnel current will be to select high permittivity dielectrics in order to increase the maximum storage charge [3]. Finally, the effect of the working temperature on the bandgap width should be kept in mind.

## THERMAL GENERATION

The thermal generation current or, even better, the minority carrier lifetime determines the technological requirements, the behaviour of the detector and the characteristics of the control electronic circuits. This can be seen especially through its influence on two parameters in CCD or CID operation: the storage time  $T_S$ , which determines the lowest frequency rate of the electronic circuits, and the transfer inefficiency  $\eta$ , which fixes the quality of the image.

A direct consequence is that the highest possible value of  $\tau$  will increase  $T_S$  and minimize  $\eta$  as it can be shown, in the latter case, from the expression of  $\eta$  which can be deduced from the H-S. Lee and L.G. Heller paper [4] and put under the form.

$$\eta = \frac{4}{\pi^2} \left( \frac{L}{L_D} \right)^2 \frac{1}{U_S} \ln \left[ 1 + \frac{U_S}{1 + \frac{4}{\pi^2} \left( \frac{L}{L_D} \right)^2} \right]$$

where  $L$  is the electrode length,  $L_D = \sqrt{D\tau}$  the diffusion length,  $U_S = \frac{\phi_S}{U_T}$  the reduced surface potential,  $U_T = kT/q$  the thermodynamic potential. A value of  $10^{-8}$ s being readily obtained for  $\tau$ , taking  $D=10$  and assuming  $\phi_S=1V$ , that means a  $3 \mu m$  electrode length should be necessary to reach in these conditions an inefficiency factor  $\eta = 10^{-2}$ ; whereas if  $\tau$  can be dropped down to  $10^{-7}$ s,  $L$  will rise up to  $30 \mu m$  which is a length easily processed in wide applications.

According to this conclusion, a correct interpretation of the measurement of the lifetime  $\tau$  and a good determination of the region of the semiconductor concerned with the measure are capital.

The method of the parallel conductance of the MIS structure can be used to provide the minority carrier lifetime at the surface of the semiconductor; considering the equivalent model of the MIS of figure 3, where  $C_0$ ,  $C_d$  and  $C_{st}$  are respectively the dielectric,

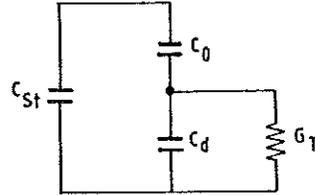


Figure 3 - Equivalent model of MIS Structure (inversion)

depletion and stray capacitance,  $G_T$  being the admittance accounting for the thermal generation,  $\tau$  has been deduced from  $G_T$  which can be expressed under the form [5] [6]

$$G_T = \frac{q n_i L_D}{U_T \tau \sqrt{U_F} - \exp \frac{U_F}{U_T}}$$

where  $q$  is the magnitude of the electronic charge,  $n_i$  the semiconductor intrinsic density,  $L_D$  the intrinsic Debye length and  $U_F = \frac{\phi_F}{U_T}$  the reduced Fermi potential. A current value of  $5 \times 10^{-8}$ s has been obtained for InSb.

The transient capacitance method, also called the "Zerbst method" [7] provides  $\tau$  within the depletion region and consists in applying a step voltage on the gate of the MIS, which deeply depletes the surface of the semiconductor.  $\tau$  is determined from the slope of the linear portion presented by the relaxation curve:  $-\frac{d}{dt} \left( \frac{C_0}{C} \right)^2$  versus  $\frac{C_F}{C} - 1$  [7], where  $C_0$  is the dielectric capacitance,  $C$  and  $C_F$  being respectively the transient and steady-state (inversion) MIS capacitance. This method is especially suitable to "bulk dominated" samples". MIS processed on semiconductor compounds can exhibit often a "surface dominated" characteristic, and make evaluation of  $\tau$  more problematic, as the relaxation curve does not present any linear shape. Measurements on InSb samples have

yielded a mean value of  $10^{-8}s$ .

A fully characterization of thermal generation in the detector implies the determination of another parameter : the surface generation velocity  $s_0$ . In silicon devices, one of the most accurate method proposed in the litterature to measure  $s_0$  used the gate controlled diode [8][9]. However, access to  $s_0$  through this method needs a high quality of the interface SiO<sub>2</sub>/Si under the junction processed under the gate. Furthermore, as imaging CCD arrays do not present any diode at the input like in shift register or signal processing systems, a special device must be therefore processed to perform the measure. Consequently, this technique cannot be straightforward applied to III-V or II-VI compound semiconductors as long as the interface state density is not severely controlled.

The "Zerbst method" [7] is sometimes proposed to get the same evaluation. Actually, this parameter has been artificially introduced to account for a positive intercept of the relaxation curve on the ordonates (Y-axis) of the model which uses an approximated form for the bulk thermal generation current  $I_G$  taking place in the MIS pulsed into deep depletion, namely  $I_G = \frac{qB_i}{\tau} (W - W_F)$  [10], where  $W$  and  $W_F$  are the transient and steady-state depletion width. In fact, the use of an expression accounting for the carrier generation in the whole space charge region rather than in the part included between  $W$  and  $W_F$  needs not any kind of such hypothesis and naturally leads to a model presenting a positive intercept on the Y-axis of the extrapolation of the linear part of the relaxation curve. [11].

The transient capacitance method being inadequate to evaluate  $s_0$ , D.K. Schröder and H.C. Nathanson [12] have proposed the assumption of a variation with time of the surface recombination velocity to overcome the discrepancies between theory and experiment : but it seems difficult to physically justify this hypothesis, especially if we consider the "screen" effect of the inversion layer during the transient.

At this state of the technology, a direct measure of  $s_0$  on IRCCD or CID processed on narrow bandgap material does

not seem available. The method developed for silicon by D.G. Ong and R.F. Pierret [13] using a CCD connected in a gate controlled diode configuration could be later a way to reach the surface recombination velocity.

#### INSULATOR TRAPS EFFECT

Very few papers in the litterature report a time instability which could affect the MIS elements of a IRCCD. However, we have often noticed, especially on structures processed on Indium Antimonide, the presence of a hysteresis on C - V characteristics whose magnitude is a function of the extremes of voltage stress :  $V_A$  (accumulation),  $V_I$  (inversion) and on the voltage sweep rate  $\frac{dV}{dT}$ . Such a problem had previously arised with the first silicon structures, the origin of the phenomenon being essentially a migration of mobile ions in the silicon dioxide. In the present case, ionic drift within the insulator or polarisation of the dielectric layer can generally be ruled out, and a study of the flat band voltage shift  $\Delta V_G(t)$  with parameters  $V_A$ ,  $V_I$ ,  $\frac{dV}{dT}$  and temperature, indicates that this shift should be due to the tunneling of free carriers from the semiconductor into the insulator traps [14][15]. The analysis of such a mechanism emphasizes the influence of the semiconductor bandgap, narrow bandgap semiconductors tending to magnify the hysteresis effect with respect to that of a structure of equal quality processed on silicon [16].

This difference can be seen through the analysis of the time dependent occupancy factor  $f_T$  of the trap located at a distance  $\delta$  from the interface, which is given by [17][18].

$$\frac{df_T}{dt} = \frac{f_T - f_S}{10^{-13} \cdot \exp(\chi^{1/2} \cdot \delta)}$$

where  $\delta$  is expressed in angström,  $f_S$  is the occupancy factor at the semiconductor surface for the corresponding trap energy level,  $\chi$  the electronic affinity of the semiconductor.

The equilibrium value  $\bar{f}_T$  being reached for  $f_T = f_S$ ,  $\bar{f}_T$  will be  $\ll 1$  for wide bandgap semiconductors like silicon

(case 1), whereas  $\bar{F}_T$  will be close to 1 for narrow bandgap semiconductors (case 2), as they present a conduction band strongly degenerated near the surface under the accumulation condition.

Accordingly, assuming that all the traps within the insulator up to a distance  $\bar{X}(t)$  from the interface are in equilibrium, the flat band shift will be

$$\text{in case 1} \\ \Delta V_{G_1} = \frac{N_T}{C_0} \cdot \bar{X}(t) \cdot \int_{E_C}^{\infty} \exp\left[-\frac{E_C - E_F}{RT}\right] dE_C$$

$$\text{and in case 2} \\ \Delta V_{G_2} = \frac{N_T}{C_0} \cdot \bar{X}(t) \cdot \int_{E_C}^{\infty} \frac{1}{1 + \exp\left[\frac{E_C - E_F}{RT}\right]} dE_C$$

where  $E_C$  is the energy of the bottom of the conduction band and  $E_F$  the Fermi level energy.

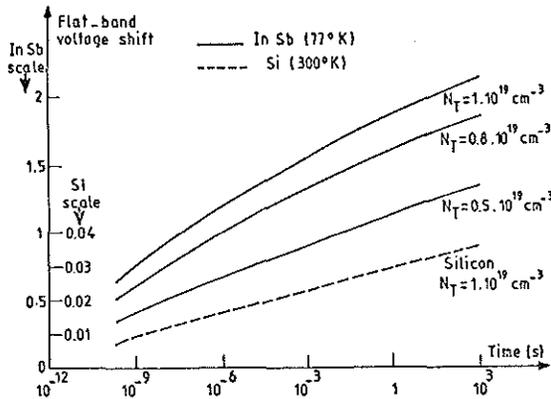


Figure 4

Values of  $\Delta V_G$  for silicon at 300°K appear in figure 4 to be a hundred times smaller than those computed for a narrow bandgap semiconductor like InSb at 77°K. (A spatially uniform energy distribution density of traps  $N_T$  is assumed in the computation).

To overcome this disadvantage in the system behaviour, a "refreshment" operation can be used, consisting in a periodic

cycling between  $V_A$  and  $V_T$ , in order to allow the MIS detector to work always along the same C-V characteristic. Such a method has been used in a 32 elements linear array processed on InSb with SiON CVD layer as dielectric and packaged in a dewar presenting a 15° field of view and a cold filter limiting the spectral bandwidth in the 3,7 to 4,8  $\mu\text{m}$  range. The sensitive area of the elementary cell is 200  $\mu\text{m}$  x 200  $\mu\text{m}$  and an image at a 25 frames/second rate has been produced (figure 5).



Figure 5

Such a technique has been also applied successfully to a 8 x 8 elements matrix array, each cell presenting a sensitive area limited to 35  $\mu\text{m}$  x 70  $\mu\text{m}$  to get a good transfer efficiency.

#### INTERFACES STATES

Interface states are a well known severe limitation, through noise, transfer and stability, of the highest performances of IRCCD and CID. As a matter of fact, noise sources in CCD have been extensively analysed, especially by J.E. CARNES and W.F. KOSONOCKY [19] [20] who have emphasized the major role of fast interface state

trapping over the other components of noise. In CID arrays, H.K.BURKE and G.J. MICHON [21] have underlined the minus importance of charge transfer noise in CCD devices, and discussed the possibility of rejection of KTC noise which could be one of the predominant source in such application, especially when the system behaviour is based on the parallel injection technique [21]. As measurement methods have been proposed by J.C. KIM to evaluate noise sources separately [22], we shall only add to, according to the works of S.CHRISTIENSSON et al on MOS Silicon transistors [23], the possible contribution of a  $1/f$  spectrum noise in narrow bandgap systems caused by the tunneling mechanism between interface states and traps in the dielectric layer, described in the precedent chapter.

Interface states are therefore to be measured with a technique which must not be affected by the presence of the hysteresis, i.e. by the instability of the structure. A high density of states, as shown in fig.6 being generally present in narrow bandgap MIS structure, a pulsed HF-C-V curve has been plotted to avoid the drift due to the tunneling of carriers between semiconductor and insulator. This transient curve is identical to the HF C-V curve [24] as long as the surface potential will not reach  $2\phi_F$ . The lowest value that we have observed on SiON - InSb interface is  $5 \times 10^{11} \text{cm}^{-2} \text{eV}^{-1}$ .

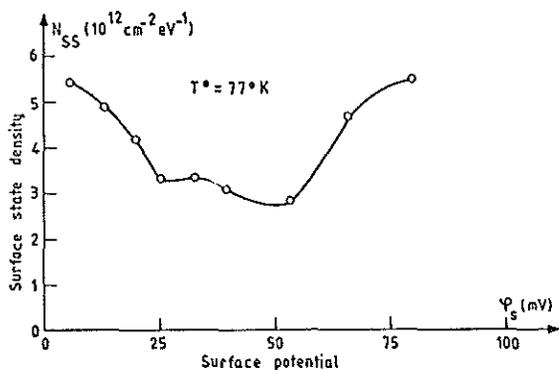


Figure 6 - Interface of an elementary SiON-InSb MIS cell

## CONCLUSION

The analysis of performance limitations due to narrow bandgap semiconductors used as a substrate in IR imaging charge coupled devices and charge injection devices has been presented.

Improvement of the characteristics of these detectors is strongly dependent on the process and on the resulting insulator - semiconductor interface quality. Besides the type of dielectric to be selected, the question is to know which technology among thermal evaporation, chemical vapor deposition, molecular electron beam or even other methods, will allow to get over a new step in the high grade device fabrication.

## BIBLIOGRAPHY

1. J.FARRE, J.BUXO and D.ESTEVE, C.R. hebdomadaire. Seanc. Acad. Sci., Paris, 283 Série B, 103 (1976).
2. W.W.ANDERSON, Infrared Phys. 17, 147 (1977).
3. M.SIRIEIX, M.GARCIA, J.FARRE and J.SIMONNE, Infrared Phys. 18, 3, 233 (1978).
4. H.S. LEE and L.G.HELLER, IEEE Trans. Electron Devices, ED-19, 1270 (1972).
5. D.ESTEVE and J.SIMONNE, Electronics Letters, 5, 9, 194 (1969).
6. D.ESTEVE, Sc.D. Thesis n°339 Université Paul Sabatier, Toulouse (1969).
7. H.ZERBST Angew. Phys. 22, 30 (1966).
8. A.S.GROVE and D.J.FITZGERALD, Solid. St.Electron. 9, 783 (1966).
9. R.F.PIERRET, Solid.St.Electron.17, 1257 (1974).

10. F.P.HEIMAN, IEEE Trans. Electron Devices, ED-14, 781 (1967).
11. J.SIMONNE, Sc.D.Thesis n°552 Université Paul Sabatier, Toulouse (1973).
12. D.K.SCHRÖDER and H.C.NATHANSON, Solid-St.Electron. 13,577 (1970).
13. D.G.ONG and R.F.PIERRET, IEEE Trans.Electron Devices, ED-22, 593 (1975).
14. F.P.HEIMAN and G.WARFIELD, IEEE Trans.Electron Devices, ED-12, 167 (1965).
15. M.H.WHITE and J.R.CRICCHI, IEEE Trans.Electron Devices, ED-19, 1280 (1972).
16. J.BUXO, D.ESTEVE, J.FARRE, G.SARRABAYROUSE and J.SIMONNE, Appl.Phys.Letters, to be published
17. J.LUNDSTROM and C.SVENSON, J.Appl.Phys. 43, 12 (1972)
18. H.C.CARD, Solid-St.Electron. 18, 881 (1975).
19. J.E.CARNES and W.F.KOSONOCKY, Appl.Phys.Letters 20, 261 (1972).
20. J.E.CARNES and W.F.KOSONOCKY, RCA Rev. 33, 327 (1972).
21. H.K.BURKE and G.J.MICHON, IEEE Journ of Solid-St.Circuits, SC 11, 121 (1976).
22. J.C.KIM Final Report Contract N° NO0014-75-C-0124, Naval Electronic Systems Command (1976)
23. S.CHRISTIENSSON, I.LUNDSTROM and C.SVENSSON, Solid.St.Electron 11, 797 (1968).
24. L.M.TERMAN, Solid.St.Electron 5, 285 (1962).