# HgCdTe CHARGE-COUPLED DEVICES*

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ABSTRACT

This paper provides a review of progress on the technology and performance of HgCdTe CCD structures under development for infrared image sensors. First emphasis has been placed on infrared sensitive time delay and integrate (TDI) registers operating at 50 KHz and 77K temperature with long wavelength cutoff in the 3-5 μm range. Charge transfer efficiencies greater than 0.999 have been obtained for 16-stage shift registers. Infrared response with 48% quantum efficiency and detectivity in TDI of $2.8 \times 10^{12}$ cm $Hz^{1/2}$/watt have been obtained in a 16-stage CCD with 4.3 μm long wavelength cutoff. Initial results on 32-stage shift registers are described.

## I. INTRODUCTION

This paper will review progress on charge coupled devices fabricated on HgCdTe alloys at Texas Instruments Incorporated. The first report of CCD action in HgCdTe demonstrated a charge transfer efficiency of 0.996 for an eight-bit four-phase CCD shift register fabricated on $Hg_{.7}Cd_{.3}Te$. [1] These results were obtained for a temperature between 77K and 140K and for clock frequencies below 100 KHz. The first results on 16-stage CCD shift registers with charge transfer efficiency of 0.9995 and near theoretical infrared detectivity in a time-delay-and-integrate mode were reported in mid-1978. [2] These promising results on CCDs were preceded by MIS studies [3,4,5] and knowledge of HgCdTe bulk properties. [6, 7,8] The present paper will detail the results on 16-stage CCD shift register and present initial results on 32-stage CCD shift registers.

The choice of HgCdTe for the fabrication of charge transfer devices has a number of advantages. Unlike the III-V alloys such as $Ga_{1-x}In_xSb$, the $Hg_{1-x}Cd_xTe$ alloy compositions can provide a bandgap approaching zero and a large range of band gap energy for only a small variation in lattice constant.[8] In comparison to the IV-VI alloys such as $Pb_{1-x}Sn_xTe$, the $Hg_{1-x}Cd_xTe$ alloys have a native oxide with excellent insulator properties and a much smaller thermal expansion coefficient [8] facilitating the design and packaging of the CCD.

HgCdTe alloys are presently used to fabricate arrays of photoconductive infrared detectors for use in infrared imaging systems operating in the 3-5 μm and 8-12 μm wavelength bands. The bias current for photoconductive detectors causes an excessive power requirement for the use of thousands of these detectors on a cooled focal plane. Photovoltaic detectors are under development for these wavelength bands and have merit in some applications, but have the disadvantage of requiring individual leads or bonds for each detector unless the detectors are fabricated on the same HgCdTe chip with a HgCdTe CCD multiplexer. For these reasons HgCdTe CCDs for infrared sensing and output multiplexing are desirable choices for an advanced infrared image sensor monolithic chip if charge transfer efficiency greater than 0.999 is obtained. Other HgCdTe devices such as charge-injection-devices and equilibrium MIS photocapacitors [4] are other possible choices with merit, but these approaches do not have the low output capacitance necessary for high voltage-responsivity and sensitivity nor the long integration times for on-chip time-delay-and-integration in an imager using a mechan-

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ical scan; both advantages are inherent in the use of CCDs.

Section II of this paper will discuss the requirements placed on HgCdTe CCDs by the infrared imager application. Foremost among these requirements are (1) the need for a large charge storage capacity to store the charge generated by the ambient infrared background and (2) the need for sufficently small dark currents. Section III will review the capability of HgCdTe MIS devices to meet these requirements; additional details on MIS properties will also be presented in later sections to explain the CCD test results.

The basic elements of the HgCdTe CCD design will be given in Section IV. Although the CCD design is intended for use as either p-channel or n-channel, all results to be presented are for p-channel operation. Sections V-VII will detail the operation of the HgCdTe CCDs as shift registers and as infrared sensors.

By varying the choice of composition, the $Hg_{1-x}Cd_xTe$ alloys with various long wavelength cutoffs can be obtained such as 5 μm at 77K, 5 μm at 192K, and 12 μm at 77K. In this study, alloys have been chosen which have long wavelength cutoffs in the 3-5 μm band at 77K. The potential for operation at longer wavelengths will be discussed in Section VIII.

## II. REQUIREMENTS FOR IR IMAGE SENSORS

The goal of this program is to demonstrate the device technology necessary for the development of area image sensor arrays and first stage signal processing (such as time-delay-and-integration and multiplexing) on an intrinsic-response semiconductor monolith. Excellent reviews of the application of charge transfer devices as image sensors are available.[7,10] Figure 1 shows a generalized layout for a type of area imager utilizing parallel detector columns. In principle, each IR sensitive element of the array could collect the charge generated by each corresponding image pixel and the data bits then be clocked out very rapidly. This concept presents a difficult challenge for the development of a new device technology because of the large number of CCD stages which must operate successfully at a very high data rate if high resolution imagery is to be obtained for real time TV display.

Most IR imagers use a mechanical scanner to provide an image scan in at least one direction across the detector array. The area array of Figure 1 can be used with the mechanical scanner (vertical scan in Figure 1) if the column shift registers are clocked to keep the motion of the column wells in synchronization with the motion of the infrared image down the columns (a version of time-delay-and-integration operation, TDI). As will be shown, CCD shift registers of up to 32-stages operated at 50 KHz clock frequency can provide significant improvement in imager performance when used in a TDI mode in the mechanically scanned system. Thus, the development of HgCdTe CCDs for TDI and output multiplexers are appropriate goals for the initial development of HgCdTe CCDs.

The HgCdTe CCD infrared imager must provide an improvement in imager performance. The overall imager performance is characterized by the minimum resolvable temperature difference MRT at a given spatial frequency. The MRT of a system is determined by the optics, scanner, sensor array, electronic processing, the display, and the observer. In this paper, only those factors determined by the sensor array will be discussed: the noise equivalent differential temperature (NEΔT) and the modulation transfer functions (MTF) of the detector structure, scan and transfer inefficiency.

The NEΔT is determined by the minimum detectable signal which is equal to the wide band noise. An NEΔT of 0.1 C for a 300°K background will be chosen. Typical optics design parameters are f/3.3 for the signal photon radiance $\Delta\phi$ and f/2.0 for the 300°K background photon radiance $\phi_{BG}$. An overall atmospheric and system transmission, $\tau$, of 0.7 will be assumed. A detector quantum efficiency, $\eta$, of 0.5 and detector area, A, of $(25.4\ \mu m)^2$ will be taken as a goal. The equation for the minimum detectable signal-generated carriers in an integrating detector with $\Delta t$ integration is given by

$$\tau\eta\Delta t A\,\Delta\phi\,\sin^2\left(\frac{\theta_{sig}}{2}\right) = \left[\eta\Delta t A\phi_{BG}\,\sin^2\left(\frac{\theta_{BG}}{2}\right)\right]^{\frac{1}{2}} \quad (1)$$

where $\theta_{sig}$ and $\theta_{BG}$ are the full angles associated with the signal and background f/#'s. The same equation would be obtained for voltage outputs.

Rather than develop a formula which ex-

plicitly shows the NE$\Delta$T, a $\Delta\phi$ corresponding to the NE$\Delta$T will be inserted into formula (1) and the $\Delta t$ required for equality will be derived. For a 3-5 μm wavelength bandwidth, $\Delta\phi$ (0.1 C) = $4.72 \times 10^{13}$ photons/cm$^2$/sec and $\phi_{BG} = 1.32 \times 10^{16}$ photons/cm$^2$/sec for a 300 K background. Use of the above parameters requires a total integration time, $\Delta t$, of 435 μsec. In TDI operation, $\Delta t = N\Delta t_D$ can be defined where N is the number of CCD stages and $\Delta t_D$ is the detector dwell time (time for an image element to traverse the detector) which for the CCD is equal to the inverse of the clock frequency. A value of $\Delta t_D$ = 20 μsec will be assumed which is equivalent to 833 detector dwell times in a full 1/60 sec scan. Thus, the 3-5 μm TDI CCD will require 22 stages to obtain 0.1 C NE$\Delta$T. CCD shift registers with 32 stages have been fabricated and tested in the present study.

As suggested by the above analysis, infrared CCD imagers can have overall noise set by the background infrared irradiance. The infrared image sensors experience much larger background irradiance than do visible or near-infrared imagers (which consequently cannot be made radiation background noise limited). The CCD must have a charge storage capacity sufficient to store the carriers generated by this large background irradiance or provide a background subtraction mode of operation. In addition, dynamic range for large signals must be provided. For 60 dB of dynamic range in signal photon irradiance referenced to a 0.1 NE$\Delta$T, the photon irradiance of the focal plane is

$$(2) \quad \phi_{BG} \sin^2\left(\frac{\theta_{BG}}{2}\right) + 10^3 \tau \Delta\phi \sin^2\left(\frac{\theta_{sig}}{2}\right).$$

For the parameters assumed, the 3-5 μm background provides $7.73 \times 10^{14}$ photons/cm$^2$/sec and a total of $1.51 \times 10^{15}$ photons/cm$^2$/sec for equation (2). For a 435 μsec storage time or 22 TDIs, this requires the storage of $5.25 \times 10^{-8}$ coulombs/(cm$^2$-of-pixel-area) or $7.64 \times 10^{-8}$ coulombs/(cm$^2$-of-pixel-area) for 32 TDIs. If the charge storage MIS well area is 50% of the total stage or pixel area, then a maximum charge storage capacity of $1.05 \times 10^{-7}$ coulombs/(cm$^2$-of-well-area) is required for 22 TDIs and $1.53 \times 10^{-7}$ coulombs/cm$^2$ for 32 TDIs.

The CCD clock voltages must be large enough to provide the charge storage capacity with the dynamic range required. However, the dark current for 22-TDI 3-5 μm CCD must be compared to the background generated current (61.8 μa amps/cm$^2$-of-pixel-area or 124 μa/cm$^2$-of-well-area for 50% quantum efficiency) rather than the total maximum photon generated current. A very conservative approach would be to require that the dark current be less than 10% of the background current or 12 μa/cm$^2$-of-well-area.

Finally, the effect of bit geometry and clocking on the modulation transfer function, MTF, must be considered. It is useful to remember the difference between (1) aperturing in space and time which determines the respective MTF values and (2) placing the sample (with these apertures) in space and time which can cause aliasing or sidebands. The spatial aperture of the CCD stage or pixel is given by the stage length (for quantum efficiency constant across the bit). The detector MTF is given by

$$(3) \quad MTF_D = (\pi \ell f_x)^{-1} * \sin(\pi \ell f_x)$$

where $f_x$ is the image spatial frequency on the detector and $\ell$ is the stage length. For a square detector, this $MTF_D$ applies to both the scan and cross scan directions.

There is also an MTF due to the fact that the CCD wells move discontinuously in steps while the infrared image moves continuously along the CCD. This MTF depends on the number of phases, p, which determine the number of times a CCD potential well steps in traversing one CCD stage; this integration time per phase is $\Delta t_D/p$ where $\Delta t_D$ is the detector dwell time. The infrared image moves one stage or detector length $\ell$ in a detector dwell time ($\Delta t_D = \ell/v$) as related by the image velocity, v, on the focal plane. This $MTF_{\Delta t}$ due to time aperaturing during image motion is

$$(4) \quad MTF_{\Delta t} = (\pi v \Delta t_D f_x/p)^{-1} * \sin(\pi v \Delta t_D f_x/p)$$
$$= (\pi \ell f_x/p)^{-1} * \sin(\pi \ell f_x/p)$$

$MTF_{\Delta t}$ affects only the scanned TDI direction and has no effect on the cross scan direction. For spatial frequencies less than the first zero of $MTF_D$ ($f_x = \ell^{-1}$), the effect of $MTF_{\Delta t}$ is not appreciable for four phase clocks (p=4) and is not large for two phase clocks.

The solid line in Figure 2 shows the product $MTF_D * MTF_{\Delta t}$ for a two phase CCD

with a 25.4 μm long detector/stage in the direction of scan. The sample frequency $f_s$ in terms of sample pairs is shown by the vertical arrow at $f_s = \frac{1}{2\ell}$ in Figure 2. This is the case for a CCD with all its stages infrared active. For a CCD with isolation bits which are inactive or whose data is thrown away, $f_s = \frac{1}{4\ell}$. Image spatial frequencies above $f_s$ will be aliased to lower frequencies and appear as false signal. The spatial frequencies passed by the optics MTF will make the total camera MTF (= $MTF_D$ * $MTF_{\Delta t}$ * $MTF_{optics}$) considerably less than the 0.57 shown at $f_s$ in Figure 2. A criterion that the total camera MTF be less than 0.4 at the sampling frequency (sample pairs) has been suggested as a guide.[11]

Finally there is an $MTF_\varepsilon$ associated with charge transfer inefficiency in the CCD.[9,10] This MTF is given in terms of the charge transfer inefficiency, ε, by

$$(5)\quad MTF_\varepsilon = \exp\left[-n\,(1-\cos 2\pi \ell f_x)\right]$$

where n = 1/2 Np with N being the number of stages in the CCD, p being the number of phases, and the factor 1/2 arising from the fact that signal charge is being added to each stage of the TDI rather than into the first stage as in a simple shift register. The various dashed curves in Figure 3 shows the product $MTF_D$ * $MTF_\varepsilon$ * $MTF_{\Delta t}$ (2-phase) as a function of nε. If $n\varepsilon \leq 0.1$ is chosen as a goal for the maximum permissible MTF degradation for a 32-stage two phase TDI CCD, then $\varepsilon \leq 3\times10^{-3}$ and CTE ≥ 0.997 are required. A CTE of 0.999 will therefore be adequate.

MTF in the cross scan direction depends on a number of design parameters which have not yet been fixed. Likewise, cross talk in the serial multiplexer depends on the number of columns to be multiplexed and whether isolation bits are to be used;[12] although these factors have not yet been fixed, a CTE = 0.999 would permit the fabrication of useful modules in which the output of a number of TDI columns could be combined on one signal output line. A complete discussion of topics is not warranted at this stage of development.

## III. CAPABILITIES OF HgCdTe MIS DEVICES

This section will address those requirements set out in Section II and add further details on HgCdTe material and MIS properties.

Dark current is the first major question. The four major dark current contributions are tunneling, depletion layer generation current, minority carrier diffusion current, and surface generation current.

Tunneling at the edge of a constant charge density depletion layer has been derived by W.W. Anderson.[13] In practical cases of interest, the Anderson result can be simplified to give

$$(6)\quad I(Tunnel) \cong \frac{q\varepsilon_o\varepsilon_s E_s^4}{\pi^4 \hbar N E_G^2} \exp\left(\frac{\pi}{-2\sqrt{2}}\frac{\sqrt{3}}{\sqrt{2}}\frac{1}{P}\frac{E_G^2}{E_s}\right)$$

where $E_s$ is the electric field at the edge of the depletion layer, $E_G$ is the bandgap, N is the carrier concentration, $\varepsilon_s$ is the HgCdTe dielectric constant, and P is the interband matrix element in the k·p model and is $8.0\times10^{-8}$ eV-cm for HgCdTe. The approximations of surface potential much larger than bandgap and the exponential coefficient larger than 14 (current slightly above threshold) have been used. All calculations to be reported utilize the more complete formula of Anderson.

The generation of dark current density in the depletion layer in a strongly depleted MIS well is given by

$$(7)\quad I(w) = \frac{q\, n_i\, w}{2\tau_g}$$

where $n_i$ is the intrinsic carrier concentration, w is the depletion layer width, and $\tau_g$ is an effective lifetime.

The minority carrier diffusion current density for thick samples is given by

$$(8)\quad I(D) = \frac{q\, n_i^2}{N}\sqrt{\frac{kT}{q}\,\frac{\mu}{\tau}}$$

where N is the majority carrier concentration, μ is the mobility of minority carriers, and τ is the minority carrier lifetime in the neutral and quasi-neutral regions underneath the depletion layer. Because of the temperature dependence of the $n_i^2$ term, I(D) will be larger than I(w) at 190K for 5 μm HgCdTe, but I(w) will be larger than I(D) at 77K.

The surface generation current density is given by

(9) $$I(s) = \frac{q\, n_i\, s}{2}$$

where s is the effective surface recombination velocity in cm/sec.

In addition to the above terms, avalanching current multiplication will occur at high electric fields for moderately high doping concentrations.

Figure 3 shows the amount of charge collected in an MIS well as a function of the duration of the integration based on the depletion layer approximation. These predictions are for 5 μm HgCdTe at 77K and include the dominant terms of tunnel and depletion currents. The dashed line at the left shows charge collected from the 120/μa $cm^2$ infrared background requirement of Section II. The two cases in the middle of the figure are for two different carrier concentrations with MIS gate voltage adjusted to make the initial tunnel current 10% of the infrared background generated current. As can be seen, the rate at which charge is collected due to tunneling decreases with time as the electric field at the edge of the depletion layer decreases with buildup of inversion charge. At times much longer than the 400-600μsec system integration time required, the depletion layer current becomes dominant and determines storage time in the absence of infrared.

Although the sample with $2x10^{15}/cm^3$ carrier concentration has a longer dark storage time as shown by the vertical arrows, the sample with $4x10^{14}/cm^3$ carrier concentration is preferred because larger charge storage capacity. The dotted curve at the right hand side shows that a reduction in gate voltage for the $4x10^{14}/cm^3$ sample still leads to a storage time less than that for the $2x10^{15}/cm^3$ sample. At 190K, all current components would be important at the initiation of the integration.

The requirement that the dark current be equal to 10% of the infrared background generated current can be used to predict the variation of maximum well capacity with ZnS insulator thickness and carrier concentration. Figure 4 shows the predictions for maximum well capacity based on tunnel current alone at 77K. A choice of 50% of the infrared current would not make a large change because of the exponential dependence of tunnel current on $E_s$. The vertical arrows in Figure 4 show typical ZnS thicknesses for the first and second level gates. The horizontal line shows the charge capacity requirement (per-$cm^2$-of-well-area) for 32 TDIs. A carrier concentration of $1x10^{15}/cm^3$ is sufficient to meet the requirements. Figure 5 shows the gate voltage required to attain the charge capacities of Figure 4.

The theoretical prediction of charge transfer inefficiency depends on a number of imperfectly known parameters for HgCdTe MIS devices. The 77K bulk mobilities for 5 μm HgCdTe are known from Hall measurements to be 400 and 40,000 $cm^2$/volt-sec for holes and electrons respectively, but the surface mobilities can only be estimated to be one-half these values. Fast surface state densities have been studied by various capacitance-voltage and conductance techniques. Typically, the conductance is too small for successful measurement on 5 μm HgCdTe devices at 77K. Likewise it is too difficult to reach quasi-static conditions [14] at this temperature. Measurements of dC/dV give no indication of any significant localized density of fast surface states, and the Amelio technique [15] implies a fast surface density of $2x10^{11}/cm^2$-volt near flat band. However a comparison of high frequency and low frequency C-V curves made at temperatures above 77°K indicate that this density of fast surface states may be too high. Conductance measurements of depleted and weakly inverted surfaces at these elevated temperatures are also not consistent with the value of $2x10^{11}$ $cm^{-2}$ $V^{-1}$. Indications are that the discrepancy is due to statistical fluctuations in the local density of fixed charge in the oxide.

The primary source of charge transfer loss and inefficiency at low frequencies in CCDs operating with a fat-zero charge is trapping in fast interface states at the edge of the CCD well. The near-horizontal lines in Figure 6 show the predictions of theory [16] for edge-induced fractional loss per transfer for p-channel HgCdTe. In addition to the parameters listed on the figure, the signal charge was assumed to be 0.8 full well and the surface state capture cross section for holes was assumed to be $10^{-17}$ $cm^2$. The calculation is for clock voltage of 5 volts riding on a substrate bias of 0.5 volts above threshold.

At higher frequencies with optimum design, the transit time across a CCD gate

is determined by fringing field drift. The near-vertical lines in Figure 6 show the predictions for charge transfer loss based on this theory. [17]

The best charge transfer efficiency of 0.9995 to be reported on a 16-stage 51 μm-wide CCD with 10.2 μm long electrodes can be fit with a fast surface state density of 6.3 x $10^{10}$/$cm^2$-volt. This value is below the value measured by dC/dV techniques and supports the speculation that the dC/dV measure is too large because of statistical fluctuations in fixed charge in the oxide.

## IV. HgCdTe CCD DESIGN, FABRICATION AND OPERATION

The HgCdTe used in this study was grown by the solid state recrystallization technique which normally gives ingots consisting of a few large crystallites with compositional homogeniety of 0.3 mole 0/0. The samples were annealed in a mercury-rich atmosphere to reduce the carrier concentration. $Hg_{1-x}Cd_xTe$ samples with $0.295 < x < 0.315$ were selected for this study. Hall measurements indicated an n-type carrier concentration 1-2x$10^{15}$/$cm^3$ and an electron mobility of 4x$10^4$ $cm^2$/v-sec at 77K. The carrier concentration measured by MIS analysis using test capacitors on the MIS test bars also indicated 1-2x$10^{15}$/$cm^3$.

All CCD designs utilized a four phase structure with tunnel (or avalanche) breakdown at an MIS-gate input and an MIS gate output. Figure 7 shows a photograph of two 16-stage HgCdTe CCD shift registers with transparent electrodes. The channel widths of the two CCDs are 127 μm and 50.8 μm as defined by the aluminum field plate for these two designs. The infrared active channel widths are 119 μm and 43.2 μm as defined for the two CCDs by the intersection of the thin nickel and thick aluminum metal layers on each gate. All phase wells are 10.2 μm long. The floating gate well is 20.4 μm long. The photomask design includes optional input and output diodes.

Figure 8 shows cross sectional views across and along the length of the CCD channel. In all cases, the first level insulator is a 700Å thick native oxide on the HgCdTe. Various designs with different thicknesses of evaporated ZnS have been used. The ZnS under the aluminum field plate is typically 1100Å thick. The ZnS under the first level gates is typically 2600Å-2700Å thick. The total ZnS thickness under the second level gates has been varied from 5300Å to 8900Å.

Figure 9 shows the capacitance voltage characteristics for electrodes on a 16-stage CCD shift register which used all aluminum opaque electrodes. All insulators included 700Å of native oxide (dielectric constant = 17) plus the following ZnS (dielectric constant = 7.5) [3] thicknesses: 1100Å to the field plate, 2600Å to the first level gates ($\phi_2$,$\phi_4$, etc.) and 6800Å to the second level gates ($\phi_1$, $\phi_3$, etc.) The flatband voltages for these three levels are approximately -2.7V, -6.0V, and -13.0 volts respectively. These values are consistent with 7.3x$10^{11}$/$cm^2$ fixed charge and -0.7 eV work function difference. Other devices have had fixed charge densities as low as 4x$10^{11}$/$cm^2$. The capacitance voltage curves show a hysteresis of about 0.1 volts characteristic of charge trapping. Beyond flatband voltage these devices show the characteristics of deep depletion with storage. Other devices with good CTE action showed high frequency characteristics at 10 KHz (but with no storage).

Figure 10 shows a generalized schematic of a 16-stage CCD with the floating gate output circuitry. The gates denoted by IG-1 and OG-2 were kept dc accumulated. The four phases were driven with four phase clocks. The clock voltages could be adjusted so that the storage capacity of all wells were similar (true four-phase operation) or so that the second level wells had little storage capacity (a quasi-two phase mode.) In the shift register measurements, an input breakdown pulse about 0.2 μsec in duration was applied to IG-2. It is not known whether the input charge is due to tunnel current at very high bias or to avalanche breakdown. Electrode OG-1 was used as either a dc or a pulsed output gate. Figure 11 shows a clock sequence used for the shift registers. Most measurements were performed with 50 KHz clocks so that the on-time (negative-going pulses) is 10 μsec for all phase clocks. Although a 9 μsec wide injection pulse is shown, an injection pulse width of 2 μsec was more typical. As can be seen from Figure 11, the input signal occurs when both phase-one and phase-two are on. With infrared input, the CCD could be operated with the same waveforms with or without the shift register signal input. "Freeze clock" measurements were also performed in

which the clocks could be stopped for an adjustable duration with any one of the phase clocks on and the other phases off. In this format, dark current or infrared signal is integrated during the freeze duration. At the end of the freeze duration, the clocks begin operation in proper order and the integrated charge per stage is clocked out to the floating gate.

The floating gate was preset empty well before dumping the signal charge into the well from the phase-four well. Signal was usually detected by clamping before the injection pulse and sampling after the injection pulse. Signal detection was also performed on occasion using slosh of charge into or out of the floating gate well. The experimental node capacitance on the measurement node varied from 5 pF to 40 pF depending on the output circuit, injection capacitor value, and whether the first stage apmlifier was inside or outside of the sensor.

The signal voltage, $\Delta V_S$, can be related to the charge transferred or injected, $\Delta Q_S$, by an approximate relationship with stray capacitance $C_p$, insulator capacitance $C_{INS}$, and the average $\bar{C}_d$ of the depletion layer capacitance before and after injection.

$$(10)\quad \Delta V_S \cong \frac{\Delta Q_S}{\bar{C}_d + C_{INS}C_p/(C_{INS}+C_p)} \cdot \frac{C'_{INS}}{C_{INS}+C_p}$$

Since the output is ac coupled, the $\Delta Q_S$ corresponds to the signal charge while dark current or fat zero is not measurable(but limits the size of $\Delta Q_S$). Dark current could be measured with the freeze clocks. Approximate values of $C_{INS}$ and $\bar{C}_d$ for the floating gate of the 127 μm wide CCD are 0.57 pF and 0.44 pF respectively which are both much smaller than the strong capacitance. Thus, the value of $\Delta V_S$ is given by

$$(11)\quad \Delta V_S \simeq \frac{\Delta Q_S}{C_p} \cdot \frac{C_{INS}}{\bar{C}_d + C_{INS}} \simeq \frac{\Delta Q_S}{1.8\ C_p}$$

The charge $\Delta Q_S$ delivered to the floating gate is limited by the charge capacity of the phase-two or phase-four electrodes which are half the area of the floating gate. For a maximum charge density of $1 \times 10^{-7}$ coulombs/$cm^2$ (Figure 3) and the 127 μm wide channel, the maximum voltage signal is 72 mV for the measured 20 pF stray capacitance.

A new CCD test bar is being tested with a number of new structures. Results will be reported on a 32-stage CCD with a 35.6 μm wide storage channel, 25.4 μm wide infrared active channel, and 25.4 μm bit length. For the measured 5 pF stray capacitance, the maximum output voltage with this device is 50 mV for $1 \times 10^{-7}$ coulombs/$cm^2$ in the phase-two and phase-four wells.

## V. SHIFT REGISTER EVALUATION

Study of the CCD structures has emphasized CTE determination by evalutaion of shift registers at 77K and with 50 KHz four-phase clocks using a tunnel (or avalanche) input. The first results obtained were 0.996 for an 8-stage shift register.[1] Many 16-stage shift registers have been evaluated with CTE results in this range. In many cases, these values were limited by the operation of the injection floating gate rather than the charge transfer efficiency of the shift register. The basic problem is injection-feedback: part of the charge injected into the substrate can diffuse back to the last stages of the shift register and be delivered a second time to the floating gate. Figure 12 shows the floating gate output when the charge is clocked out to an electrode more remote from the last stage of the shift register rather than being injected at the floating gate. A CTE of 0.9995 was obtained at 77K for 50 KHz clocks. The magnitude of the signal output is in agreement with theory for the measured 40 pF stray capacitance and the 4-volt voltages (beyond theshold) used on the phase-four and phase-two clocks. Similar CTE improvement could be obtained by providing a drift field in the substrate.

Figure 13 shows the result of Zerbst analysis[18,19] of a test capacitor (area= $6.45 \times 10^{-4}$ $cm^2$) on the same CCD test bar used in the CTE test shown in Figure 12. The pulsed capacitance decay in this MIS lasted for over 80 seconds (this long storage time is consistent with predictions for 4.4 μm HgCdTe with the doping concentration observed - $1.5 \times 10^{15}/cm^3$). The initial decay (large $C_p/C$ -1) shows a variable slope probably associated with a varying surface generation current.[19] According to Zerbst analysis, the linear region in this plot is dominated by depletion layer generation current with a constant surface generation rate. A least squares fit to the linear portion of the data yielded an effective generation lifetime of 6.8 μsec and a surface recombination of 1.30 cm/sec with a 0.993 correlation coefficient for the fit. Minority carrier lifetimes for the n-type bulk of 10-20 μsec have been measured for 5 μm

HgCdTe. A lifetime of 10 μsec yields a minority carrier diffusion length of 45 μm compared to the 30.5 μm distance from the floating gate well to the phase-two well which is on during injection.

Other CCD test bars had Zerbst generation lifetimes as short as 1.8 μsec. Figure 14 shows the results of CTE testing on one such 16-stage CCD which had CTE > 0.999 when operated in the standard floating gate detection mode using injection. Fat zero was provided by background radiation from an 11° field of view. The magnitude of the signal output is consistent with theory for the measured 12 pF parasitic capacitance for the clock voltages which were 5 volts beyond threshold.

In all the tests on HgCdTe CCD shift registers, some fat zero was supplied by dark current generationin the phase wells, infrared generation of carriers, or by fat zero intentionally supplied by a second 0.2 μsec-wide input pulse which occurred every clock cycle. n those cases where dark current contributions were reduced, a fat zero of less than 10% full well was sufficient to eliminate most leading edge fixed loss. The amount of fat zero (of any origin) required for best CTE varied from device to device.

Initial results from the tests on the 32-stage shift register described in Section IV are shown in Figure 15. A CTE of 0.997 was measured at 77K for 50 KHz clocks. A fat zero input pulse was required to obtain this result, and this input reduced the voltage output from 400 mV to 200 mV (gain X100). Due to excess dark current from 4-5 stages (seen in freeze clock measurments), the phase-two and phase-four gates were biased to only 2 volts beyond threshold. The small value of output is due to the excess dark current and fat zero. These results are encouraging in that these results are for the first 32-stage CCD tested in our laboratories.

## VI. DARK CURRENT MEASUREMENTS

The standard shift register measurements described in the previous section provided only indirect knowledge about the magnitude of dark current and no knowledge on the origin of dark current from the various stages of the shift register. The freeze clock technique described in Section IV provides this knowledge. Defective operation of CCD shift registers could be explained by the freeze clock results which could show blockage due to inoperative phases or dark current spikes due to bad stages in the center of the CCD.

Figure 16a and 16b show freeze clock measurements on a transparent gate 16-stage CCD with no infared radiation incident on the device (a cold cap on the device flat pack). During the 1 msec freeze only the phase-four wells were on and collecting dark current. The photographs show a readout of the dark current from the 16 stages of the CCD followed by a normal shift register output due to signal introduced at the far end of the shift register after the clocks opertion begins again after the freeze. Figure 16b shows a significant increase in dark current when the field plate is biased to be more heavily accumulated. These results suggest that this dark current is associated with the edge of the channel. One possible explanation under study for this excess current is tunnel or avalanche current at the field plate edge (enhancement of the electric field at the MIS well edge).

## VII. INFRARED MEASUREMENTS

The major aims of the infrared portion of this study have been to (1) establish the infrared quantum efficiency for the CCD stages and the uniformity of this parameter and (2) demonstrate responsivity and detectivity gain due to the integration of signal and background irradiance as the potential wells transverse the stages of the CCD.

Quantum efficiency for infrared detection was studied using (1) the CCD output and (2) the conductance of MIS test capacitors on the test bar. The signal voltage at the output of the CCD in continuous clock operation is

$$(12) \quad V_S \cong \frac{q}{1.8\ C_p}\ \eta\phi_S A_D N \Delta t_D$$

where $C_p$ is the stray capacitance, $\eta$ the quantum efficiency, $\phi_S$ the signal photons/$cm^2$/sec, $A_D$ the detector area (the infrared active portion of each stage), N the number of stages, and $\Delta t_D$ is the inverse of the clock frequency.

In the freeze clock mode of operation, the clocking of the potential wells is

stopped for a freeze period $\Delta t_{FZ}$ with only one phase on and then clocking is resumed and all bits clocked out. This is a differential measurement in that all bits clocked out have experienced the infrared irradiance for at least $N\Delta t_D$ seconds, but the frozen data bits have in addition, experienced $\Delta t_{FZ}$ seconds of irradiance. Thus, the differential signal voltage in the freeze clock measurement is

$$(13) \quad \Delta V_S \cong \frac{q}{1.8\ C_p}\ \eta\phi_S A_D \Delta t_{FZ}$$

Figure 17(a) shows freeze-clock-mode output for CCD 13AT8NR at 77K using 50 KHz clocks, phase-two and phase-four clock voltages -5 volts beyond threshold, a stray capacitance of 20 pF, and a gain of 100. The infrared irradiation is due to a 20° field of view for ambient 300K radiation. The first output (negative) to occur is that due to a 1.8 msec freeze with the phase-four wells on with consequent integration of the carriers generated by ambient radiation. Shortly after clocking is resumed after freeze, a tunnel (avalanche) signal is fed in from the input end of the CCD and the standard CCD shift register output (negative) is shown for four bits (not saturated).

Figure 17(b) shows the same type of data for a 4.0 msec freeze and with the shift register input voltage increased. Now both the freeze clock and the shift register outputs are saturated (full well). Comparison of Figures 17(a) and 17(b) show that the slight decrease in freeze clock output seen for freeze clock output bits 9, 10, and 11 disappear upon saturation. This phenomenon is due to the shadow of a gold bonding wire which passes above the CCD. The initial signal bits (1, 2, and 3) have larger outputs in both Figure 17(a) and 17(b) and are not due to a variation in quantum efficiency, but arise from preamp recovery after a large false signal during freeze. The variation in unsaturated output signal is considerably less than 10% for all uniformly irradiated true data bits indicating very little variation in quantum efficiency among the CCD stages. The average quantum efficiency derived from equation-13 is 46%. Similar measurements were made with smaller field-of-view and a 500K blockbody source and also with a 0°FOV using a GaAs near-infrared diode emitter.

The deviation of quantum efficiency from the CCD measurements requires the accurate knowledge of the stray capacitance at the measurement node. In a second measurement, a quantum efficiency of 48% was derived from analysis of the low frequency conductance of a large test capacitor on the same bar with 13AT8NR in a 20° field of view.

Spectral response was measured using the photoresponse of the test capacitor biased to near the minimum in the low frequency capacitance-voltage characteristic. Most test bars had long wavelength cutoffs (one-half-response wavelength) in the range 4.3 - 4.7 μm. One test bar (9A20) having a 16-stage CCD with 0.997 CTE had a long wavelength cutoff of 5.0 μm.

Signal integration as the potential wells are clocked along the 16-stages of the CCD is demonstrated by Figure 18 which shows the response of CCD 12AT3 (50 KHz clocks) to GaAs diode emitter pulse of 520 μsec duration. During the first 320 μsec of the non-infrared pulse, the CCD output increases in steps as the data bits experience one through sixteen clock periods of infrared illumination. During the next 200 μsec, all output bits experience sixteen clock periods of illumination. At the end of the illumination, there is a period of 320 μsec in which bits illuminated for sixteen to one periods of illumination are clocked out. The uniformity in the magnitude of the voltage steps between data bits is evidence for excellent uniformity in quantum efficiency.

Signal-to-noise in an infrared detector is characterized by its detectivity or $D^*$ for blackbody irradiance (or monochromatic irradiance) in the presence of ambient irradiance. The experimental blackbody detectivity is derived by

$$(14) \quad D^*_{BB} = \frac{1}{H_S}\ \frac{V_S}{V_N}\left(\frac{B}{A_D}\right)^{1/2}$$

where $H_S$ is the total signal irradiance (watts/cm$^2$) on the detector, $V_S$ is the signal output voltage, $V_N$ is the noise output voltage in frequency bandwidth B, and $A_D$ is the detector/stage area. The theoretical conversion from $D^*_{BB}$ is wavelength and temperature dependent and is x13 for a 4.3 μm cutoff and a 500K blackbody source.

Detectivity at 77K was measured for

several CCDs using a chopped 500 K blackbody source. The 500K source was chopped at a low frequency (100 Hz) to obtain good waveform reproduction using 50 KHz clocks for the CCD (see Figure 18). In these measurements, the stray capacitance was 15 pF and the 500K signal flux was $1.2\times10^{-6}$ watts/cm$^2$ on the CCD. For a 20° field of view, the derived $D^*_{\lambda p}$ was $2.8\times10^{12}$ cm Hz$^{1/2}$/watt for CCD 13AT8NR which had a 4.3 μm long wavelength cutoff.

A theoretical maximum value for $D^*_{\lambda p}$ can be obtained for infrared background limited performance by using equation (12) for signal and equation (15) for the narrow band uncorrelated noise $\langle V_f^2 \rangle^{1/2}$ for B = 1 from a time-delay-and-integrate detector integrating for $N\Delta t_D$ seconds and read out every $\Delta t_D$ seconds.

$$(15) \quad \langle V_f^2 \rangle^{1/2} = \frac{q}{1.8C_p} \Delta t_D \sqrt{2\eta\phi_{BG}A_D N}$$

where $\phi_{BG}$ is the ambient irradiance on the detec or due to the field-of-view. The theoretical value for $D^*_{\lambda p}$ is

$$(16) \quad D^*_{\lambda p} = \frac{\lambda}{hc}\left(\frac{N\eta}{2\phi_{BG}}\right)^{1/2}$$

For 4.3 μm long wavelength cutoff, a 300°K ambient seen through a 20° field-of-view and a 46% quantum efficiency the theoretical value of $D^*_{\lambda p}$ is $4.0\times10^{12}$ cm Hz$^{1/2}$/watt.

The experimental value of $D^*_{\lambda p}$ is 70% of the theoretical value. This discrepancy is due to the aliased white noise of the first stage amplifier [20] which consists of a cooled JFET operated as a source follower. The degree of aliasing was attenuated by use of a 1 μsec RC filter between the low noise post amplifier (gain X12) and the 50 KHz sampling circuit. The total amplifier noise referred to the input node was 30 nV/(Hz)$^{1/2}$ under the above test conditions. The total detector plus amplifier noise in the D* tests was 50 nV/(Hz)$^{1/2}$ referred to the input. Therefore, within experimental error, the amplifier noise which is dominated by the aliased buffer noise limits the present results on D*. The detector noise results were measured for a background which gave only 10% full well charge. Experimental detectivities closer to theory should result from the use of larger field of views and/or decreased white noise of the buffer amplifier.

## VIII. POTENTIAL FOR 8-12 μm APPLICATIONS

As previously discussed, $Hg_{1-x}Cd_xTe$ alloys can be used to fabricate infrared detectors for 8-12 μm window. Both photoconductive and photovoltaic detectors have been demonstrated. The application of CCD (or CID) technology to HgCdTe with 12μ m cutoff to imagers using large background field of view is a challenging task. Application of HgCdTe with 10 μm cutoff is more promising. The problem is two-fold: (1) the smaller bandgap of this material causes tunneling to occur at lower electric fields and (2) the 8-12 μm wavelength band contains considerably more radiation to be stored than does the 3-5 μm band. On the other hand, a much shorter integration time is needed to obtain 0.1° NEΔT.

Analyses for the same system parameters as used in Section II yield a requirement for 84 μsec integration time for 8-10 μm HgCdTe thus requiring only 4 TDI stages of 20 μsec each for 0.1°C NEΔT. The 60 dB dynamic range requirement plus the larger background requirement for the 8-10 μm band will require the storage of $1.6\times10^{-7}$ Coulombs/cm$^2$-of-pixel-area for 4 TDI's and require a dark current density of less than 130 μa/cm$^2$-of-pixel-area. Actually, an 8-10 μm system would need to be cold shielded more efficiently than the above example potentially cancelling the bit-area/well-area ratio requirement of Section II. Furthermore, the above calaculation of NEΔT was based on identical atmospheric transmission for the 3-5 μm and 8-10 μm bands which improperly penalizes the 8-10 μm band. A precise comparison would depend on the atmospheric model utilized and thus is beyond the scope of this paper.

The requirement that the total tunnel current be less than 10% of the background current is shown for several wavelength bands in Figure 19. A ZnS insulator thickness of 1000Å has been assumed as a projection of present technology. It can be seen that 8-10 μm application will require HgCdTe material with carrier concentration less than $2\times10^{14}$/cm$^3$. Material with this carrier concentration is feasible.

Unlike the case shown for 5 μm material at 77K in Figure 5, both minority carrier diffusion and depletion layer currents can make significant contributions to the total dark current of a 10 μm MIS device

biased near the tunnel limit for $2x10^{14}/cm^3$ material (about 0.95 volts/μm electric field.) Both mechanisms can give dark current contributions in the range of 30-60 μamps/$cm^2$. Both these contributions for 10 μm HgCdTe could be eliminated by reducing the focal plane temperature to a temperature similar to that proposed for 3-5 μm-response extrinsic silicon detectors.

The application of MIS technology to 8-10 μm applications appears feasible provided top quality material with carrier concentration in the $2x10^{14}/cm^3$ range and depletion generation lifetime greater than 10 μsec is utilized. The importance of this application suggests that these challenges will be overcome.

## IX. CONCLUSIONS

Excellent progress has been obtained on 3-5 μm wavelength HgCdTe CCDs operating at 77K. Charge transfer efficiency adequate for most anticipated applications has been demonstrated. Infrared detection with time-delay-and-integration enhancement of responsivity and detectivity has been demonstrated. Both 16-stage and 32-stage CCD shift registers have been tested at the 50 KHz clock frequencies required for time-delay-and-integration in an infrared imager with a 1/60 sec mechanical scan. Future studies will include multiplexer evaluation at higher frequencies and time-delay-and-integrate demonstration with mechanically scanned imagers.

Sufficient charge storage for the 8-10 μm wavelength band is within the range of possible design parameters and will necessitate the use of the highest quality material and innovative device design.

The device technology utilized for Hg CdTe CCDs has potential for application to other charge transfer device designs such as CIDs. Implementation of a large number (20-30) TDI stages is much more straightforward using CCD designs. The implementation of a few TDI stages for applications with storage time limitations could be performed with HgCdTe CIDs combined with silicon signal processing CCDs. Staring arrays could be implemented with either HgCdTe CCDs or CIDs depending on the application requirements.

The authors wish to thank Herb Kraus & Maurice Brau for HgCdTe material and Jerry Schaefer for discussions on systems analysis. Jeff Beck has assisted on edge field studies and Zerbst analysis. Extravagant praise is due to all the device fabrication specialists and electronic specialists responsible for the success of this program. The authors also wish to thank Drs. W. Dean Baker, Richard A. Reynolds, and Ron A. Belt for support of this program.

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FIGURES

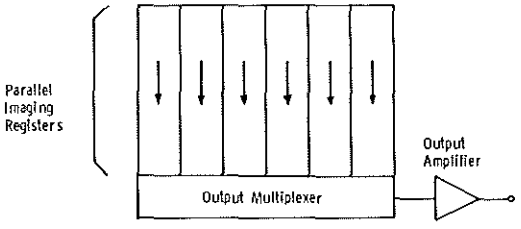



Figure 1. A generalized type of area CCD imager. When used as a TDI array, the infrared image is scanned from top to bottom of the figure.

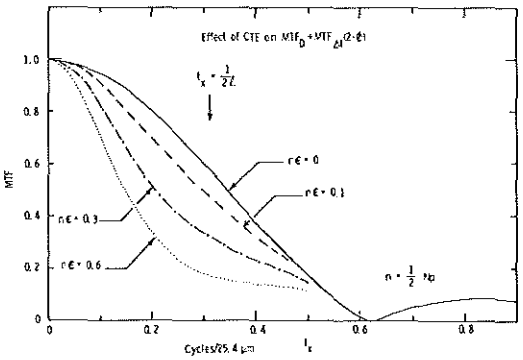



Figure 2. Modulation transfer function in the direction of transfer (shift register with 25.4 μm stage length.)

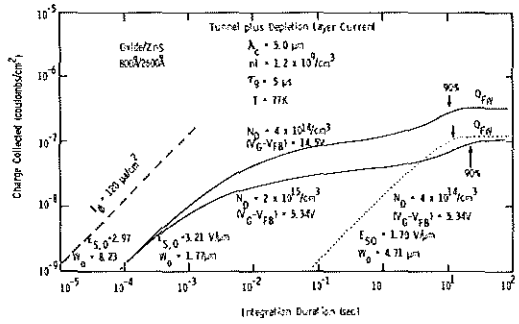



Figure 3. Charge collected versus time in an MIS showing that depletion layer current dominates storage time in 5 μm HgCdTe at 77K. Tunnel current is the dominant dark current for the <1 msec integration times anticipated.

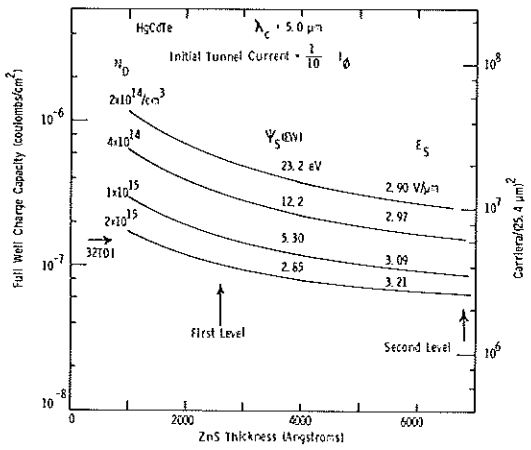



Figure 4. Predicted full well charge capacity as a function of ZnS insulator thickness with carrier concentration as a parameter. HgCdTe long-wavelength cutoff is 5 μm.

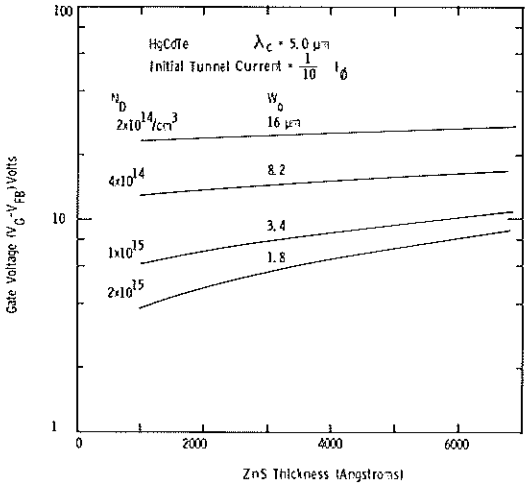



Figure 5. Predicted gate voltage to obtain the full well capacities of Figure 4.

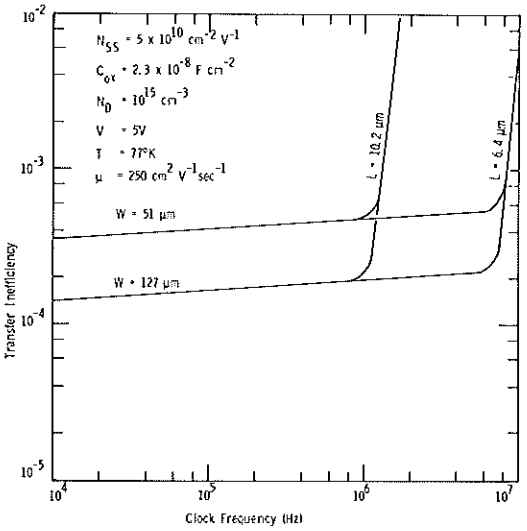



Figure 6. Theoretical CTE vs Frequency for p-channel 0.25 eV HgCdTe

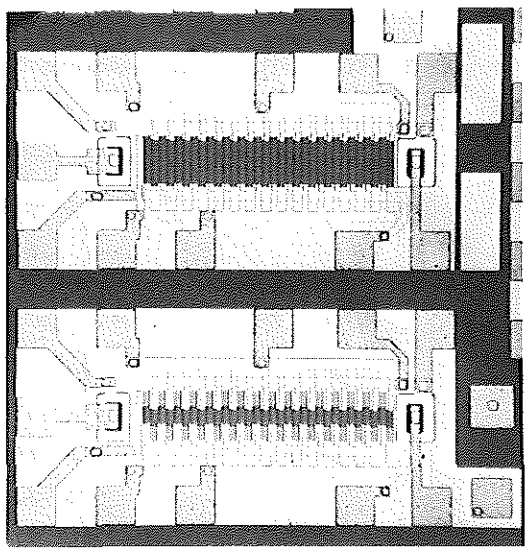


Figure 7. Two 16-stage HgCdTe CCD shift registers with transparent electrodes.

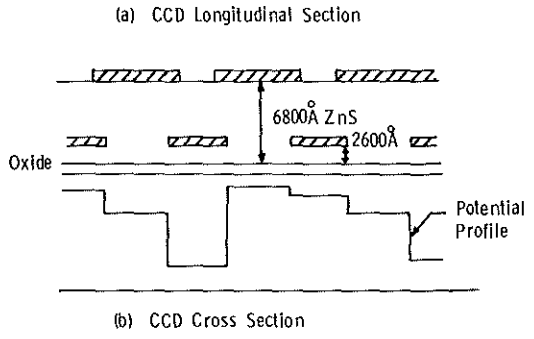



Figure 8. CCD shift register geometry (one type)

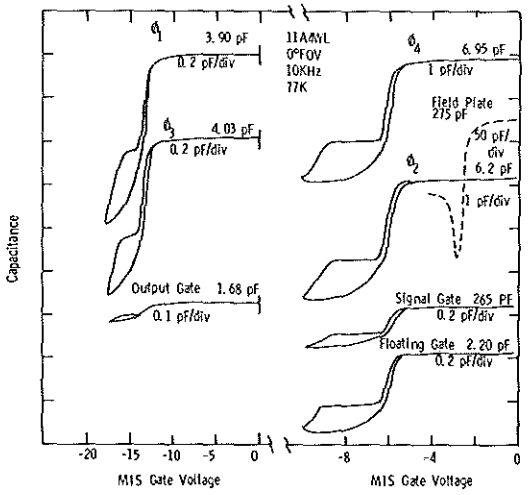



Figure 9. Capacitance-voltage characteristics for 16-stage CCD 11A4WL

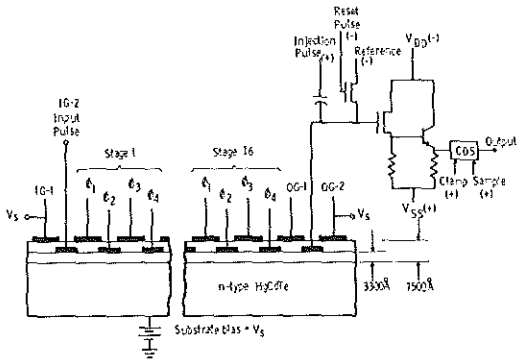



Figure 10. Schmatic of CCD shift register and output circuit

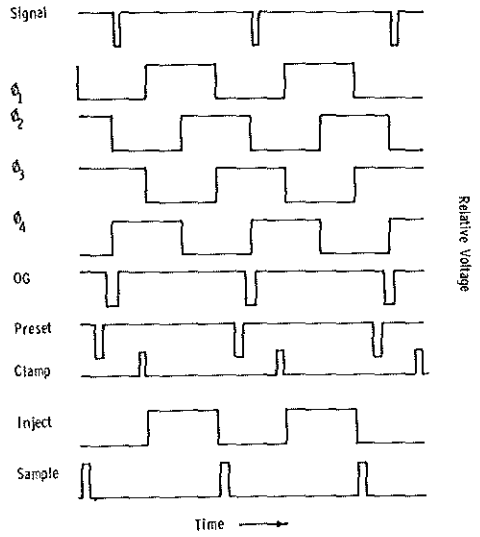



Figure 11. Clock sequence for 16-stage shift register

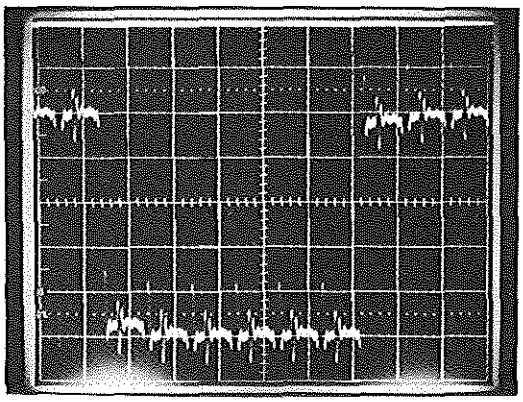


Figure 12. Output for 16-stage CCD 11A4WL showing CTE = 0.9995. Vertical 20mV/div. Horizontal 20 μs/div. Gain X70. Stray capacitance = 40pF

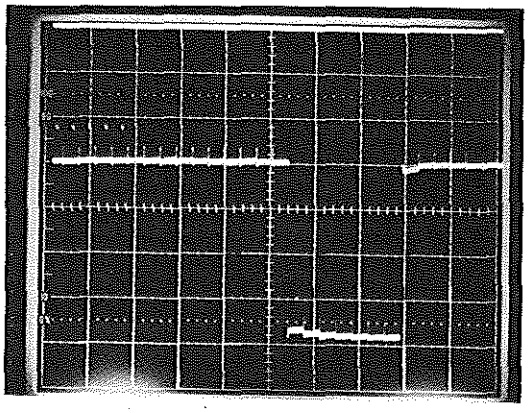


Figure 14. Output for 16-stage CCD 12AT3W. Upper: input at 5 volts/div. Lower: output at 0.5V/div. Both 50 μs/div. 77K temperature and 11° FOV. Stray capacitance = 12 pF.

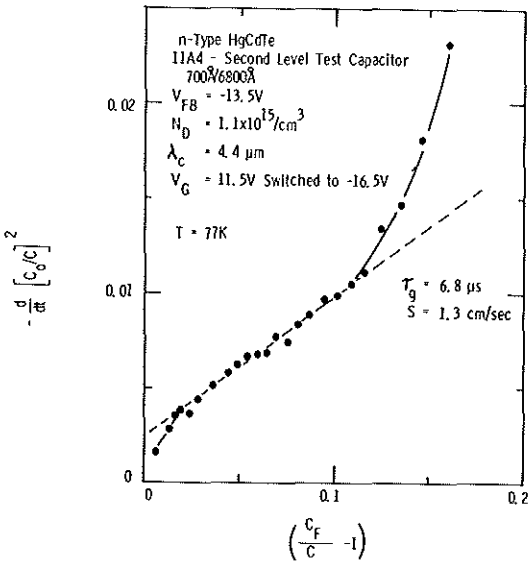



Figure 13. Zerbst plot for second level test capacitor on bar with 11A4WL. Indicated generation lifetime is 6.8μsec and surface generation rate is 1.3 cm/sec.

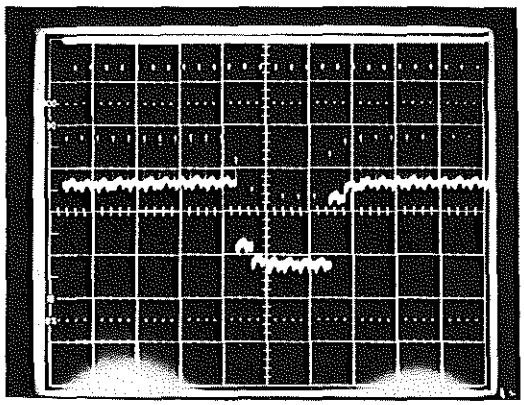


Figure 15. Output from a 32-stage CCD (15AT2) 100 mV/div and 50 μs/div. CTE = 0.997.

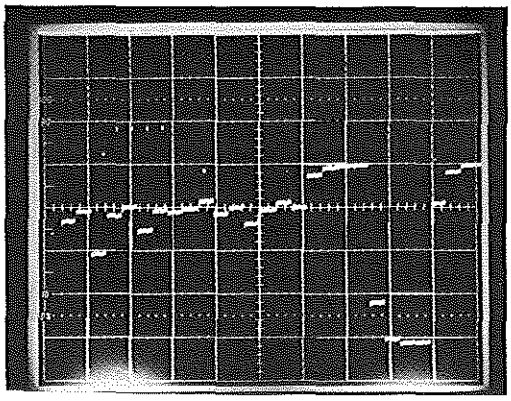
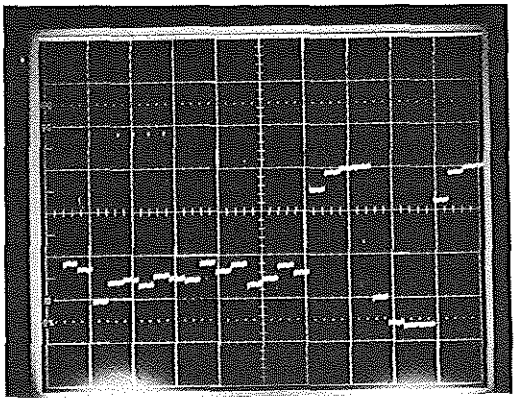


Figure 16. (a) Dark current collected after 1 msec freeze (field plate gate 1.1 volts in accumulation) for 16-stage. CCD-13AT8NR. 500 mV/div and 50 μs/ div.



(b) Dark current for field plate gate 1.8 volts in accumulation.

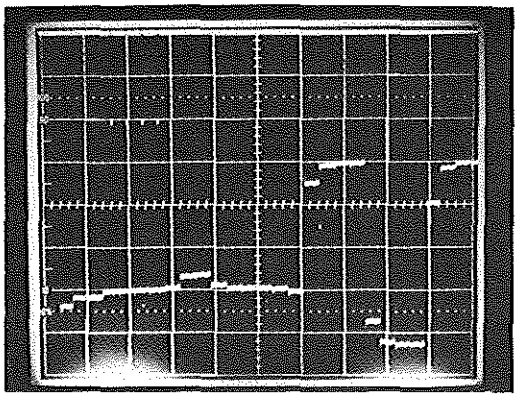
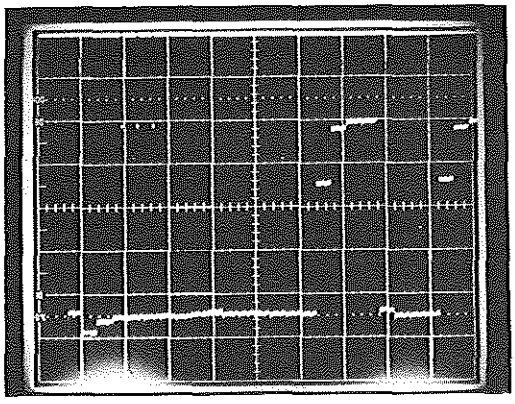


Figure 17. (a) 1.8 msec freeze clock with 20° FOV infrared background for 16-stage CCD-13AT8NR. 500 mV/div and 50 μs/ div. Shadow of gold wire is on bits 9 & 10. Shift register output at right side.



(b) MIS well saturated by 4 msec freeze and increased shift register input.

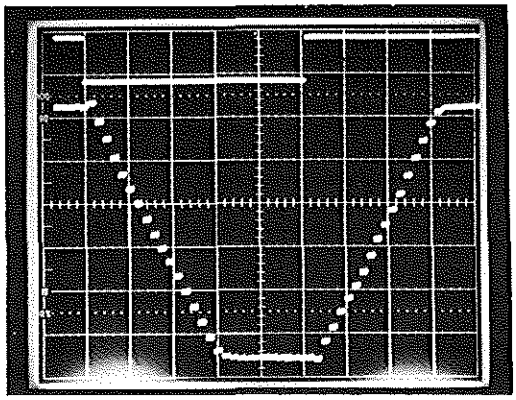


Figure 18. Time-delay-and-integrate operation demonstrated for 16-stage CCD-12AT3 with 50 KHz clocks using a GaAs near-IR diode emitter.

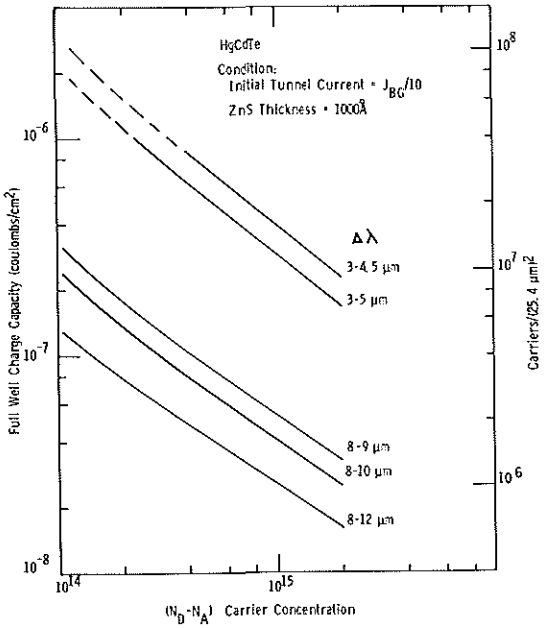



Figure 19. Full well charge predicted for various wavelength bands as a function of carrier concentration.