TECHNIQUES FOR THE DESIGN OF HIGH-DENSITY HIGH-SPEED TDI-CCD IMAGE SENSORS*

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ABSTRACT

New techniques are described for construction of high-speed, high-density TDI-CCD image sensors. The new design concepts incorporated in a 748x96 TDI-CCD test array were: (1) electrode-per-bit clocking of the TDI array which increases vertical resolution, (2) two types of 4:1 output register multiplexing to increase the horizontal resolution, and (3) charge-gating multiplexer and temporary one-horizontal-line storage to achieve a high performance transfer of data from the TDI array to the multiplexed output registers.

A. INTRODUCTION

New techniques are described for the construction of high-speed, high-density charge-coupled image sensors which can be used in future Electronic Message Service systems. An example of one potential application is a high-speed page-reader that would be capable of processing up to 20 standard pages per second. This CCD sensor would have 1728 or 2200 horizontal picture elements and, for improved sensitivity up to 96 time-delay and integration (TDI) vertical elements. The new design concepts required for such a CCD sensor were implemented in a 748x96 element TDI-CCD test array, which was designed and fabricated to study the feasibility of a full-size high-speed 2200x96-element TDI-CCD sensor with 4:1 multiplexed output [1]. The following new techniques were incorporated into this test array:

1. Electrode-Per-Bit Clocking of the TDI Array

The concept of electrode-per-bit clocking, that is now widely used in the area of CCD memories [2,3], was adapted to increase the vertical resolution of the TDI sensor. With four-phase electrode-per-bit clock the vertical resolution of the TDI sensor is increased by a factor of 1.5 above the value obtained for the same gate structure operated with the conventional two-phase or four-phase clock.

2. Output Multiplexing

By using the horizontal output multiplexing a CCD area image sensor can be constructed with very high horizontal resolution that is not limited by the definition of the serial output register [4]. However, in addition to allowing higher horizontal resolution, the output multiplexing also provides an increase in the effective serial scanning rate of the TDI array.

3. High-Speed TDI Multiplexer

A new charge-gating structure has been incorporated in the 748x96-element test array. With this new technique high resolution 2:1 and 4:1 multiplexing of the TDI output can be achieved. Also to minimize the time required to load the four parallel output registers, the concept of a temporary line storage register has been introduced into the multiplexer section. Before discussing these new techniques in detail,

*This work was supported by Naval Ocean Systems Center, San Diego, CA 92152, under Contract No. N00173-76-C-0980.

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it is necessary to consider possible approaches to page-reader systems.

B. HIGH-SPEED CCD PAGE READER SYSTEMS

To satisfy the requirement of reading up to 20 pages per second, a 2200 element line reader CCD sensor should be capable of a horizontal scanning rate of 84 MHz. Since it is difficult to provide drivers for clocking the CCD output register much above 21 MHz, the readout of this array must involve some form of output multiplexing. The four different systems with 4:1 multiplexed outputs considered for this purpose are illustrated in Fig. 1.

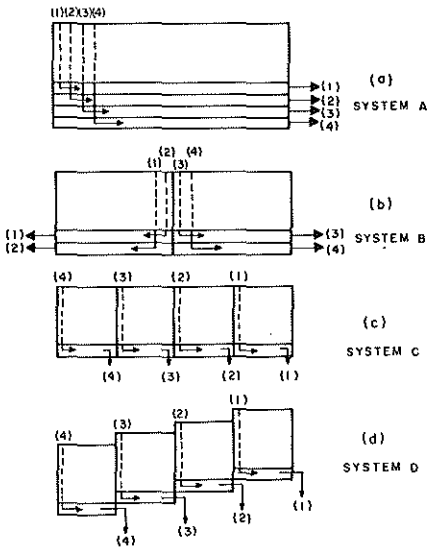

Fig. 1. System organization for TDI array with 4:1 multiplexed output.

System A shown in Fig. 1(a) represents the approach with 4:1 multiplexed output that is capable of the highest horizontal resolution. In this system every four adjacent pixels of the sensor array are transferred into four adjacent horizontal CCD output registers as will be shown. System B, shown in Fig. 1(b), is split into two sections, each having a separate set of 2:1 multiplexed registers. System C, shown in Fig. 1(c), provides the output signals from four simultaneously scanned output registers. This system represents four smaller sensors in adjacent locations designed to form a single and continuous (in the horizontal direction) optical sensor. System D, see Fig. 1(d), was suggested by Frank Martin of Naval Ocean Systems Center. This system is similar to System C, but is designed with each adjacent section (from right to left) displaced down one line of TDI delay. In this system a sequential reading of sections 1, 2, 3, and 4 provides a readout of one continuous line of the TDI sensor array.

A more detailed description of the 4:1 and 2:1 output multiplexing used in Systems A and B is given in Sections D and E. The main advantage of using such horizontal output multiplexing in the design of CCD image sensors is that it allows an increase in the horizontal resolution without the requirement of a simultaneous decrease in the stage length of the output register. This, however, also imposes a trade-off between the improvement in the horizontal resolution and a limitation on the maximum clock frequency at which the output register can be operated with low transfer losses. This loss in transfer efficiency due to the higher order of horizontal output multiplexing is due to the proportionally longer gates in the output register.

The main advantage of an approach such as that used in Systems C and D is that it is not limited by the frequency response of the output registers. However, at the same time this form of output multiplexing imposes the restriction that the length of the pixel in horizontal direction be equal to the length of one stage of the output register.

Finally, a compromise between the improvement in the horizontal resolution and the maximum allowable frequency response is achieved in system B, as shown in Fig. 1(b). This type of splitting of the imager into two parallel sections can be used also to achieve an 8:1 multiplexed output in the form of two sets of 4:1 multiplexed outputs. Such an approach may be desirable if the frequency response of System A is too low to satisfy the required effective serial output scanning rate of 8.4×10^7 pixels per second, and the construction of System B imposes too-small feature length for the design of the dual 2:1 horizontally multiplexed output registers.

C. GENERALIZED ANALYSIS OF MTF ROLLOFF DUE TO TIME-DELAY AND INTEGRATION

The time-delay and integration mode of operation is required since sensitivity must be increased due to the low levels of illumination used in page-reader systems. However, MTF degradation occurs in the TDI mode because the image is moving at a constant velocity while the collecting potential wells move with a "jerky" motion. Thus, the center of the collecting well will move relative to the image with a periodic motion, falling behind, and then jumping ahead, etc. The degree of the MTF degradation due to this effect depends upon the details of the clocking scheme, the gate dimensions as well as the spatial frequency of the pattern being imaged. The following discussion is a generalized analysis of the contrast transfer function (CTF, appropriate for square wave patterns) for electrode-per-bit clocking with unequal gate lengths and three-phase clocking for unequal gate lengths.

1. CTF for Electrode-Per-Bit Clocking of a TDI Sensor

As shown in Fig. 2, this discussion assumes a generalized electrode-per-bit clocking scheme consisting of pairs of gates, one of length L_1 and the other of length L_2, in which p packets are stored under p + 1 gates. Each gate consists of a storage region and a barrier. P + 1 clocks would be required for this scheme. Figure 2 illustrates the progress of a charge packet for p + 1 = 4. After three clock transitions ($t = t_4$), each packet has moved one gate ahead - one quarter of a full stage. Thus, it takes p(p + 1) clock transitions to move the charge pattern to the right one full stage.

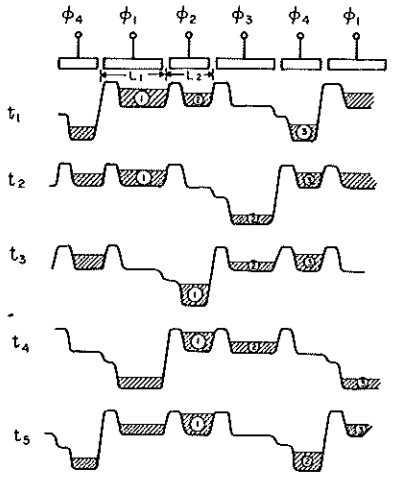

Fig. 2. Operation of a TDI array with four-phase electrode-per-bit clocking, illustrating the presence of the three variable sizes of pixels for each four electrodes.

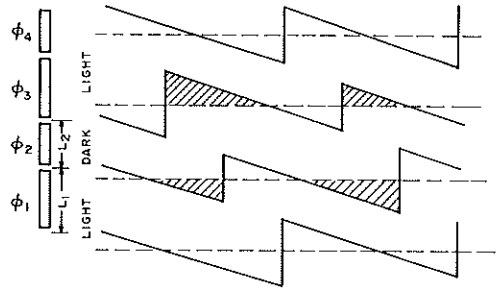

Fig. 3. Position of the collection wells of the TDI array with four-phase electrode-per-bit clocking relative to the moving image in the form of light and dark bar pattern.

Figure 3 shows the position of the collecting wells relative to the moving image (i.e., the reference is assumed to be moving with the image) as a function of time for p + 1 = 4. Six time periods are shown. The light pattern shown corresponds to the Nyquist limit. The relative speed between a stationary well and the image is

$$\frac{\left(\begin{matrix}\text{length of}\\ \text{full stage}\end{matrix}\right)}{\left(\begin{matrix}\text{time to transit}\\ \text{full stage}\end{matrix}\right)} = \left(\frac{(p+1)\ \frac{L_1+L_2}{2}}{p(p+1)\ \Delta t}\right) \qquad (1)$$

where Δt is the time between clock transitions, i.e., $f_{clock} = 1/(p + 1)\ \Delta t$. The shaded areas indicate the regions where the collecting well centered on the dark part of the image extends into the light regions.

The area of the larger triangular shaded region is $\frac{1}{2}\left(\frac{L_1}{2}\right)\left(\frac{L_1}{2}\right)\left(\frac{2p\Delta t}{L_1 + L_2}\right)$. The smaller area is $\frac{1}{2}\left(\frac{L_2}{2}\right)\left(\frac{L_2}{2}\right)\left(\frac{2p\Delta t}{L_1 + L_2}\right)$. There is one of each such triangular areas for every p time periods. Therefore, the fraction for dark in light is

$$\text{Fraction} = \frac{\frac{\Delta tp}{(L_1 + L_2)}\left[\frac{L_1^2}{4} + \frac{L_2^2}{4}\right]}{\Delta tp\,\frac{p+1}{p}\left(\frac{L_1 + L_2}{2}\right)} \qquad (2)$$

$$= \left(\frac{p}{p+1}\right)\frac{(L_1^2 + L_2^2)}{(L_1 + L_2)^2}\,\frac{1}{2}$$

The contrast is reduced by twice this amount since the light wells spend an equal time in the dark, so that

$$CTF = 1 - \left(\frac{p}{p+1}\right)\frac{(L_1^2 + L_2^2)}{(L_1 + L_2)^2} \qquad (3)$$

In this case the resolution center-to-center spacing is given by:

$$D = \left(\frac{p+1}{p}\right)\frac{(L_1 + L_2)}{2} \qquad (4)$$

An example of such a structure would be L_1 = 10 μm, L_2 = 7.5 μm and p + 1 = 4. Here the resolution center-to-center would be 11.7 μm and the CTF at the Nyquist limit would be 0.61735. If all the gates were 10 μm, the center-to-center spacing would increase to 13.3 μm and the CTF would increase only slightly to 0.62500. Therefore, using L_2 = 7.5 μm vs 10 μm would provide a 10% decrease in chip size at a negligible change in CTF.

2. CTF for Three-Phase Clocking

This discussion assumes a standard three-phase clocking scheme but with unequal gate lengths, L_1, L_2 and L_3. Using an analysis similar to the ripple-clocking case, the CTF can be shown to be:

$$CTF = 1 - \frac{11(L_1^2+L_2^2+L_3^2) - 2(L_1L_2+L_1L_3+L_2L_3)}{36(L_1+L_2+L_3)^2} \qquad (4)$$

The resolution center-to-center spacing is:

$$D = L_1 + L_2 + L_3 \qquad (5)$$

An example is a three-phase device with L_1 = 7.5 μm, L_2 = 5 μm, and L_3 = 5 μm. Here the resolution center-to-center is 17.5 μm and the CTF is 0.91213. If the gates were all equal to 7.5 μm, the resolution center-to-center would be 22.5 μm and the CTF 0.91667.

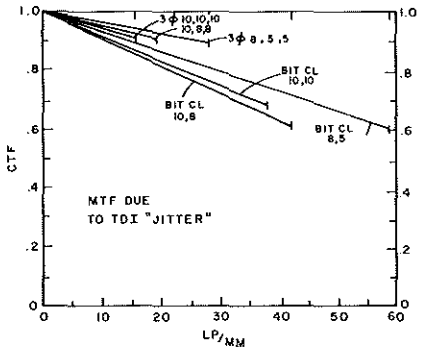

Fig. 4. Contrast modulation function due to the TDI jitter for TDI array.

Finally, Fig. 4 summarizes the CTF rolloff for various configurations. Generally the electrode-per-bit clocking approach results in smaller pixel dimensions and correspondingly higher Nyquist limits but more CTF rolloff. The three-phase approach has better CTF characteristics but larger dimensions.

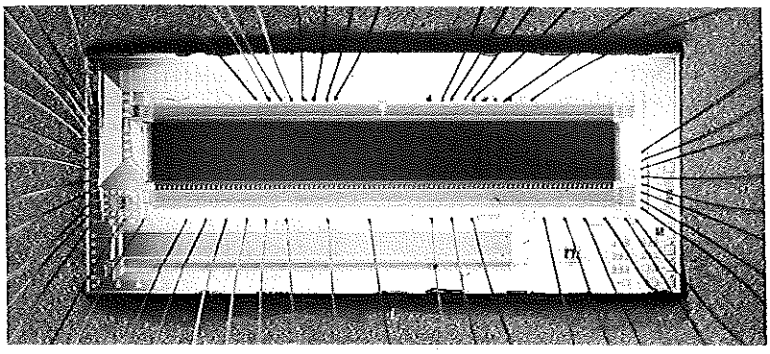

Fig. 5. Page-reader test chip.

D. PAGE-READER TEST CHIP

The photomicrograph of the 14.5 mm x 5.9 mm page-reader test chip is shown in Figure 5. The masks for this chip were masterplates photocomposed from three reticles. The page-reader test chip was fabricated with two-level polysilicon buried-channel CCD technology. A 748x96-element TDI-CCD line sensor with a 4:1 multiplexed output (System A in Fig. 1) was chosen as the main device for the page-reader test chip. The 748x96-element array represents about 35% of the area of the 2200x96-element TDI line sensor, and it contains all of the features necessary for construction of the full-size page reader.

To achieve an effective resolution in the TDI array of 15 μm x 15 μm pixels, the TDI electrodes were designed with 8 μm gates and 3 μm spaces for both levels of polysilicon. The resulting 11 μm electrodes in conjunction with 4-phase electrode-per-bit clocked TDI array results in an effective vertical pixel dimension of 15 μm. The horizontal pixel dimension of 15 μm has been defined by 10 μm TDI-CCD channels and 5 μm channel stops. In addition to the 4:1 output, the 748x96-element TDI array can be read out by a double 2:1 multiplexed output register (System B).

A block diagram of the test array is shown in Figure 6. The main structural difference between the two types of 4:1 multiplexed outputs is that in the case of 4:1 multiplexed output (shown on the bottom), the output registers have 60 μm long CCD stages, while in the case of the double 2:1 multiplexed output the output registers have 30 μm long stages. The advantage of the 4:1 multiplexed output registers with 60 μm stages is that they can be laid out with two-level polysilicon gates using rather non-critical design rules. The layout of 2:1

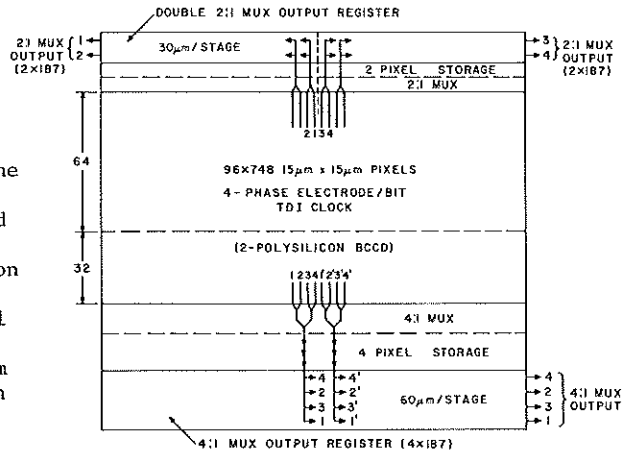

Fig. 6. Block diagram of 748x96-element TDI-CCD line sensor with 4-phase electrode-per-bit TDI clock and two types of 4:1 multiplexed outputs.

multiplexed output registers with 30 μm stages, on the other hand, requires much tighter design rules. The advantage of the double 2:1 multiplexed design is that it offers a higher speed capability. The layout details of the output registers of both the 2:1 and the 4:1 structures are illustrated by the photomicrograph in Figures 7 and 8, respectively.

E. CONSTRUCTION AND OPERATION OF 748x96-ELEMENT TDI-CCD LINE SENSOR

1. General Description of the Device

In this section a more complete description will be given of the construction and the operation of the 4:1 multiplexed output of this TDI array. A schematic sketch of the complete 748x96-element TDI array with 4:1 multiplexed output is shown in Fig. 9. The second-level polysilicon gates are illustrated in this figure by solid lines. The first-level polysilicon gates are shown as dotted lines. In the actual layout the second-level polysilicon gates overlap the first-level polysilicon gates. For simplicity, the first-level polysilicon gates are shown in Fig. 9 as narrower than the actual size. In fact, the spaces between the second-level polysilicon gates in the direction of the CCD channels are intended to represent the length of the first-level polysilicon gates, however, they are not drawn to scale.

2. The TDI Section

Figure 9 illustrates how the 748 horizontal pixels are subdivided into four groups, or four frames, each containing 187 pixels. The 96 TDI elements are composed of 128 electrodes, where each electrode corresponds to two gates (the first polysilicon is the storage gate, and the second polysilicon gate is a transfer gate). Since this TDI array has been designed to operate on a four-phase electrode-per-bit clock scheme it has three vertical pixels for every four TDI electrodes. Since each TDI electrode is made up of two polysilicon gates, the TDI array is clocked by eight separate clocks, shown as ϕ_1 to ϕ_8. In operation of the array, the pairs of clocks ϕ_1 and ϕ_2, ϕ_3 and ϕ_4, ϕ_5 and ϕ_6, as well as ϕ_7 and ϕ_8 have the same waveforms but different dc voltage levels.

3. The 4:1 Multiplexer and Temporary Storage Register

The output from the TDI image sensor section is transferred directly into the parallel to serial multiplexer section. In the multiplexer section, every fourth vertical CCD channel is routed into one of the four horizontal CCD channels. The clocks M1 through M7 are used to provide the timing to clock the charge through the multiplexer. This new charge gating technique allows a layout with very high horizontal resolution. In fact, the resolution of this TDI array, corresponding to 15 μm x 15 μm pixels is limited mainly by the vertical resolution, which in turn is limited by the minimum practical gate length of the TDI array.

Two novel techniques have been developed for the multiplexer section. One technique uses a "window-gate" structure and the other uses ion implanted barriers to control the charge flow in the multiplexer.

The operation of the "window-gate" 4:1 signal charge multiplexer is illustrated in Figs. 10 and 11. This parallel-to-serial signal-charge gating is accomplished by two sequential binary switches. The first charge switch is formed by gates M1 and M2 which separates the channels 1 and 3 from channels 2 and 4. The window gate shown in a top view of Fig. 9 is shown in cross-sectional view in Fig. 10. The cross-sectional structure in Fig. 10(a) applies only to channel 2 and 4. The first polysilicon gate, M1, over these two channels contains a window and the second polysilicon gate that covers this window can be used to control the channel potential in the window. The other channels (1 and 3) have a continuous gate M1 and the charge transfer in that case is conventional.

The ideal operation of the charge gate shown in Fig. 10(a) is illustrated by the potential profile in Fig. 10(b). In this case, when gate M2 forms a barrier (as is illustrated by the solid line in Fig. 10(b)), the signal charge will be prevented from being transferred into the potential well under gate M4. But, when gate M2 is turned on (as is illustrated by the dotted lines), the signal charge originally stored under the left-hand part of gate M1 will be completely transferred to the potential well

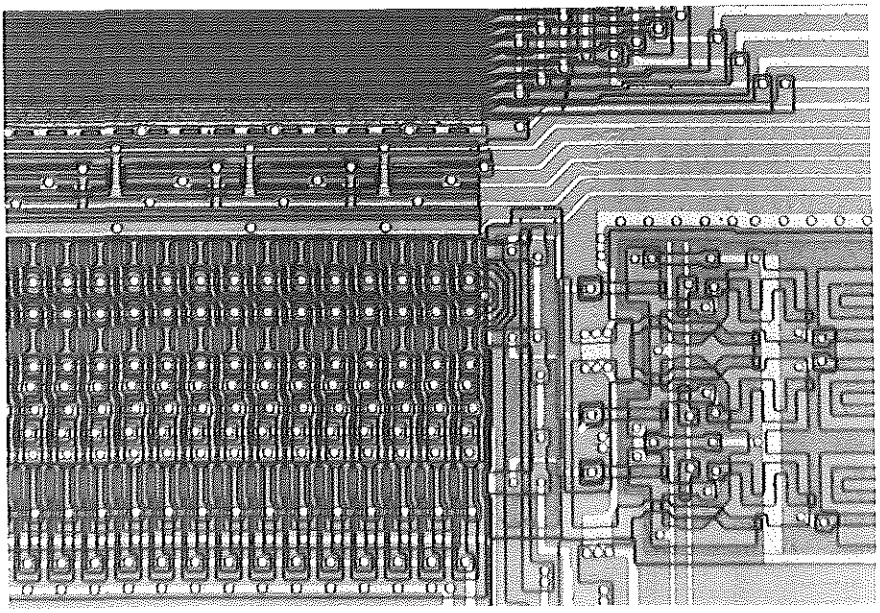

Fig. 7. The output section of the dual 2:1 multiplexed output registers.

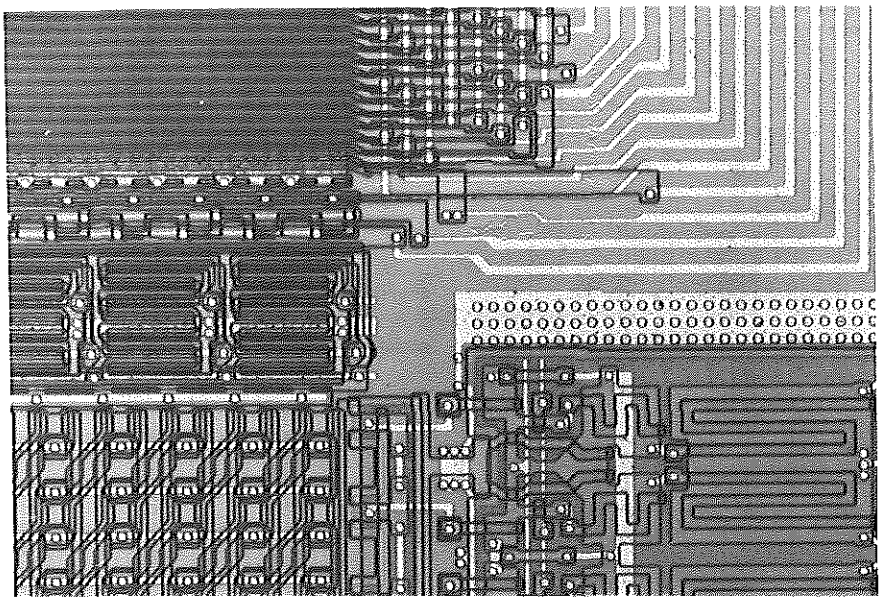

Fig. 8. The output section of the 4:1 multiplexed output registers.

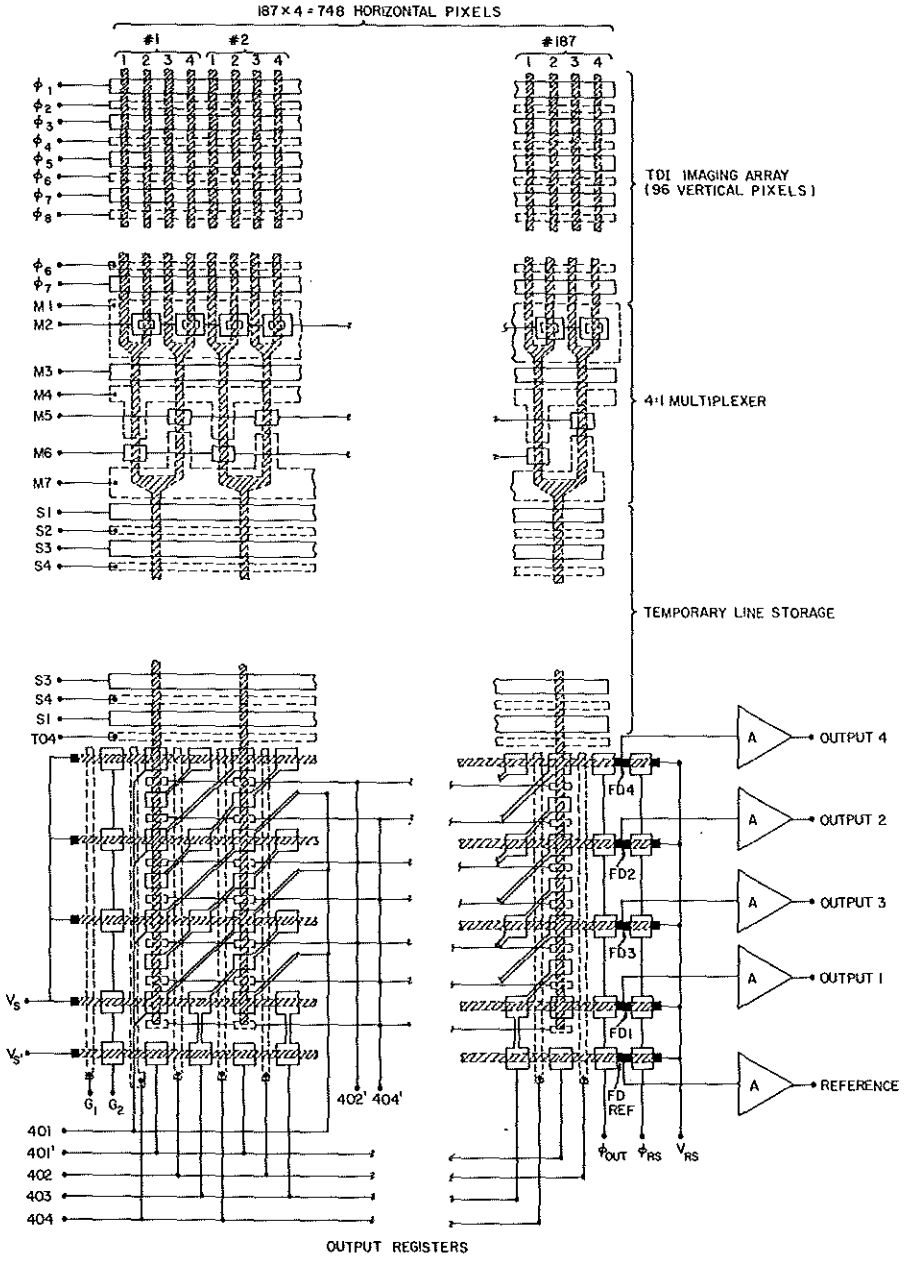

Fig. 9. Schematic layout of the 748x96-elment array with 4-phase electrode-per-bit TDI clock and 4:1 multiplexed output.

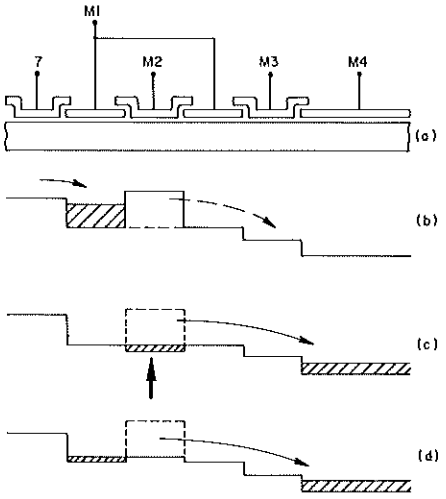

Fig. 10. Construction schematic (a) of the "window-gate" charge switch used in the 748x96-elment array as the first 2:1 multiplexer in Fig.9, and its operation (b), (c) and (d).

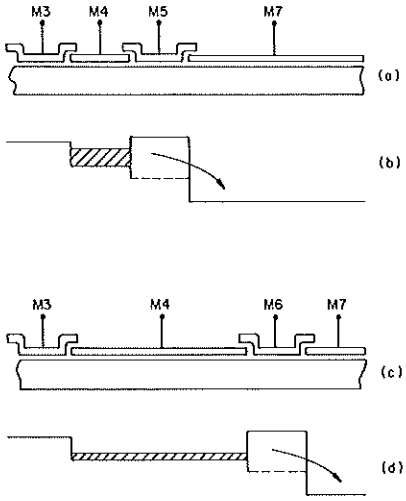

Fig. 11. Construction in (a) and (c), and operation in (b) and (d) of the "interleaved gate" charge switch used as the second 2:1 multiplexer.

under gate M4, which is the receiving well for the next charge multiplexer section.

In actual operation, it is difficult to maintain the channel potential under gate M2 exactly equal to the channel potential under gate M1. Therefore, this charge gate must be operated in one of the modes shown in Fig. 10(c) or Fig. 10(d). Consider the mode illustrated in Fig. 10(c). During the transfer of the charge signal from the well under the left part of gate M1 a potential well is formed under gate M2. This well will momentarily trap some of the signal charge. However, it is possible to make a substantially complete charge transfer, if the fall time of the clock M2 is relatively slow. A slow fall time of M2 will assure that all the original charge under gate M2 is pushed from this well into the potential well under gate M4. Thus, no appreciable amount of charge can be trapped under the left-hand part of gate M1. However, any charge trapped at this position will tend to degrade the vertical MTF of the imager.

The second mode of operation of the charge gate is illustrated in Fig. 10(d). Here, during the transfer of charge to the potential well under gate M4, a potential barrier is formed under gate M2. Due to this potential barrier some charge will always be left behind under the left part of gate M1. This mode of transfer is referred to as incomplete transfer or bucket-brigade mode of operation and contributes to the device transfer loss. In steady-state operation with a bias signal, a fat zero, a typical transfer loss for this type of transfer is on the order of 10^{-3}. However, even without a fat zero, the expected charge transfer loss in this case is expected to be on the order of 10^{-2} (or 1%), which should have a negligible effect on the MTF of the TDI array.

The most important advantage of the first 2:1 multiplexing by the window-gate is that it can be accomplished with very high resolution. The second charge switch is accomplished by the interleaved gates

M4 and M7 which allow the charge to be transferred either by the transfer gate, M5, as is shown in Figs. 11(a) and (b), or by the transfer gate, M6, as is illustrated in Figs. 11(c) and (d). From the operational point of view, this second switch is much more straightforward, however, it does not allow the packing density that is possible with the window gate.

The operation of the implanted 4:1 multiplexer is very similar in operation to the previous approach except the window and the interleaved gates are replaced by implants. A cross-section of channel two is shown in Fig. 12. Channel one has an identical gate structure without the ion implanted regions. Initially the charge is transferred into the storage well under gate M3 in both channels. If M4 goes to an intermediate value between its low and high value, the charge in channel one will flow into the M5 electrode area. However, the charge in channel two will remain under the M3 electrode because of the potential in the ion implanted region. After the charge in channel one has been clocked to the desired location, M4 can be clocked to its high value which will allow the charge under M3 in channel two to flow into the M5 electrode area. The two parallel charge packets have now become serial packets. This structure can be repeated horizontally and vertically for the desired 2:1 and 4:1 multiplexing structures. The advantage of the ion implanted structure is that all gates can have the same minimum geometry and therefore packing density and transfer efficiency is improved. In addition, bucket-brigade mode operation is avoided. However, it does require an extra implant step and slightly more complicated clocking waveforms.

The loading time of the output registers can be minimized by incorporating a temporary storage register which holds four pixels from the multiplexer section, see Fig. 9. The temporary storage section of the array corresponds to four stages of two-phase CCD registers which are powered by clock phases S1 to S4. Here, S1 and S3 are transfer gates, and S2 and S4 are storage gates. The function of this temporary storage register is to allow essentially a full line readout time for multiplexing the TDI output by loading the parallel output registers in minimum time. The output register loading time in this design should take about 2.0 μs, or less than 10% of the minimum line readout time. To insure the minimum time for the loading of the output registers, all of the gates involved in this type of transfer have been strapped by aluminum busses.

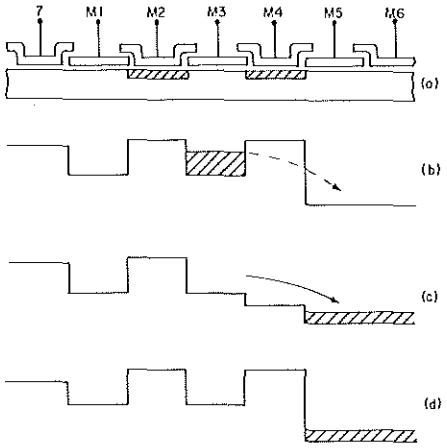

Fig. 12. Construction schematic (a) of the ion implanted charge switch which can be used as a 2:1 multiplexer and its operation (b), (c) and (d).

The temporary storage register is separated from the output register by a transfer gate, T04.

4. The Output Register Section

The construction of the output registers is shown in Fig. 7, 8 and 9. Although this is a schematic representation, it illustrates the general stategy used for the layout of the output registers. There are actually five parallel output registers. Each of these registers has 187 two-phase stages, an electrical input, and a high-speed, source follower output amplifier. The first four output registers serially read out the 4:1 multiplexed output of the TDI array. The fifth output register has been included in this design to serve as a reference channel

for differentially canceling the clock pick-up in the outputs.

The two-phase clocks for the operation of the output registers consist of clock phases 401, 401', 402, 403, and 404; where the clocks 401, 401', and 403 drive the transfer gates and the clocks 402, and 404 drive the storage gates. Other gates and timing clocks for the output register are the input gates, G_1 and G_2. The last gate before the floating diffusion, FD, is ϕ_{OUT}. The gate resetting the floating diffusion to the drain potential V_{RS} is ϕ_{RS}. The voltage V_S is the voltage driving the source diffusions of the first four output registers. The fifth, the reference register, has a separately controlled source diffusion voltage, V_S, so that an independent charge signal can be introduced into the reference register during the readout of the TDI array by the first four registers. In this case, the four output registers will be operated without the electrical input.

The data transfer from the temporary storage section into the output registers is described in the following. In this charge transfer the four-stage temporary storage registers are clocked together with the four output registers in an inter-register transfer mode. The contents of the temporary storage registers are transferred to the four output registers, by a two-phase interregister clocking scheme. The clocks involved in this transfer are S1 to S4, T04, 401, 403, 402', and 404'. During this vertical transfer from the temporary storage section into the output registers, the clock phases 402 and 404 act as channel stops preventing the charge from flowing horizontally in the output registers. Conversely, during the horizontal readout time, the clock phases 402', 404' and T04 act as channel stops, preventing charge flow in the vertical direction.

The floating diffusion, FD, output of each channel is amplified by a three-stage MOS amplifier, to provide maximum dynamic range and frequency response up to the clock frequency of 21 MHz. The first two stages are designed to operate as source followers. The first stage is followed by a sample-and-hold circuit to reduce the output clock noise. The second stage isolates the sample-and-hold circuit from the high-capacitance output device required to drive the load.

F. CONCLUSION

The new CCD imager design concepts incorporated in the 748x96-element page-reader test array include:

(1) Electrode-per-bit clocking of the TDI array to increase vertical resolution.

(2) Output register multiplexing to increase horizontal resolution and the effective read-out rate.

(3) Charge-gating multiplexer and temporary one-horizontal-line storage to achieve a high performance transfer of data from the TDI array to the multiplexed output registers.

ACKNOWLEDGMENT

We would like to acknowledge the contributions to this work of D. Allesandrini, A. R. Criado, W. S. Romito, F. V. Shallcross, and C. Y. Tayag.

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