INTRODUCTION TO CHARGE-COUPLED DEVICES

C. H. Séquin

Bell Laboratories
Murray Hill, New Jersey 07974, U. S. A.

ABSTRACT. The basic concepts of charge transfer devices will be reviewed. In particular, the principles of charge-coupled devices (CCD's) including surface and bulk channel structures and a variety of different electrode arrangements will be discussed. Some of the important parameters characterizing the performance of CCD's will be introduced.

FOREWORD

This lecture intends to give an introduction to the wide variety of charge-coupled devices for the reader who is unfamiliar with the basic concepts. Compared to the extent of the subject, this lecture has been kept rather short since all of this material is covered in a much more extensive and rigorous manner in a recently published book Charge Transfer Devices, from which substantial material and several figures have been adopted with the explicit permission of Academic Press, Inc. [44].

1. HISTORICAL BACKGROUND

The first integrated charge transfer devices were built in the late 1960's in the form of bucket-brigade circuits [1], even though the basic concept of such circuits dates back to Wiener [2]. He proposed the use of capacitors separated by telegraph-type repeaters to store and shift analog information. Later such circuits were implemented with discrete components using bulky buffer amplifiers with vacuum tubes [3] to realize analog sampled data delay lines in which the total delay time

could be varied by altering the driving clock frequency of the circuit. And ultimately such circuits using simple MOS switches between the storage capacitors were built with the silicon integrated circuit technology [1,4].

In 1969, while searching for an electrical analog to magnetic bubble memory, Boyle and Smith [5] conceived the idea of charge-coupled devices. In the simplest implementation CCD's consist of closely spaced capacitors on an isolated surface of a semiconductor. When pulsed in the proper sequence, these electrodes generate moving potential wells which can transport packets of minority carriers. This simple but powerful concept proved to be so stimulating, that almost overnight a host of variations of the electrode structure and dozens of potential applications were conceived. It only took a few days to verify the concept experimentally on an existing structure with closely spaced test capacitors [6]. A few months later the first completely designed CCD was demonstrated as a delay-line and as a simple line imaging device [7]. The idea then caught on rapidly since the scientific community was ready, mentally and technologically, to accept and develop the new ideas.

In retrospect it appears that many workers had been pursuing a route that eventually might also have led to charge-coupled devices. Further development of the integrated MOS bucket-brigade circuits might also have brought forth the more functional viewpoint of moving potential wells. And surface charge transistors [8], in which the source and drain of an ordinary MOSFET are replaced with the inversion layer under an MOS electrode, can also form a charge transfer device, when strung together in series and operated with the proper pulse sequence.

On the practical side there was a well-developed MOS technology awaiting the new concepts. With only small changes in the processing sequence the new designs could be fabricated on existing lines. Starting with only eight elements [7], larger and larger devices were soon built, growing in size at a rate of more than an order of magnitude per year.

Though CCD's were originally conceived as a replacement for binary magnetic bubbles, it became evident immediately that due to their analog charge handling capabilities they could be used in applications other than the storage of digital information. CCD's have been used to build analog delay lines and many related devices such as transversal filters or Fourier correlators, and they have begun to play an important role in signal processing. However, most of the initial enthusiasm for CCD's was generated by their potential use as solid-state image sensors, owing to lack of a practical alternative in the early 1970's. Using the

photoelectric properties of silicon, the information is placed into a CCD by optical means. Incident photons generate minority carriers, which are integrated in the individual potential wells under the transfer electrodes. Subsequently, the information is read out electrically in serial form.

For the first time, charge-coupled devices allowed the implementation of solid-state image sensors which were free of the striation problems of earlier approaches and which thereby demonstrated that the time for the realization of solid-state image sensors with medium to high resolution capabilities and good uniformity had finally arrived.

2. CHARGE-COUPLED DEVICE PRINCIPLE

2.1 The MOS Capacitor

Charge-coupled devices are composed of closely spaced electrodes each of which forms an MOS capacitor. Some aspects of the physics of an MOS capacitor will be reviewed to prepare for the understanding of CCD's. Figure 1 shows a row of MOS capacitors formed by a metal electrode deposited on a thermally oxidized p-type silicon substrate. If at time $t = t_o$ suddenly a positive voltage V_2 is applied to one of the metal electrodes (Fig. 1a), the majority carriers underneath, holes in this case, are repelled, and a potential well forms in the silicon substrate which is at first depleted of free carriers. Subsequently minority carriers, electrons, thermally generated in or near this potential well, will accumulate in this potential well within a layer of less than 10 nm of the interface. The interface potential in the presence of some minority charge Q_{sig} is then given by

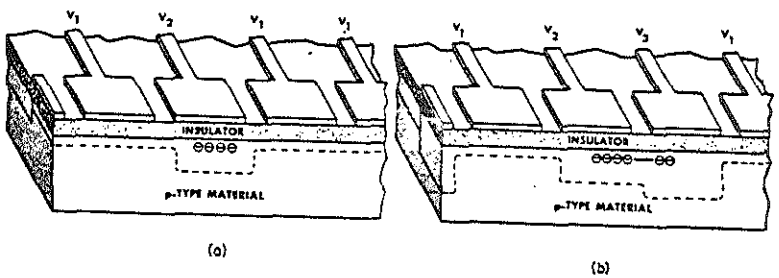


Fig. 1 Basic cell of a 3-phase CCD formed by three MOS capacitors shown (a) during integration and storage and (b) during charge transfer.

$$\varphi_s = V'_G + V_o - (2V'_G V_o + V_o^2)^{1/2} \qquad (1)$$

with

$$V'_G = (V_G - V_{FB}) + Q_s/C_o$$

$$V_o = qN_A\varepsilon_o\varepsilon_s/C_{ox}^2$$

$$C_{ox} = \varepsilon_o\varepsilon_{ox}/d_{ox}$$

where V_G is the voltage applied to the gate electrode; Q_s is the mobile charge in the inversion layer; C_{ox} is the oxide capacitance given by the thickness of the oxide layer d_{ox} and its permittivity ε_o; ε_s is the dielectric constant of the substrate; and N_A its doping density in acceptors/cm^3. As time progresses and the collected charge in the well increases, the interface potential is thus reduced. At the same time the depletion region the width of which is given by

$$X_d = (2\varepsilon_o\varepsilon_s\varphi_s/qN_A)^{1/2} \qquad (2)$$

shrinks, and correspondingly the electrode-to-substrate capacitance increases.

This thermal relaxation time or storage time of the MOS capacitor depends on the quality of the bulk material and on the integrity of the interface and can be several hundred seconds. For time intervals short compared to this relaxation time the MOS capacitor can serve as a storage element for analog information represented by the amount of charge in the well. This charge can be injected electrically or can be generated by photoelectric processes in the silicon. In the latter case the amount of charge contained in the well is a function of the integrated light flux, and the device can thus be used for image sensing purposes.

2.2 Charge Transfer

If two electrodes are placed so closely that their depletion regions overlap and their potential wells merge or "couple" any mobile minority charge will accumulate at the location with the highest interface potential. Thus it is possible to transfer charge in a controlled manner from one electrode to an adjacent electrode. In this context it is convenient to think of the potential well as a bucket and of the minority charge as a fluid that partially fills this container. The potential distribution

of the empty well, plotted with positive values in the downward direction, can be used to depict schematically the size of the bucket, and the potential profile in the presence of charge is used to show the fluid surface of the partially filled well. The area between the two surfaces represents the amount of charge as a liquid sitting at the bottom of the bucket, whereas in the real device the charge resides at the interface. This model has proven very useful in depicting qualitatively the processes in a CCD. In Fig. 1 and in the following cross-sectional drawing of various electrode structures the dotted line represents the potential profile in empty devices.

With two adjacent electrodes simultaneously turned on to the same potential the charge packet will distribute uniformly underneath the two electrodes. When the first electrode is turned off, the charge will be pushed completely to the second one (Fig. 1b). To continue this charge transfer the following electrode is pulsed to a high potential, and so on.

These electrodes can be lumped together in a periodical manner into phase systems, and several packets of charge can then be transferred simultaneously. With the described isotropic electrodes, at least three phases are required to define the direction of transfer. Only one neighbor to an electrode holding charge at a certain moment must be turned "on", and the third electrode in each "cell" must be held at a low potential to act as a blocking electrode that prevents the backward flow of charge. It was this single-level 3-phase principle which was originally proposed [5] and which led to the first realization of a charge-coupled device [7].

Although a 3-phase CCD consists in principle of an array of MOS capacitors which could all be formed with a single mask level, a real device is typically much more complicated. At least four, and normally more, mask levels are required because of the following reasons:

(1) The minority carriers have to be confined laterally in the direction perpendicular to the charge transfer, and thus transfer channels have to be outlined. This can be done either by a channel stopping diffusion or, in the case of an n-type substrate, by a thick field oxide.

(2) The devices normally require input and output diodes in order to be useful.

(3) The topologically unavoidable crossings in the 3-phase electrode structure may necessitate diffused crossunders and contact windows.

The narrow gaps between the transfer electrodes of the described 3-phase CCD are unattractive features. They are frequently subject to metal shorts and thus reduce the yield of these devices. In addition, the interface potential under the bare gaps is poorly controlled. A change in the charging condition of the outer surface can produce potential bumps which inhibit the complete transfer of charge and thus affect the performance of the device in an undesirable way. Other electrode structures have therefore been developed, which result in a completely covered transfer channel, but at the expense of at least one additional mask level.

3. TRANSFER ELECTRODE STRUCTURES

3.1 Nondirectional Electrodes

The first devices with a completely sealed transfer channel used four phases of overlapping electrodes (Fig. 2) formed in two levels of metallization separated by a deposited insulator [8,9]. An insulator of high quality has to be used to avoid interlevel shorts through pinholes and to obtain high yield. Good results have been obtained [10,11] with a thermally grown oxide on polysilicon electrodes in the first level and with aluminum electrodes in the second level (Fig. 3). Alternatively, aluminum can also be used to form the electrodes which are subsequently anodized to form an insulator of the required integrity. The attractiveness of this double level aluminum metallization [12] lies in the high conductivity of aluminum and in the fact that no high temperature steps are required to form the electrode structure.

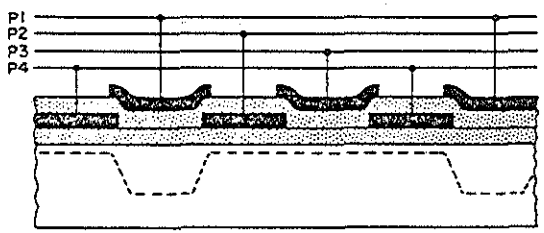


Fig. 2 Four-phase CCD electrode structure employing two metal levels with an intermediate deposited insulator. (Ref. 44)

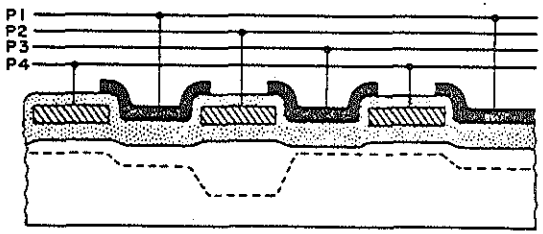


Fig. 3 Four-phase CCD electrode structure employing combination of oxidized polysilicon and metal electrodes. (Ref. 44)

In principle the number of electrodes per CCD cell could readily be increased. However, in most cases this becomes impractical because of the topological problems involved in connecting the electrodes to the many bus lines. With the opposite goal in mind, to shrink the cell size and thus to increase the packing density, the 2-level metallization scheme has also been used to make 3-phase devices. Each phase line then feeds electrodes which alternately lie in the first and second level of metallization. The double level aluminum metallization is especially useful for the implementation of such a 3-phase approach, since both levels can be used to form bus bars of high conductivity (Fig. 4).

Two other approaches have been used to build 3-phase charge-coupled image sensors with a completely covered transfer channel. Using three levels of polysilicon [13] a structure can be built in which each of the three phases is formed in a separate level of interconnection (Fig. 5). The features within each level can thus be made really large though the overall minimum cell

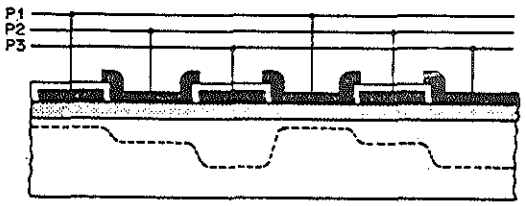


Fig. 4 Three-phase CCD electrode structure formed with two levels of anodized aluminum. (Ref. 44)

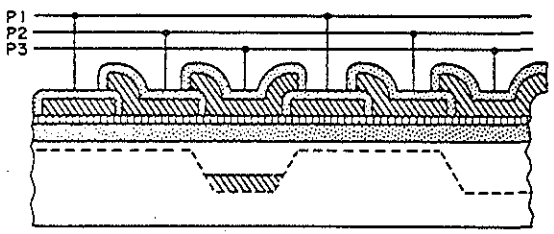


Fig. 5 Three-phase CCD electrode structure employing three levels of overlapping polysilicon electrodes. (Ref. 44)

dimension is still very compact. A major source of trouble can thereby be avoided. Intralevel shorts produced by mask defects, by flaws in the photoresist or by dust in the etching process no longer render a device completely inoperable and are less likely to cause any harm at all. Interlevel shorts, on the other hand, are not more problematic than in 4-phase structures and can be kept at low values when an insulator of high integrity, such as a thermally grown oxide on polysilicon electrodes, is used. A drawback of the 3-level approach is the rather long processing sequence to deposit, dope, define and oxidize the three levels of polysilicon. This approach has also disadvantages when it is applied to image sensors with circuit side illumination where the light has to pass through the electrode structure in order to reach the silicon substrate. Absorption in the polysilicon electrodes results in a significant loss in the blue response, and the many oxide-silicon interfaces cause losses due to reflections and optical interferences [14].

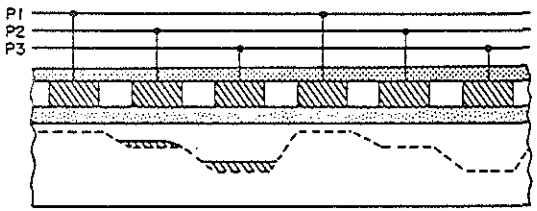


Fig. 6 Three-phase CCD electrode structure in which the electrodes are formed by selective doping of a single layer of high resistivity polysilicon. (Ref. 44)

These losses are minimized as far as possible in a single-level approach (Fig. 6) where the whole active area is covered with a single layer of high resistivity polysilicon in which the electrodes are formed by localized selective doping [15]. The necessary crossovers, address bus lines, light shields and bonding pads are formed in an additional level of true metal.

3.2 Directional Electrodes

In devices with symmetrical electrodes the phase relation between three or more clock systems determines the direction of charge transfer. On the other hand, two clocks are sufficient if the directionality [16] is built into the electrodes. If the potential profile shows an asymmetrical step under each electrode, the signal charge will accumulate in the deeper "storage" part of the well. The charge packets will then remain isolated from one another by the built-in potential "barriers" even when both electrode systems are held at the same potential. Charge transfer will occur only if the two phases are offset by a large enough voltage so that the signal charge can flow from the storage part of one electrode across the potential barrier of its neighbor.

A step in the interface potential can be produced in many different ways. The two most common approaches are a step in the thickness of the gate oxide and a localized change of the doping of the substrate near the interface. Other schemes using different dielectrics, differences in work function or fixed charges in the gate insulator have also been proposed. Even a normal 4-phase device can be operated in a 2-phase mode, by pulsing neighboring electrodes in pairs, suitably biased with a dc-voltage offset.

In Fig. 7 a 2-phase device is shown which is produced by connecting adjacent electrodes in a 2-level structure in pairs [10,11]. If the gate oxide difference under the two metal levels is not producing a sufficiently high barrier, it can be enhanced by an ion-implanted barrier which is self-aligned with the first-level electrodes [17,18]. Other ways to produce stepped-oxide 2-phase CCD's using only a single level of metal rely on the breaks that occur in an evaporated metal at sharp oxide steps. In one scheme the formation of a break is enhanced by forming a deliberate undercut in a dual dielectric structure [19]. In another approach (Fig. 8) the metal is evaporated at an oblique angle onto a castellated oxide to produce step coverage on one edge but a complete break on the other [20]. However, these latter single-level metal structures run into topological limitations in the fabrication of more complicated devices. Furthermore, the open breaks may cause yield or reliability problems.

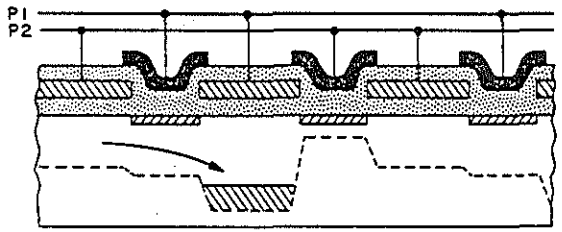


Fig. 7 Two-phase CCD electrode structure employing overlapping electrodes connected in pairs and an optional implant to enhance the potential step. (Ref. 44)

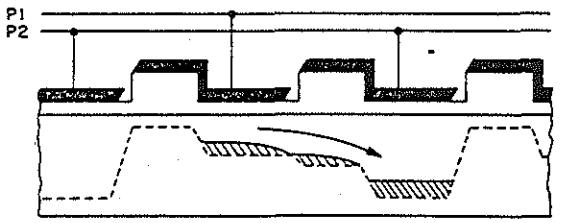


Fig. 8 Two-phase CCD electrode structure employing stepped electrodes formed by oblique evaporation. (Ref. 44)

A potential step can also be produced with a localized ion-implanted region placed under one side of the electrode [21]. However, if the barrier is not properly aligned with the edge of the transfer electrodes (Fig. 9), a potential pocket is formed which retains some charge at all times. In each transfer the signal charge is added to the carriers in this pocket, and in the subsequent transfer across the implanted barrier it has to be skimmed off again from this reservoir of carriers. The amount of signal charge transferred will thus vary with any modulation of the barrier height or width [22].

In that respect the above device operates in a manner similar to an integrated MOSFET bucket-brigade device (BBD) [1,4] which is shown in Fig. 10. In this latter device the storage areas under each electrode are formed by a conductive region of opposite polarity to that of the substrate. The areas between these reverse-biased diodes, having the original substrate doping, form

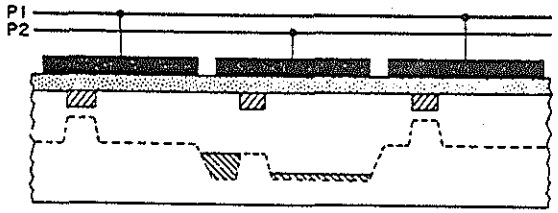


Fig. 9 Two-phase CCD electrode structure employing ion-implanted barriers. (Ref. 44)

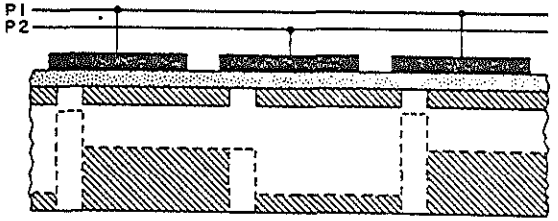


Fig. 10 MOS bucket-brigade electrode structure. (Ref. 44)

the barrier regions. Alternatively, and the way in which these devices were originally conceived, this region can be understood as a MOSFET channel. A BBD is thus an integrated chain of MOSFET's with deliberately enhanced gate to drain capacitances. The two sets of MOSFET's are coupled with their gates to the two phase lines and act as switches which allow the signal charge to flow in a 2-phase manner from capacitor to capacitor. Because of the channel length variation with varying source-drain voltage these devices have limited transfer efficiency (see Section 5) and have therefore not gained too much significance for high resolution image sensors. However, by using special channel geometries or shield electrodes the transfer efficiency of BBD's can be improved substantially [4,23].

To avoid the bare gaps between the transfer electrodes, 2-phase devices with implanted barriers have also been built with a single continuous sheet of high resistivity polysilicon, in which the transfer electrodes are formed by selectively doped areas (Fig. 11). This approach is particularly useful in bulk channel devices (see Section 4) where the stronger fringe fields

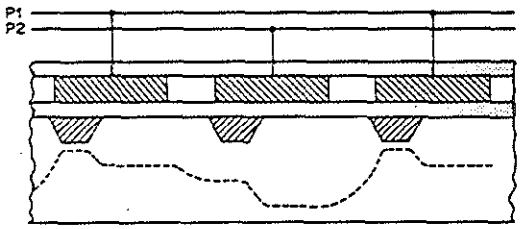


Fig. 11 Two-phase CCD electrode structure using a single layer of selectively doped polysilicon and ion-implanted barriers.

alleviate the registration problems [24] and thus prevent the formation of potential pockets which can retain charge and thereby degrade transfer efficiency.

Many variations of the electrode structures presented in this already rather lengthy list have been proposed, or implemented and are still being invented. Metal electrodes can be replaced by polysilicon electrodes to obtain transparency required for image sensors. Oxidized polysilicon could be replaced with anodized aluminum where speed is the main goal and necessitates high conductivity in the electrodes. Undercutting schemes are used with 2-level electrode structures to reduce the amount of overlap between the two levels, and additional implants can be used to enhance the barrier heights produced by thick-thin oxide steps.

Electrodes placed over oxide steps or using implanted barriers for directionality can be combined in the same device. This has been realized in an offset-mask technique which has been developed to produce high density 2-phase electrode structures. An effective barrier width as small as half the minimum design feature F can be obtained by offsetting one mask against another by half a feature dimension. A first mask is used to form thick-thin oxide steps each of length F. The polysilicon electrodes are then placed offset by F/2 over the thick-thin oxide steps. This forms one phase of directional electrodes. The first polysilicon electrode and the original thick oxide then jointly serve as a mask for a low energy ion implant which forms barriers of width F/2 which are self-aligned with the edges of the polysilicon electrodes. After implantation, the exposed gate oxide is stripped to the substrate, a new uniform thin gate oxide is grown, and the second electrode level is deposited (Fig. 12). In these devices both electrode phases are formed in a separate level of

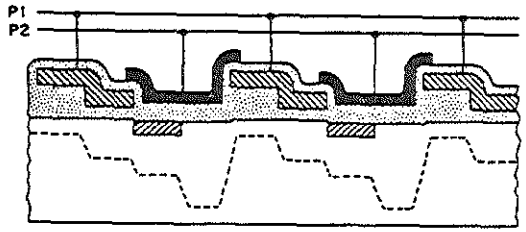


Fig. 12 Two-phase CCD electrode structure formed with offset mask technique using ion-implanted barriers under second level electrodes. (Ref. 44)

interconnection. This results in the same advantages as discussed earlier for the 3-phase 3-level electrode structure: less critical mask feature dimensions and higher yield. The second level is especially uncritical since it could take the form of a continuous strip of metal. This electrode structure looks attractive for the formation of high-density memories, but may be less suitable for image sensors because of the different optical properties of the various MOS structures.

In general, a 2-phase structure can be operated with only one active phase and with the other set of electrodes held at an intermediate constant potential. The active phase is pulsed about the dc phase with a sufficiently large amplitude so that it drains out all the charge from the dc phase in its "on" condition and dumps all the charge in its "off" condition. This principle of operation can lead to a uniphase device [26]. An implanted barrier which defines the directionality is combined with thick-thin oxide areas in such a manner that the thick oxide areas act as a quasi-static phase under which the interface potential varies only a small amount as the single electrode is pulsed (Fig. 13). Two or three implants are used to shift the thresholds in the various areas to the correct value, which allows the potential in the thin areas to be pulsed symmetrically about the thick oxide potential.

The uniphase structure looks attractive from an operating point of view and also for the formation of large memory planes or area image sensors, in which the whole active area could be covered by a continuous sheet of metal. However, because of the many processing steps required to build such a structure, the tight tolerances on the implants and the low signal handling compared to the applied pulse potentials, it remains questionable, whether this structure will gain commercial significance.

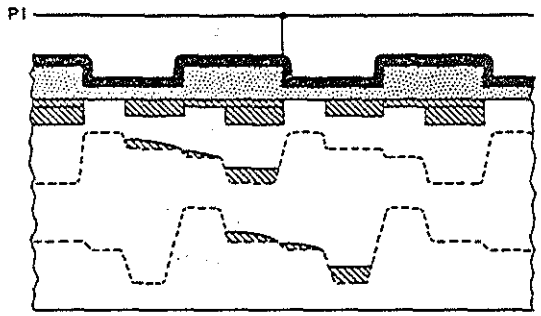


Fig. 13 Uniphase CCD electrode structure employing a combination of thick-thin oxide steps and various implanted regions. (Ref. 44)

4. SURFACE AND BULK CHANNEL CCD'S

The interaction of the signal charge packets with interface states imposes certain lower limits on transfer inefficiency and transfer noise (see Section 5). To prevent this interaction the effective transfer channel can be located away from the Si-SiO_2 interface deeper into the bulk of the device [27,28]. This can be achieved with the use of an epitaxial or ion-implanted silicon layer of opposite polarity to that of the substrate. This layer is in electrical contact with the output diode (Fig. 14), which drains out all mobile carriers when suitably reverse biased. The potential minimum under each transfer electrode will then be formed inside this layer, but generally away from the Si-SiO_2 interface. Its exact location depends upon the doping profiles, the applied voltages and the amount of signal charge present (Fig. 15). The clock pulses applied to the transfer electrodes modulate the channel potential to produce moving potential wells just as in the case of a surface channel charge-coupled device (SCCD). In these bulk channel charge-coupled devices (BCCD) which have also been called "buried channel CCD's" [27,29] or "peristaltic CCD's" [28] the signal charge moves completely inside the bulk of the silicon. The carriers thus never come in contact with the interface states. However, similar trapping and re-emission action now takes place with the traps in the bulk of silicon, but the effective density of these traps which interact with the signal is normally much lower than typical densities of interface states [30].

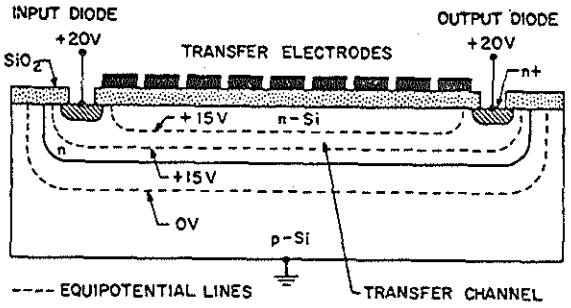


Fig. 14 Longitudinal cross section through a bulk channel CCD showing the channel layer in contact with the reverse biased input-output diodes and equipotential lines which indicate the actual position of the transfer channel.

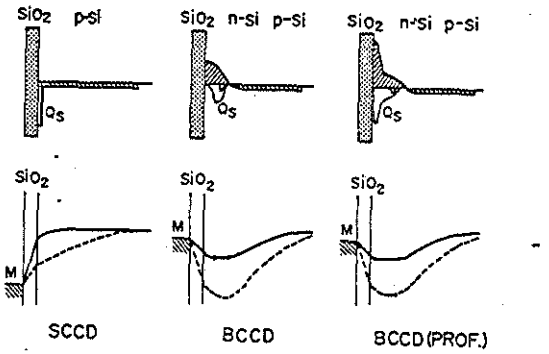


Fig. 15 Schematic doping profiles and charge distribution (top) and potential distribution (bottom) perpendicular to the semiconductor surface in a surface channel CCD, a bulk channel CCD, and a BCCD with a profiled channel. The dashed lines represent the nearly empty well and the solid lines the profile in the presence of a substantial charge packet.

The region of depleted silicon between the signal charge and the gate oxide increases the effective thickness of the gate insulator. The fringe fields thus are considerably stronger than in an SCCD of comparable geometry and will speed up the transfer of charge (see Section 5). Devices with a 5 μm thick epilayer have been operated at clock rates above 100 MHz [31]. On the other hand, a thicker effective gate insulator reduces the capacitance per area and thus the signal handling capability. To obtain maximum signal handling, a shallow implant concentrated near the $Si\text{-}SiO_2$ interface is required. However, the best features of both devices can be combined. The combination of a lightly doped epilayer and a shallow concentrated implant generates a profiled channel [32] which carries large packets close to the surface but has a potential minima which lies deep in the bulk in the presence of small packets (Fig. 15). This structure thus combines a large signal handling capability with strong fringe fields which speed up the transfer of the last fraction of charge.

The choice between a surface channel or one of the bulk channel devices will mainly depend on the performance required in a particular application. The lower transfer inefficiency and noise and the higher operating speed of a BCCD are bought at the expense of a more complicated processing sequence.

5. PERFORMANCE PARAMETERS

5.1 Signal Handling Capability

To first order the amount of charge Q_s which can be stored in each individual potential well depends on the "size of the bucket"

$$Q_s = A \cdot C_{ox} \cdot V_p, \tag{1}$$

i.e., its active area A and its "depth" given by $C_{ox} \cdot V_p$ where C_{ox} is the gate oxide capacitance per unit area and V_p is the pulse potential applied to the electrode with respect to the neighbor electrodes. The amount of signal current I_s which can flow through a 3-phase device pulsed at an element or clock rate f_c then becomes

$$I_s = A \cdot C_{ox} \cdot V_p \cdot f_c. \tag{2}$$

Devices with more than three symmetrical electrodes per unit cell can be operated in a special mode where more than only one electrode is turned on at all times. The maximum signal current I_s can then be

$$I_s = (p-2) \cdot A \cdot C_{ox} \cdot V_p \cdot f_c \tag{3}$$

where p is the number of phases. This mode has some significance in 4-phase devices where it can effectively double the signal handling capability.

In devices with symmetrical electrodes the clock amplitudes V_p can, at least in principle, be adjusted within reasonable limits to match the required signal. At the lower limit, minimum pulse amplitudes of typically about 1-2 V are required to overcome anomalies in the potential distribution at the edges of the electrodes or threshold voltage differences between adjacent electrodes. An upper limit for V_p is reached when the fields at the oxide-silicon interface become strong enough to produce avalanche breakdown. The generated carriers would then flood the potential well and lower the interface potential. In the presence of a full charge packet the main potential drop occurs across the gate oxide, which also has a limited breakdown strength of about 5×10^6 V cm^{-2}, or about 50 V for a 100 nm thickness. The maximum number of electrons that can be stored at the $Si\text{-}SiO_2$ interface is thus on the order of 10^{13} cm^{-2}.

In 2-phase devices the maximum signal current and the necessary operating pulse potentials are more or less predetermined by the built-in potential step or barrier, although in most devices the step height also scales to a certain extent with the applied clock potential. For electrodes with a built-in barrier $\phi_b(V_p)$ and a storage part of area A_{st} with a capacitance per unit area C_{st} the signal handling capability is

$$Q_s = \phi_b(V_p) \cdot A_{st} \cdot C_{st}. \tag{4}$$

Since $\phi_b(V_p)$ normally increases with applied electrode voltage, the device will have the highest signal handling capability when operated with overlapping clock pulses, also called push clocks [33], so that one electrode is fully turned on before the other one turns off. This mode of operation is also more advantageous than the nonoverlapping or drop clock mode with regard to obtaining best transfer efficiency (see Section 5.2).

If 2-phase devices are operated with clock amplitudes which do not exceed the built-in barrier height $\varphi_b(V_p)$, then not all charge can transfer from one well to the next, and the device then operates in the incomplete charge transfer mode or bucket-brigade mode. The amount of charge retained behind the barrier in the previous well is not absolutely constant but is modulated by changes in the barrier height or width, which depend on the amount of signal charge transferred. This mode has thus serious drawbacks with respect to the transfer efficiency that can be obtained.

5.2 Transfer Efficiency

In a suitably designed 3-phase CCD, which is operated with sufficiently large clock pulses, eventually all the charge would flow from one well to the next, if enough time is allowed for this transfer. The main fraction of a reasonably large charge packet will transfer within a very short time on the order of only a few ns under the influence of the self-induced electrostatic forces. But once the charge density remaining under the sender electrode has fallen to about 10^{10} electrons/cm^2 the final stage of the charge transfer is governed by thermal diffusion. The time constant with which the last few percent of charge flow from the sender electrode will thus increase with the square of the electrode length. For a 10 µm long electrode it is about 30 ns.

If insufficient time is allowed for the transfer, the sender well cannot empty to a negligible fraction, and a small signal dependent amount of charge is left behind. This effect is cumulative and can amount to substantial signal degradation after many transfers. Assuming that a constant fraction ε of the signal is left behind, an isolated charge packet which has undergone n transfers will be reduced by a factor

$$Q_{out} = Q_{in}(1-\varepsilon)^n \approx Q_{in}(1-n\varepsilon) \qquad (5)$$

and the subsequent, originally empty packet will have accumulated some residual charge

$$Q_{res} = Q_{in}(1-\varepsilon)^n n\varepsilon \approx Q_{in} \cdot n\varepsilon. \qquad (6)$$

The approximations hold as long as the "inefficiency product" $n\varepsilon$ is sufficiently small compared to unity, so that second order terms can be neglected. The degradation of a single charge

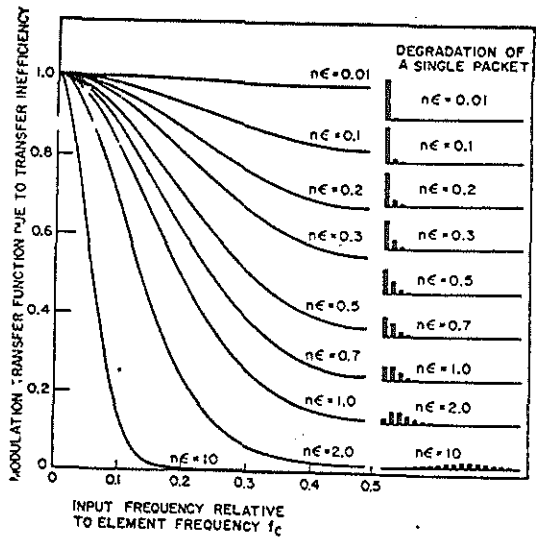


Fig. 16 Effect of incomplete transfer on the modulation transfer function and on the appearance of an isolated charge packet for different values of the inefficiency product nε. (Ref. 43)

packet for increasing inefficiency products nε is illustrated on the right-hand side of Fig. 16.

The curves on the left-hand side represent the signal degradation in the frequency domain calculated from the same linear model. Charge transfer devices are analog sampled data systems, and the maximum signal frequency f which can be properly represented is equal to half the clock frequency f_c. The transfer functions have thus been normalized with respect to f_c. The stronger roll-off towards higher frequencies with higher inefficiency products nε is evident. For imaging devices nε products in excess of 0.3 would lead to a noticeable loss of resolution near the Nyquist limit.

As an introduction we had considered the limitations imposed on transfer efficiency by the clock rate and the thermal diffusion time constant. Obviously shorter electrodes will permit higher speed of operation. However, in practice it is just as effective to use substrate materials of high resistivity and

thicker gate insulators. Then the fringe fields will reach under the electrodes and the carriers will move much more rapidly under the influence of these drift fields [34-36]. This effect becomes especially important in bulk channel devices [37]. If it were only for the limitations discussed so far, transfer inefficiencies below 10^{-6} could readily be obtained at MHz clock rates.

In bucket-brigade devices, or in 2-phase CCD's operating in the incomplete transfer mode because of insufficient clock pulse amplitudes, the speed of the transfer is limited by the bottleneck represented by the MOSFET channel or by the barrier region. Furthermore, the length of this channel or the height of the barrier is modulated by the signal charge transferred. Thereby the charge retained in the previous well is also a function of the signal packet size. Typically the transfer inefficiency is on the order of 10^{-3} unless special care is taken to reduce these modulation effects.

In devices with electrode separations of a few micrometers such as the original 3-phase CCD, or in 2-phase CCD's with improperly aligned implanted barriers, spurious potential bumps can form which also retain part of the signal charge. Normally these undesired barriers are narrow and largely dominated by fringe effects. The modulation effects due to the signal charge can then be especially strong, and the device will show a correspondingly poor transfer efficiency [38,39].

In CCD's of proper design operating in the complete transfer mode the dominant mechanism producing transfer inefficiency is due to the interaction with interface states [40,41]. A signal charge packet coming in contact with empty interface states will supply the necessary charge to fill these states almost instantaneously. As the charge packet moves on, these interface states release the captured charges again but with considerably slower time constants which depend on the energy levels of the states in the band gap. Many carriers will thus be released too late so that they can no longer join their own charge packet but will be added to one of the following packets, and they will thus produce a small tail following the last full charge packet. The loss experienced by the first full packet of a sequence increases with the time elapsed since the last transfer of charge through the device (Fig. 17a), since all interface states which have emptied in the meantime have to be refilled.

This effect can be mitigated by operating the device with some bias charge also called "background charge" or "fat zeros" (Fig. 17b). In this mode most of the interface states are kept filled during most of the time and ideally each signal packet would lose into the interface states the same amount of charge which it would gain from the previous packet. In reality this

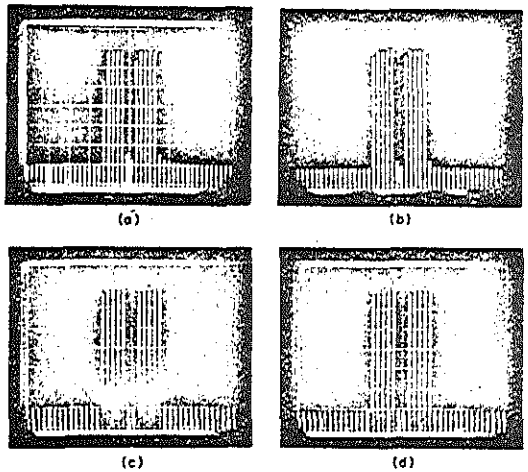
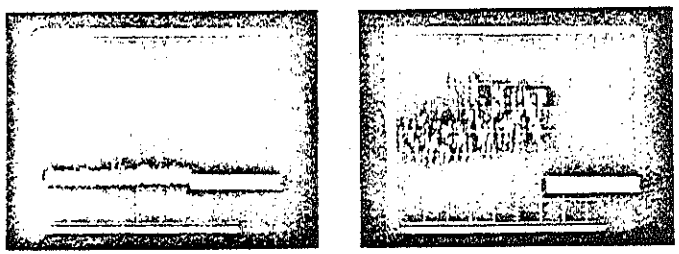


Fig. 17 Output signals observed on a 256-element 3-level 3-phase CCD: (a,b) on an SCCD and (c,d) on a BCCD, both without and with a 10% bias charge. (Refs. 13 and 30)

cancellation is not perfect since the size of a charge packet increases somewhat with its charge content. A full charge packet will thus reach a larger number of interface states at the edges of the potential well than a bias charge packet does. This remaining residual edge effect limits the transfer efficiency in wide channel devices to the range of 10^{-4} to 10^{-5}. In principle the same effects take place in bulk channel devices owing to interaction with the traps in the silicon bulk. However, because of the lower effective trap density, transfer inefficiencies below 10^{-5} can be obtained in BCCD's (Fig. 17c,d) [13].

5.3 Dark Current

In the potential wells of a CCD, as in any solid-state image sensor, thermally generated carriers are added to those produced by the incident light. The two most important sources in a potential well under an MOS electrode are the generation of carriers via midband states located at the Si-SiO_2 interface and in the depleted silicon bulk. This dark current background will thus appear superposed on the video signal. Since the generation rate



(a) (b)

Fig. 18 Integrated dark current distribution in a linear CCD for integration times of (a) 0.1 s and (b) 1 s, respectively, showing noisy background and several individual dark current spikes. (Ref. 44)

is not uniform over the whole device, the granularity of this background will typically set a lower limit to the amount of light required to produce an image of a certain quality. Of course, the dark current contribution increases with longer integration times (Fig. 18), and it can be reduced by cooling the device.

In present-day devices the average dark current is in the range from 1 to 10 nA cm^{-2}. At this rate a potential well under an electrode pulsed to 10 V would be completely filled in about 10 s. These numbers include already the more complicated processing sequence required to make a real device. Much longer storage times can be obtained on isolated MOS capacitors.

In addition to the dark current accumulated in the integration sites, some consideration has also to be given to the contribution of the readout registers. In principle all packets which pass through the same registers at the same transfer rate will get the same dark current contribution, and nonuniformities will thus average out. Furthermore, the readout time is normally not longer than the integration time, and thus if the dark current is low enough to give adequate levels in the unaveraged integration sites, the contributions in the readout registers can typically be neglected. In surface channel devices the latter dark current component even has a beneficial aspect since it provides an automatic bias charge which improves transfer efficiency.

5.4 Noise

The noise in the video signal can, of course, never be lower than the fluctuations given by the Poisson distribution of the randomly arriving photons. The variance of this noise is given by the square root of the number of collected carriers and thus gets lower as the light flux is reduced. The thermal noise at the input of the preamplifier and other system noise, however, are constant and will thus become dominant in low light level applications.

In addition to these general considerations, the signal in a CCD is subject to transfer noise. The amount of charge left behind in each transfer has not only a systematic dependence on the signal, which results in transfer inefficiency, but also shows statistical fluctuations introducing additional noise [40,42]. These fluctuations are related to the absolute amount of charge which is captured and subsequently reemitted in each transfer. In a well-designed device, operating in the complete charge transfer mode, the transfer noise will then be determined mainly by the density of interface states or bulk traps. For this reason surface channel devices will exhibit more transfer noise than bulk channel devices. Furthermore, in SCCD's the size of the charge packet and therefore the transfer noise are fairly constant, while in BCCD's the size of the charge packet varies with its charge content. At low signal levels the signal packets interact with fewer bulk traps, and the BCCD has therefore much less transfer noise. This is also the reason that BCCD's, when operated at small signal levels with no additional bias charge, still exhibit good transfer efficiency [30].

6. CONCLUSION

A wide variety of designs of charge transfer devices are available and their operation is well understood. For high-resolution image sensors considerations of good transfer efficiency and low noise are dominant. For this reason devices such as 2-, 3-, and 4-phase CCD's operating in the complete charge transfer mode are used almost exclusively at present. For low light level applications bulk channel devices are preferred. Other important considerations are long storage times, or low and uniform dark current. This latter property is strongly technology dependent. A great deal of effort is currently being spent to develop processes which meet all of the above specifications and which produce defect-free devices with high yield.

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5.0 METHODS FOR INTRODUCTION OF ELECTRICAL INPUT

5.1 Current Integration Input

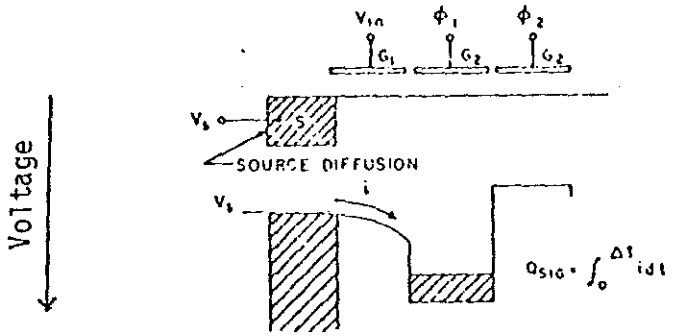


FIGURE 1

The source diffusion S in conjunction with the input gate G_1 forms a current source that introduces charge into the input potential well under the electrode G_2. Other terms used are: current input and dynamic current injection.

5.2 Voltage Input

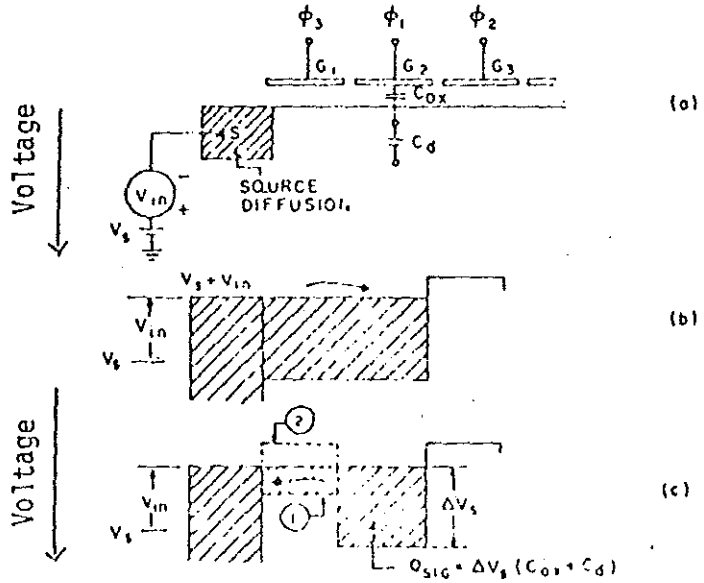


FIGURE 2

(a) Input structure

(b) Potential diagram which illustrates the filling of the input metering well under electrode G2 to the source potential, $V_S + V_{in}$.

(c) 1) During the turn-off time of electrode G1 the charge in the conducting channel under gate G1 is returned to the source diffusion S.

2) When the channel under electrode G1 is cut off, a charge packet Q_{sig} is retained under electrode G2, which is at the same potential as the source diffusion.

Other terms used: gate diode input, reverse biased diode input, transmission gate input.

5.3 Charge-Preset Input

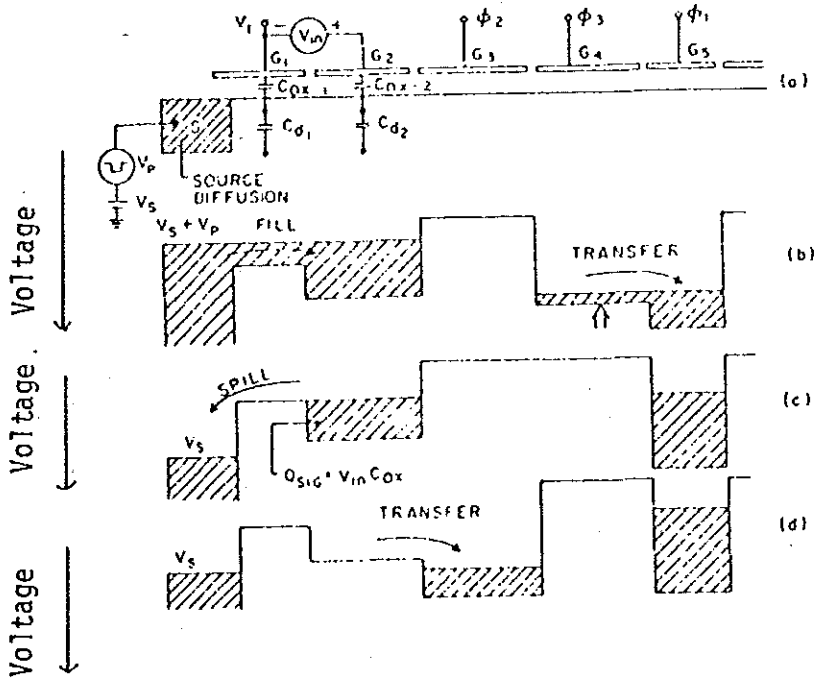


FIGURE 3

(a) Input gate structure; (b) and (c) potential profiles illustrating the fill and spill operations; (d) potential profile showing the transfer of input charge signal, Q_{sig}, from the input well to the CCD register. Other terms used: potential equilibration input, stabilized charge input, and fill-and-spill input.

5.4 Voltage-Preset

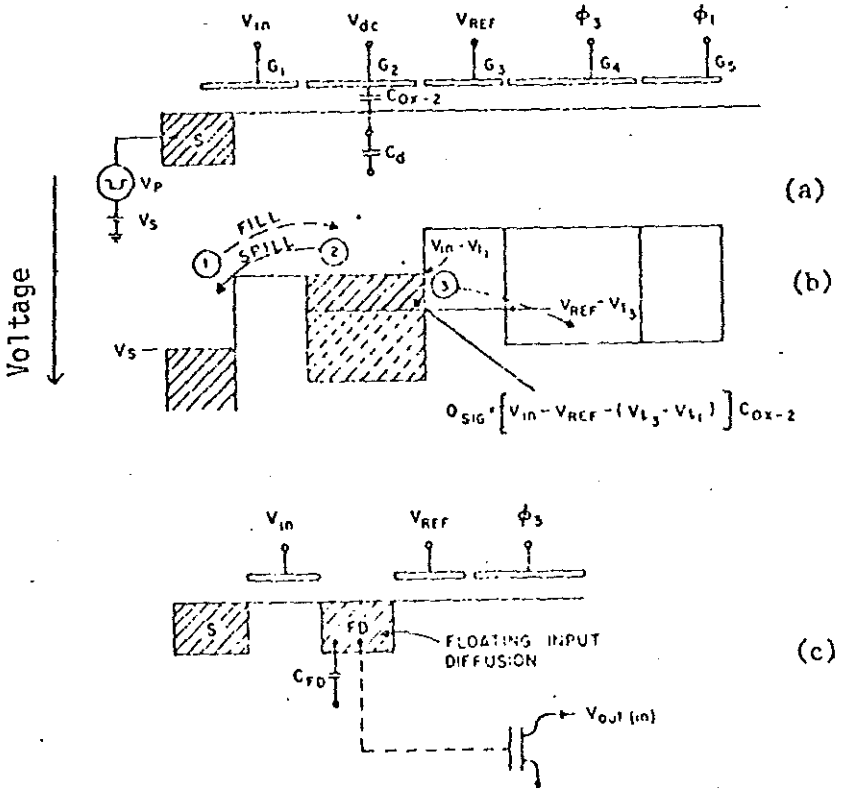


FIGURE 4

This input method is a special form of charge-preset input in which the charge in the input metering well is never completely emptied. This metering well can be formed under a d-c biased

electrode G2 as shown in (a) or by a floating diffusion as shown in (c). In operation the input/metering well is preset with charge by method 5.3. Subsequently, voltage V_{ref} is applied to G3 and a charge packet is transferred into the charge transfer channel. A version of the voltage-preset input method that is insensitive to MOS threshold voltage is shown in Figure (d).

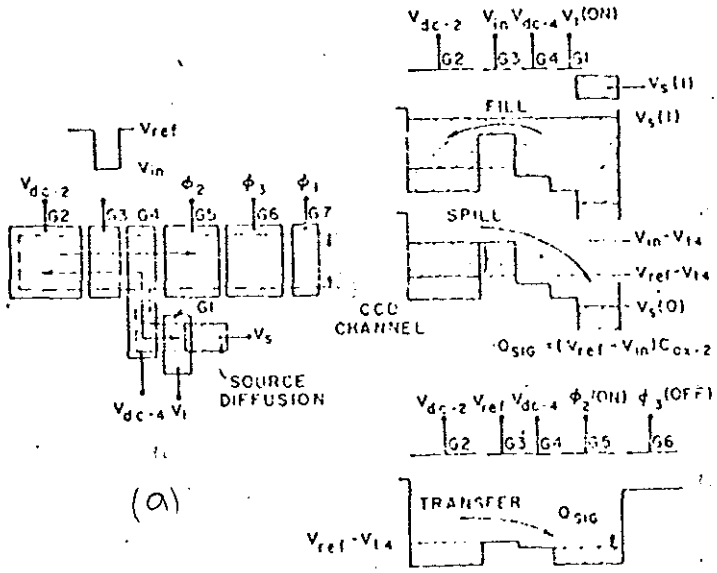


FIGURE 5

In this case the charge packet is preset with the same electrode that controls the size of the charge packet that is moved into the transfer channel.

6.0 TYPES OF OUTPUT CIRCUITS

6.1 Current Output

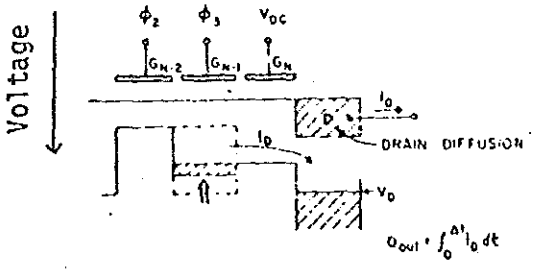


FIGURE 6

The current from the output diode or drain diffusion is measured directly.

6.2 Floating Diffusion Amplifier (FDA)

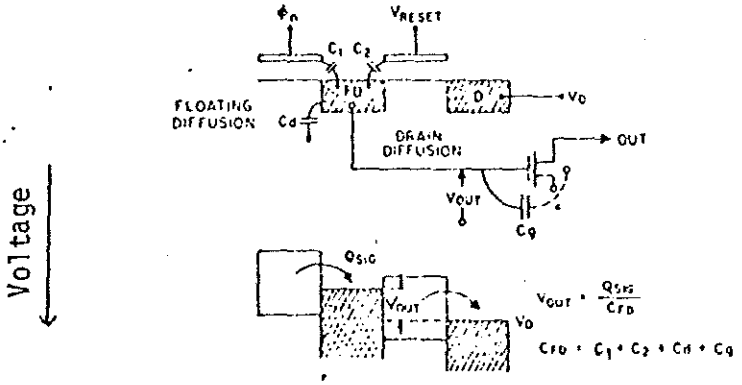
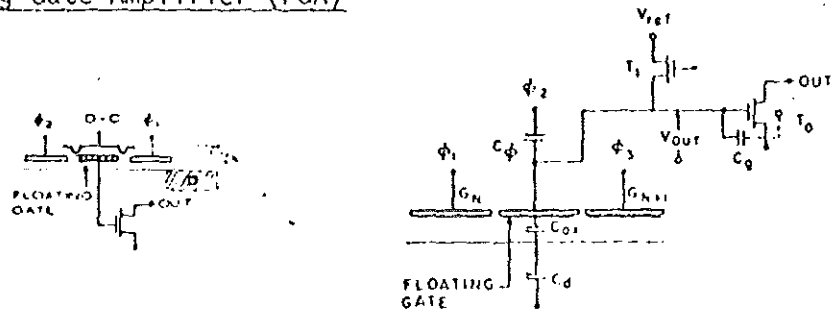


FIGURE 7

The floating diffusion is a sense node connected to the gate of a MOSFET. It is usually reset every clock cycle to a fixed potential via a reset gate or a transfer electrode. This amplifier is also known as the gated charge integrating (GCI) amplifier.

6.3 Floating Gate Amplifier (FGA)



a) (b)

FIGURE 8

Fig. 8(a) and 8(b) show two versions of a floating gate amplifier. In (a) the floating gate is permanently isolated while in (b) it is periodically reset.

6.4 Distributed Floating Gate Amplifier (DFGA)

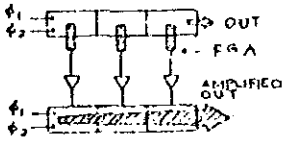


FIGURE 9

The signal is sensed non-destructively several times at successive FGA's in one CCD and is regenerated coherently into a second parallel register with parallel inputs which is clocked at the same rate. This time delay summation of the outputs, ideally, improves the rms power signal-to-rms.noise ratio by a factor $\sqrt{N}$ for N FGA stages. It should also decrease significantly coupling into the output of many clock subharmonics.

6.5 Correlated Double Sampling (CDS)

A method of readout which eliminates reset noise inherent to the floating diffusion amplifier. In operation, after reset, the reset voltage level V_1 is measured and stored. The signal is then transferred onto the sense node and this voltage V_2 is measured. The measured values V_1 and V_2 are then subtracted. If the time between measurements is<<RC (where R is the off resistance of the reset switch and C is the sense node capacitance), the reset noise is removed.

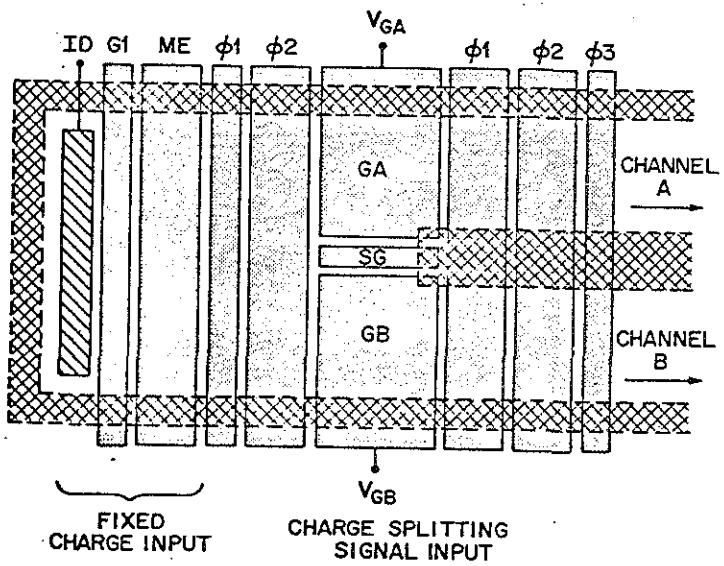
A SYMMETRICALLY BALANCED LINEAR DIFFERENTIAL CHARGE SPLITTING INPUT FOR CHARGE-COUPLED DEVICES

by

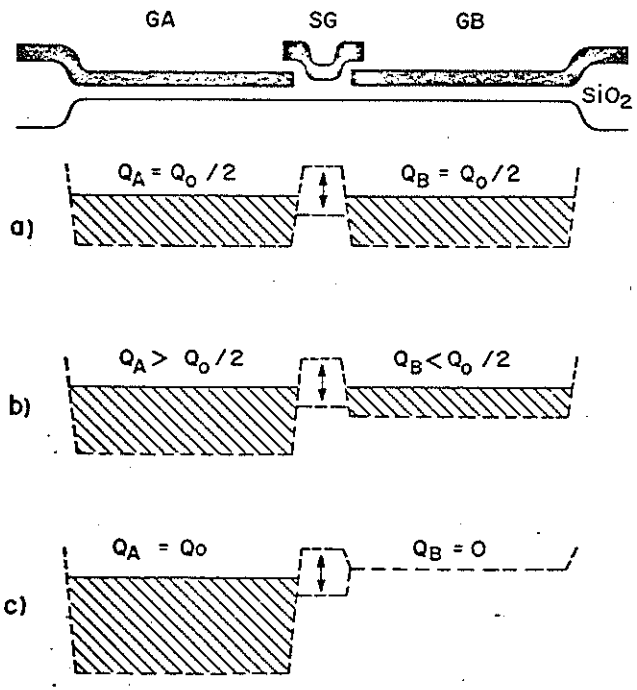
C. H. Séquin, M. F. Tompsett, D. A. Sealer, and R. E. Crochiere
Bell Laboratories
Murray Hill, New Jersey 07974

ABSTRACT

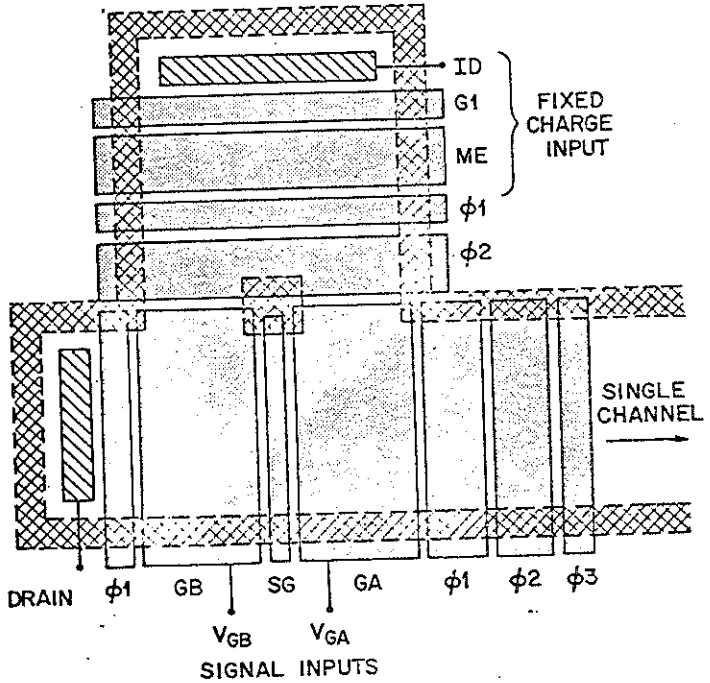
A new charge input scheme for charge-coupled devices is described. Charge packets of a fixed size are produced in each clock cycle. Each charge packet is subsequently split into two parts under two input gates. The difference between the two resulting fractional charge packets is a linear function of the potential difference between the two signal input gates. This input scheme is particularly suitable for use with differential charge-coupled delay lines since the charge representation of the input signal and its complement are produced in a highly symmetrical manner. The principle may also be used for splitting charge packets in any required ratio for more general application.



Conceptual plan view of symmetrical differential input structure for differential charge transfer channels.



...ss section through the input gates GA and GB ...d th...ough the separation gate SG. Potential ...ofiles and charge distribution are shown for ... the balanced case, b) an unbalanced case and ... saturation.



Use of the differential input structure as a charge input for a single charge transfer channel.

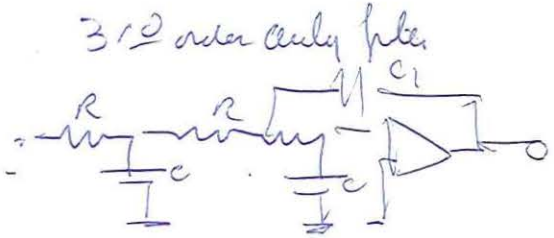
ANTIALIASING INPUTS FOR CHARGE COUPLED DEVICES

Carlo H. Séquin*

ABSTRACT

An input scheme for analog charge coupled signal processing devices has been developed that acts as a prefilter to suppress the aliasing frequencies produced by the sampled data nature of the CCD. Each charge packet injected into the CCD is a sum of several weighted subsamples taken at a multiple of the CCD clock rate. Various approaches that differ in their rates of oversampling and in their time periods over which subsamples are combined have been compared with respect to their usefulness to produce a sharp cutoff prefilter. A particular implementation using only a factor of two oversampling but an averaging period that extends over two CCD clock periods results in a good prefilter characteristic and has been applied to a charge-coupled split-electrode transversal filter. Different implementations of the basic scheme and layout considerations are disucssed.

* C.H. Séquin is with Bell Telephone Laboratories, Murray Hill, N.J. 07974. He is currently on leave of absence with the Department of Electrical Engineering and Computer Sciences, University of California, Berkeley, Ca. 94720.



ANTIALIASING INPUTS FOR CHARGE COUPLED DEVICES

Carlo H. Séquin

INTRODUCTION

Charge coupled signal processing devices are discrete-time sampled-data structures and thus subject to the effects of the repetition of the signal spectrum at the sampling frequency. Normally the sampling process occurs inherently in the input stage of the CCD and thus happens at the operating clock rate (element rate) f_c of the device. Any input signal frequency $f_s = \pm f_o + nf_c$, where $n \cdot f_c$ is an integer multiple of the clock frequency, will produce the same response inside the charge transfer channel as the frequency f_o lying in the fundamental branch of the spectrum between 0 and $0.5f_c$. Thus a prefiltering operation that limits the input signal spectrum to half the element rate is normally required before the continuous input signal can be broken up into separate charge packets without producing aliasing frequencies.

For low-pass sampled-data filters with a passband edge f_p the prefilter can gradually roll off from the frequency f_p to the frequency $f_c - f_p$ where it must have the desired rejection. Thus the higher the clock rate the sampled-data main filter, the easier the task of the prefilter. On the other hand, the order of a transversal implementation of the main filter increases with higher clock rates and the fabrication of the filter becomes more difficult and more expensive.

These tradeoffs are illustrated in Figure 1 using the example of a low-pass filter for speech applications with a passband from 0 to 3kHz and

a stopband starting at 4kHz. Because of the Nyquist theorem, the lowest element rate at which the main filter could be implemented would be 8kHz; this, however, would require a prefilter with an even sharper transition between passband and stopband than the main filter itself. As the clock rate of the main filter is increased to 32kHz and 128kHz, the prefilter could be implemented with a second or third order active filter and with a simple RC circuit, respectively. At the same time the main filter length has grown to about 50 taps for 32kHz and to about four times this size at 128kHz. The first solution is a good compromise, whereas the amount of silicon used for the latter would be hard to justify.

TRADITIONAL PREFILTER IMPLEMENTATIONS

Passive LC filters or active RC networks could readily be used to implement the necessary low-pass prefilter. Only the latter approach is compatible with the silicon integrated circuit technology. Even then the cost of the prefilter may exceed that of the CCD mainfilter, when external or laser trimmed RC components are required to yield the desired accuracy. It is preferable to choose a prefilter that can be realized in a technology compatible with CCD processing, so that the prefilter can be included on the same chip to form a self-contained signal processing unit. A second feature, which may be desirable for on-the-shelf devices to be used in applications requiring different or variable clock rates, is to use a prefilter with a cutoff frequency that scales with the operating clock rate of the CCD. This requirement obviously implies a discrete-time approach, and thus basically a prefilter operating at a higher sampling rate. Such a prefilter does not overcome the need for a preceding analog, continuous-time filter, but the requirements for such a filter can be relaxed in proportion to the amount by which the sampling

rate is increased. For higher effective sampling rates the roll-off of the analog prefilter can be very gradual, and it is then possible to implement that filter with a small number of external low-precision elements; often a single capacitor will be sufficient.

The sampled-data prefilter can be implemented as a transversal filter of relatively low order. In the context of the example illustrated in Figure 1, a prefilter is required that rolls off between 4 and 28kHz for the practical case where the main filter operates at an element rate of 32kHz. Such a prefilter, with a rejection of 40dB between 28 and 36kHz and with a passband ripple of less than 1% could be implemented with a transversal filter having only 6 taps and operating at 64kHz, or 13 taps when the prefilter sampling rate is increased to 128kHz.

However, the implementation of such a transversal prefilter with a split-electrode CCD would require the complete overhead of charge injection and detection circuitry, countdown logic, clock drivers and auxiliary gating pulses. The duplication of these peripheral circuits for the prefilter requires an area of silicon that is out of proportion to its function. As will be shown in this paper, the transversal prefiltering can be done entirely in the charge domain and the required circuitry is rather simple.

PREFILTERING BY OVERSAMPLING AND SUMMING

The high frequency components in the input signal can be attenuated if the incoming continuous signal is averaged over the clock period rather than sampled with a delta function (Figure 2a). It has been discovered that the potential equilibration or "fill and spill" input produces such a filtering function for small signal amplitudes (1). The discrete-time equivalent which is applicable to signal amplitudes of any

size would be to take multiple samples during each clock period. These samples are then summed or averaged to obtain one sample which is injected into the charge transfer channel (Figure 2b). Charge-coupled devices are particularly suitable for such an oversampling approach since the summing of the subsamples can be achieved directly in one of the potential wells of the CCD. The prefilter can then be integrated into the input structure of the CCD (2,3). Furthermore, if metering electrodes of different sizes are used to generate different subsamples, these subsamples can be assigned different weights, and thus one obtains additional flexibility in tailoring the roll-off function of the prefilter (Figure 2c).

Figure 2d illustrates that prefiltering achieved by oversampling with suitable weighting coefficients and subsequent summing corresponds to transversal filtering with a prefilter operating at the oversampling rate followed by a subsequent decimation of the produced output signal samples to reduce the data rate to the clock rate of the main filter. All of these prefiltering operations can be performed entirely in the charge domain and thus produce charge packets that can be injected directly into the main CCD filter.

Before we discuss actual implementations of such input structures, we will give an overview over the prefilter functions produced for different sampling rates, averaging periods, and weighting coefficients to develop a better understanding for the main tradeoffs.

COMPARISON OF VARIOUS PREFILTER FUNCTIONS

If the prefilter simply averages the input signal over the full CCD clock period T, corresponding to the inverse of the actual element rate, the resulting frequency response is equal to $\sin(\pi fT)/(\pi fT)$ as displayed in Figure 3a. The discrete-time implementation of this function obtained

by sampling at a higher rate, S, and summing the individual subsamples taken during one clock period results in the responses shown in Figure 3b and 3c for the cases of two and four delta-function samples per clock period, respectively. All these prefilters have a rather slow roll-off, and even though they have a true zero at the CCD clock frequency, they have an effective stopband region around that area that is too narrow for practical purposes.

A steeper roll-off can be achieved if the averaging period P is extended. Figure 3d shows the result of a continuous averaging process over the extended period of 2T. Figures 3e and 3f represent the discrete-time implementation, taking four and eight samples at the same rates as previously used for Figures 3b and 3c, respectively. Even though the roll-off is now steeper, the effective stopband region has not become much wider. An efficient way to widen this stopband is to place a multiple zero at the CCD clock frequency. This can be done by assigning the respective weights of 1/8, 3/8, 3/8 and 1/8 to the four samples taken during an averaging period of 2T. The prefilter response becomes $(\cos \pi fT)^3$ and is displayed in Figure 3g. Since these four weighted subsamples can be regarded as the impulse response of a transversal filter, a computer program based on the Remez algorithm can be used to optimize these weights so that the errors in the passband and in the stopband are minimized (4). Referring to the example discussed in the introduction, we define the passband from 0 to 4kHz and the stopband from 28 to 36kHz for a CCD clock frequency of 32kHz. The computer optimization yields respective weights of 0.328 and 0.115 and a "ripple" (error) of 2.7% in both bands (Figure 3h). The corresponding numbers for the previous filter function (Figure 3g), i.e., the deviations from

the desired values at 4kHz and 28kHz, are 5.7% and 0.7%, respectively. Thus the special weighting coefficients that yield a triple zero at the CCD clock frequency give more rejection in the stopband at the expense of a stronger droop in the passband.

Figures 3i and 3j have both been generated with a sampling rate of 128kHz but average over one clock period (four subsamples) and two clock periods (eight subsamples) respectively. The respective optimized errors obtained from the Remez algorithm are 12.4% and 2.3%. Considering the narrow effective stopband and the correspondingly large error of the prefilter 3i, it becomes evident that for a fixed number of samples (four) the extension of the averaging period to two clock cycles of the CCD (Figures 3g or 3h) is more important than an increase of the sampling rate from 64kHz to 128kHz (Figure 2i).

The baseband of some important cases of the filter responses displayed in Figure 3 have been superimposed on a normalized scale in Figure 4 for easier comparison. It can be seen that the stopband rejection of prefilters e and c which use unweighted samples are really poor compared to g and j using suitable weights. Figure 4 further shows that the stopband performance of curve g with the artificial third order zero at f_c surpasses even the "optimized" response of prefilter j which uses twice as many samples.

A PARTICULAR IMPLEMENTATION

The choice of a specific approach not only depends on the application and the prefiltering requirements, but also upon the difficulty or expense in terms of additional silicon area on the CCD-chip that is used for its implementation. The particular device for which a prefilter had to be implemented is a low-pass transversal filter corresponding to the

description in the introduction. This device (5), which is described elsewhere in this issue, is operated in a four-phase manner with two dc clock phases. All timing pulses are derived from a master clock running at four times the element rate of the CCD. One of the boundary conditions for the choice of the prefilter was that the on-chip countdown logic should not be complicated unnecessarily and no higher multiple of the master clock should be used. A prefilter, according to approach g or h (Figure 3), using a sampling rate of 64kHz combined with an extended averaging period of 2T, seemed easy to implement and to offer adequate prefilter performance.

The weighting coefficients of prefilter g were preferred because they give the better stopband rejection, and the droop of the frequency response in the passband between 0 and 4kHz can readily be compensated by adjusting the tap weights in the transversal charge-coupled main filter to give a suitable boost of the response towards the passband edge.

Figure 5 is a schematic representation of the operation of the prefilter. Since the averaging period P extends over two clock cycles T, but a charge packet has to be injected into the main CCD on every clock cycle, an interleaved approach of the charge packet generation has to be used. Weighted subsamples are added in two separate summing wells which then alternately inject the integrated samples into the charge transfer channel.

This particular CCD filter employs a "voltage input" in which the input signal is applied to the input diode. A small input gate acts as a sampling gate to slice off a charge packet under the metering electrode that produces the same interface potential as that on the input

diode at the moment when the gate turns off. Referring to Figure 5a, samples are taken in the metering wells in time slots 1, 3, 5, 7 of the master clock. These samples are transferred to the summing wells in time slots 2, 4, 6, 8, and are alternately injected from there into the CCD at the beginning of each CCD clock period.

In principle, only two separate metering electrodes with sizes 1/8 and 3/8 of a full size electrode in the CCD have to be provided for the implementation of the prefilter function shown in Figure 3g. However, to obtain a layout with no crossings between the transfer paths of the charge packets representing the subsamples and with fewer crossovers and contact windows among the address leads that perform the switching between the metering and the summing wells, an approach with two separate metering electrodes for both summing electrodes has been adopted. A functional block diagram of this input structure is shown in Figure 5b. The metering wells (MW) and the summing wells (ΣW) are shown as simple rectangles and the transfer gates as simple switches. The numbers below each switch indicate the time slots during which a charge packet is transferred.

The actual layout of the antialiasing CCD input is shown schematically in Figure 6. The dotted areas indicate the MOS electrodes which in reality are implemented by two layers of overlapping polysilicon electrodes, with MW and ΣW in the first level. The blank stripes SG, IGX, and IGY are aluminum conductors that access the corresponding gates through contact windows (X). The outline of the transfer areas and the input diode (ID) is marked by a dashed line. All four metering wells are formed under the same electrode (ME) and the respective weighting coefficients 1/8, 3/8, 3/8, 1/8 are determined by the width of the

transfer channels underneath. A photograph of the actual device input is presented in Figure 7.

RESULTS

The described antialiasing input has been used in a self-contained 55-tap split-electrode low-pass filter (5). In addition to the charge transfer elements, this chip carries all peripheral logic circuitry and pulse drivers to operate the CCD and its input-output circuitry. It carries several n-MOS operational amplifiers and other analog circuit elements for charge detection and signal reconstruction. The devices have been fabricated using a 6-mask double-level polysilicon process with self-aligned source and drain diffusions. For comparison, devices with and without the antialiasing input have been built on the same wafer. Figure 8 compares the frequency responses of the two devices. In the device with the normal voltage input the passband (0-3.2kHz) is repeated above and below each multiple of the clock frequency of 32kHz. All repetitions of this band are attenuated by a factor $(\sin \pi fT)/(\pi fT)$. This factor, which produces true zeros at all multiples of the clock frequency, originates from the sample-and-hold signal reconstruction circuit. The antialiasing input, on the other hand, suppresses all repetitions of the passband associated with odd multiples of the clock frequency.

An expanded view of the fundamental branch of the overall frequency response is presented in Figure 9. It can be seen that the response of the main filter can be suitably predistorted to compensate for the combined droop due to the prefilter and the sample-and-hold circuit, so that the overall response throughout the passband and up to the Nyquist limit (16kHz) in the stopband is rather flat. The observed ripples in the two bands correspond closely to the predicted frequency response of

the ideal 55-tap filter with suitably rounded coefficients.

DISCUSSION

The layout of the actual input structure is very compact, and compared to the length of the main CCD only a small additional length is required to accommodate the summing wells and the additional conductors and contacts for the multitude of input gates (Figure 6). The overall width of the input structure is only slightly larger than the CCD channel, since the sum of all weighting coefficients adds up to unity, and thus the sum of all partial channel widths under the metering electrode (ME) is equal to the CCD channel width.

The additional logic circuitry required to drive the prefilter consists of a flipflop, used to provide signals at half the CCD clock rate for the interleaved summing and injection into the CCD, plus some NAND and NOR gates to decode the special gating functions IGX, IGY, ΣA, ΣB, DA, and DB.

For this particular device it may be desirable to raise the oversampling rate to $4f_c$ (128kHz) so that the unavoidable analog prefilter can be realized with a single RC circuit. Even though this complicates the layout of the input end of the device, since metering wells of four different sizes are now required, necessary gating signals can still be derived from the master clock of $4f_c$ without needing any multiples of this frequency. Samples are now taken in all 8 time slots of Figure 5. However, regardless of the timing details of a specific implementation, a problem may arise in the largest metering well which must take two samples and transfer them to a summing well in two subsequent time slots. Two separate implementations of this metering well may have to be used in order to avoid a race condition between the loading of one sample and

the discharge of the previous charge packet.

Because of this difficulty the simple approach sampling at 64kHz has been taken.

OTHER IMPLEMENTATIONS

For prefilter functions generated by the combination of more than four subsamples, and particularly if the averaging process stretches over more than two clock periods T which would require more than two summing wells, the layout of the input structure can get complicated. It is then more difficult to avoid crossings of the transfer paths of the subsamples and to provide access leads from the logic to the various transfer gates. Also, the decoding of the various gating pulses may become more difficult. It may then be advantageous to combine the charge packets in the moving potential wells of the CCD itself and to use the different phases of the CCD to do the oversampling operation. This leads to the transposed form of a charge coupled FIR (finite impulse response) prefilter shown in Figure 10. This circuit topology corresponds to a parallel in – serial out transversal filter (6) or to an arrangement of parallel delay lines of different lengths proposed by Berger and Coutures (2).

In principle a prefilter of this form could combine any number of subsamples and the averaging process could stretch over many clock periods without any topological difficulties in the basic layout. This approach is best suited when the main CCD is operated with four active clock phases, each T/4 apart. An oversampling rate of $4f_c$ can then be obtained in a natural manner. Still, there are some nontrivial layout problems to be solved. All the metering wells for all four phases should be implemented under electrodes that lie in the same level of polysilicon; and access leads to all the transfer electrodes and input gates in the input

section must be provided.

Following an opposite philosophy one may want to separate the metering process completely from the charge transfer channel. The capacitors that convert the input voltage with a certain weighting coefficient into a corresponding charge packet could be implemented either as MOS structures with a heavily doped counter electrode in the substrate or as double-level polysilicon structures (Figure 11). These approaches have the advantage that the capacitors at the output of the CCD that perform the inverse conversion from a charge packet to a voltage signal can be implemented with the same structure, so that the overall gain of the device then depends only on a ratio of two areas. Furthermore, better linearity may be expected, since the voltage dependence of capacitors using majority carriers is smaller than that of an MOS inversion capacitor. Charge is transferred from the "top" plate of the capacitor (Figure 11) to the CCD when a voltage step $V_{in} - V_{zero}$ is applied to the bottom plate (7). A proportional amount of charge is then pushed across a threshold barrier established under an MOS gate into a summing well at the input of the CCD. The same capacitor could act as the metering device for several summing wells if the MOS transfer gates are suitably pulsed. The signal paths can readily be crossed since the charge on these capacitors consists of majority carrier, and thus the topological layout problems are alleviated.

In this latter approach it may be desirable to use as few precision capacitors as possible and to multiplex their use to the highest degree. Therefore, the number of different weighting coefficients should be minimized. Figure 12 compares the two prefilter functions corresponding to Figure 3g and 3j with a compromise approach using also 8 subsamples

but only 2 different well sizes. For all three cases the filter responses at the passband edge and first stopband edge are also given.

It can be seen that it is possible to construct a prefilter using only two capacitors or well sizes, which gives adequate rejection of the first three repetitions of the passband.

CONCLUSION

An approach to on-chip prefiltering for charge-coupled signal processing devices has been demonstrated which represents a good compromise between on-chip circuit complexity and prefilter performance. Several suitably weighted charge subsamples are combined and then injected into the main CCD. Different prefilter responses can be realized by different oversampling rates, averaging periods, and weighting coefficients. For a particular application a prefilter function should be selected which reduces the necessary analog prefiltering function to a simple low precision off-chip RC circuit. This circuit can readily be adjusted when the operating clock frequency of the CCD is changed or it can be designed with suitable margins to cover a range of clock frequencies. The on-chip prefilter function generated by oversampling with suitably weighted subsamples scales directly with the clock frequency.

A particular scheme that uses four subsamples with respective weights 1/8, 3/8, 3/8, 1/8, taken at twice the element rate of the CCD has been incorporated in a self-contained 55-tap split-electrode low-pass filter. The suppression of the aliasing components meets the theoretical expectations.

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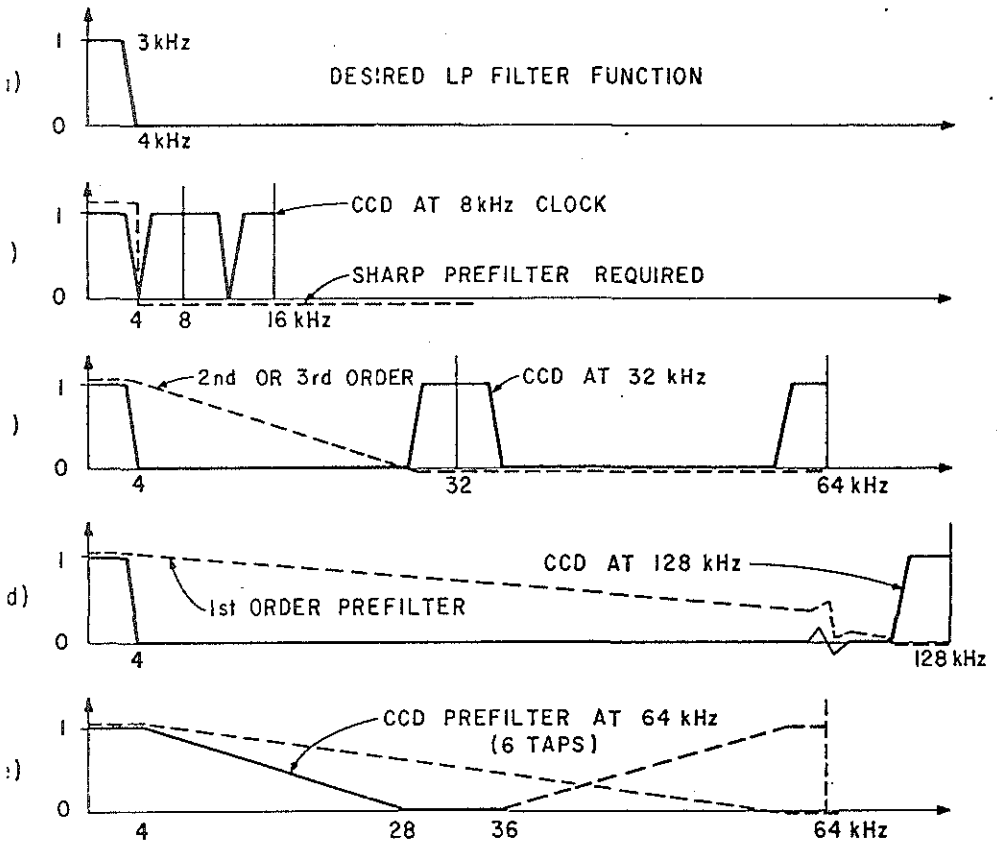


Fig. 1 Comparison of the prefilter requirements for various operating clock rates of the main CCD low-pass filter. (a) Desired overall filter function, (b) Lowest clock rate of 8kHz requiring sharp cutoff prefilter, (c) Practical clock rate of 32kHz with 2nd or 3rd order active prefilter, (d) High clock rate of 128kHz with simple RC prefilter, (e) 6th order transversal prefilter running at 64kHz.

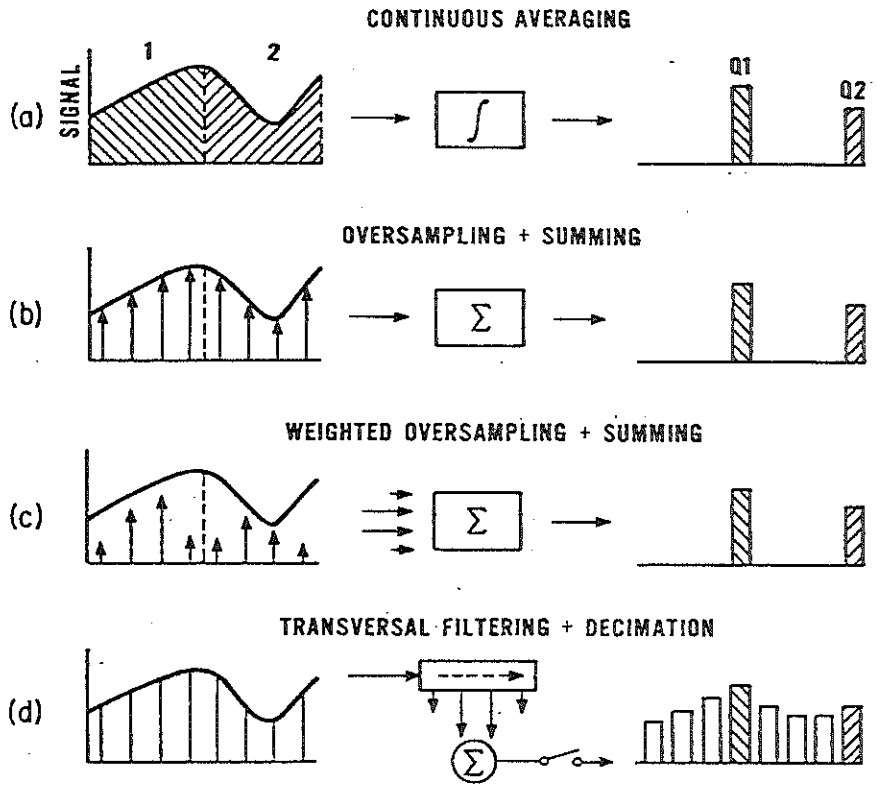


Fig. 2 Prefiltering by various averaging techniques. (a) Continuous averaging by integration, (b) Discrete-time equivalent using oversampling and summing, (c) Weighted oversampling and summing for better prefilter characteristics, (d) Equivalent operation using transversal filtering and decimation.

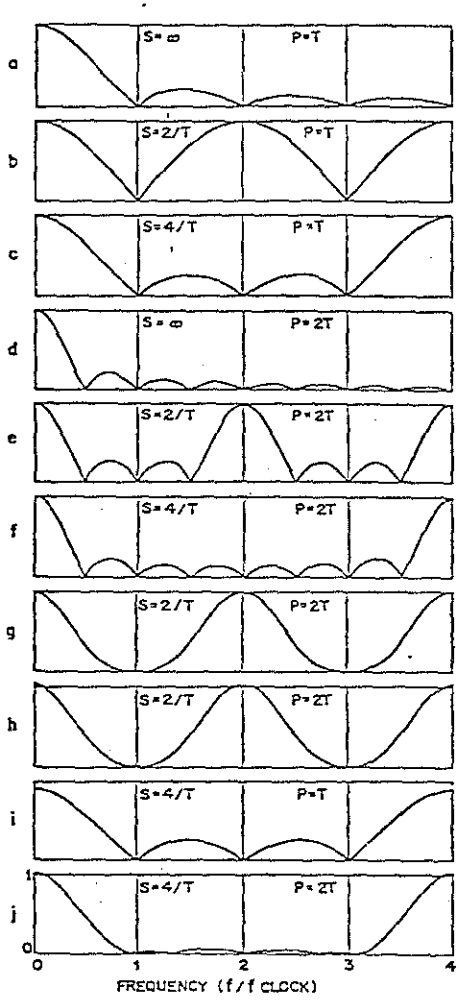


Fig. 3 Comparison of prefilter functions produced by: (a) Continuous averaging over clock period T, (b) 2 equal samples at $2f_c$, (c) 4 equal samples at $4f_c$, (d) Continuous averaging over 2T, (e) 4 equal samples at $2f_c$, (f) 8 equal samples at $4f_c$, (g) 4 weighted samples at $2f_c$, (h) 4 optimized samples at $2f_c$, (i) 4 optimized samples at $4f_c$, (j) 8 optimized samples at $4f_c$.

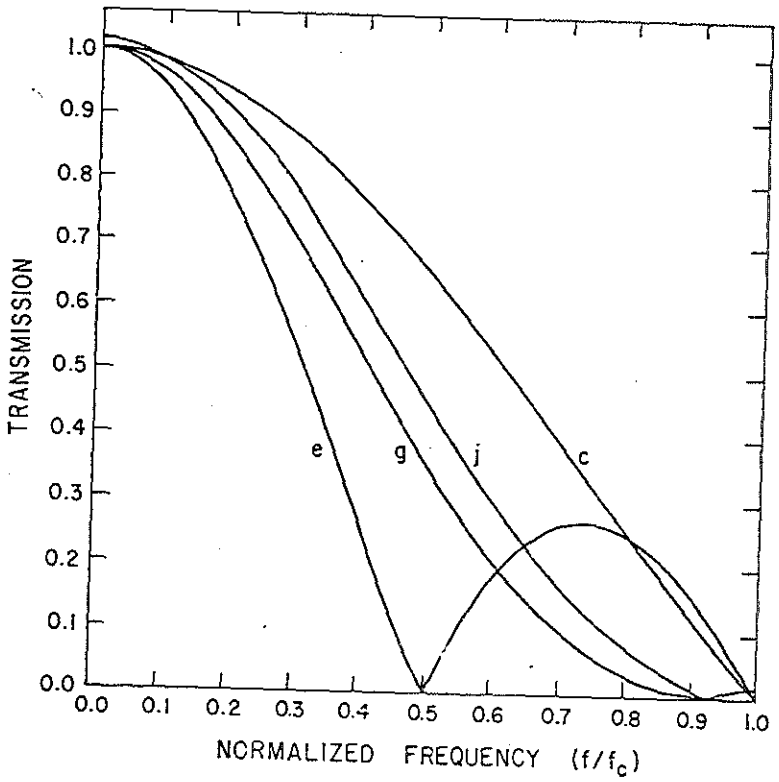


Fig. 4 Superimposed baseband branches of some of the prefilter responses shown in Figure 3. Curve g is the function actually selected for implementation because of its good stopband rejection.

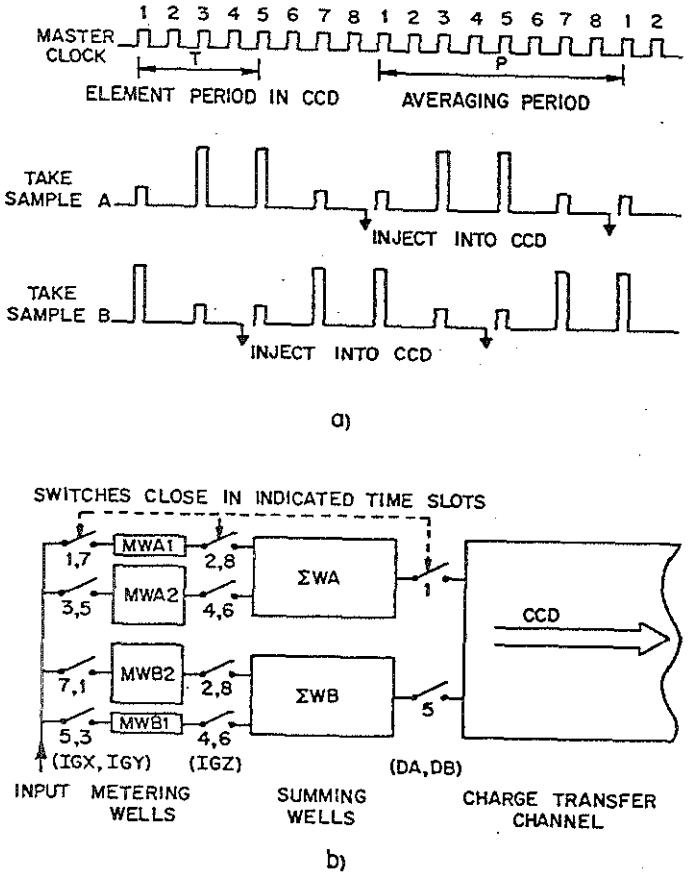


Fig. 5 Basic operation of the prefilter according to approach g. (a) Timing of master clock and subsamples, (b) Schematic structure of the prefilter. The numbers below the switches indicate the time slots during which charge packets are transferred to the metering wells (MW), to the summing wells (ΣW) and into the CCD.

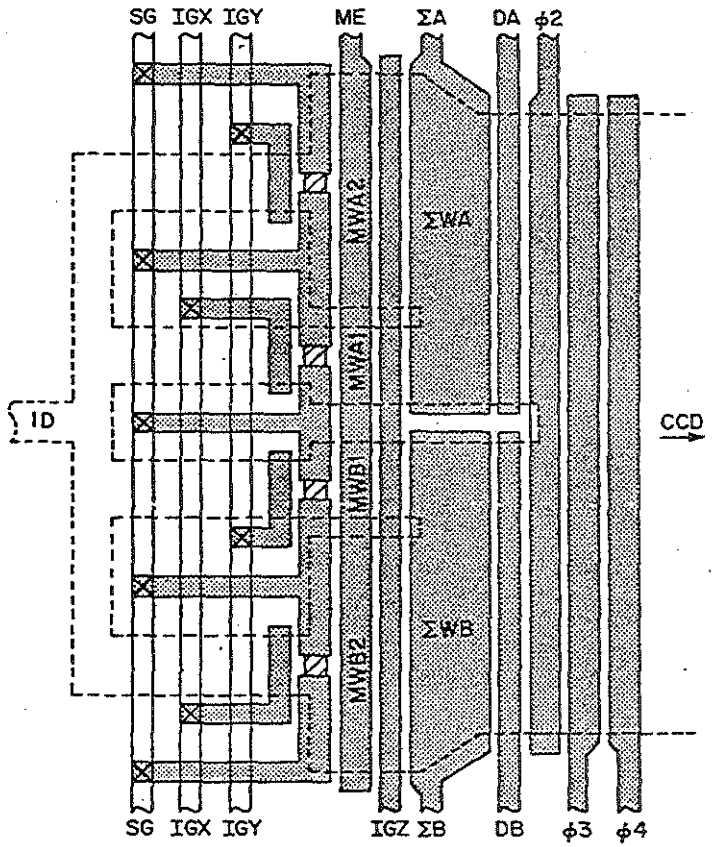


Fig. 6 Schematic layout of antialiasing CCD inout using a factor of two oversampling and an averaging period of 2T. Shown are input diode (ID), input gates (IGX and IGY), metering wells (MWA1, MWA2, MWB1 and MWB2), summing gate (IGZ), summing wells (ΣWA and ΣWB), and gates for discharge of packet into CCD (DA and DB). Weighting coefficients are 1/8, 3/8, 3/8, 1/8.

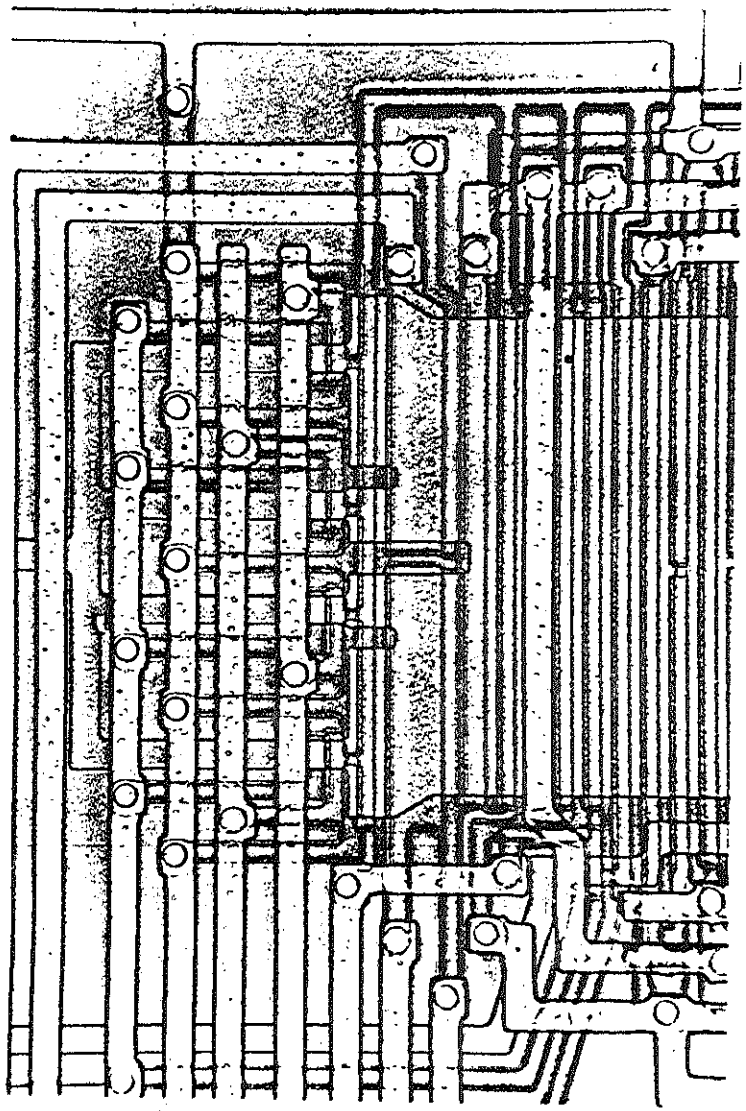


Fig. 7 Photograph of the actual device input corresponding to the schematic layout of Figure 6. The first split electrode of the main CCD filter is visible on the right hand edge.

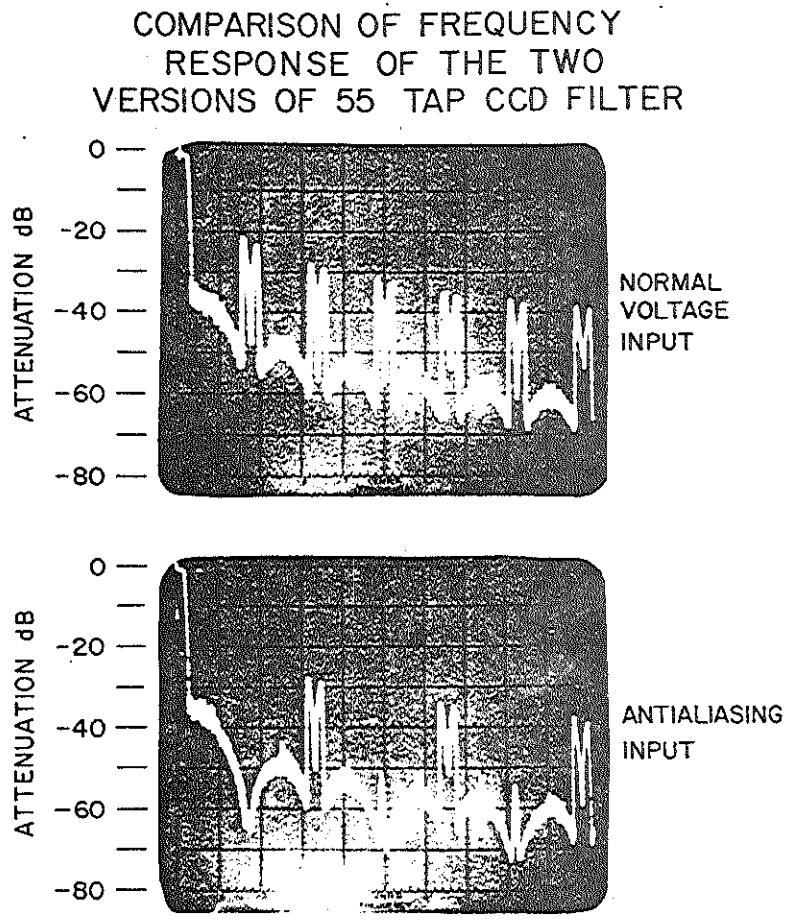
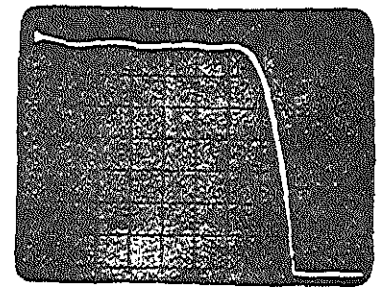
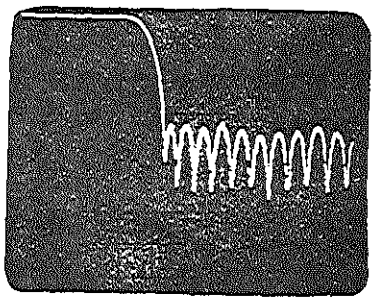


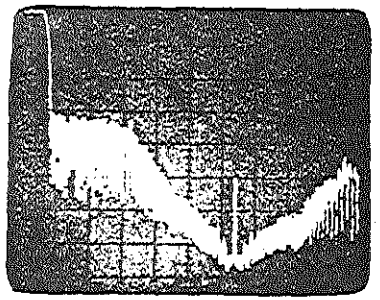
Fig. 8 Comparison of the frequency responses of a low-pass filter with a normal voltage input and of a device with an antialiasing input that suppresses the reproduction of the passband at all odd multiples of the clock frequency. Clock frequency is 32kHz, horizontal scale is 20kHz/div.



(a)



(b)



(c)

Fig. 9 Expanded view of the fundamental branch of the frequency response of the low-pass filter with antialiasing input on 3 different scales: (a) 500Hz/div., 2dB/div.; (b) 1kHz/div., 10dB/div.; (c) 5kHz/div., 10dB/div.

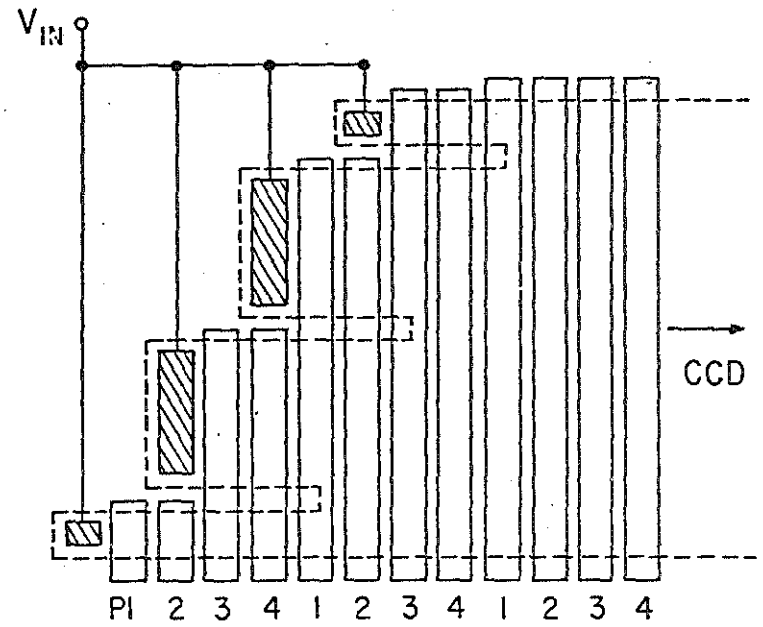


Fig. 10 Schematic layout of an antialiasing CCD input implemented with a parallel in - serial out transversal filter.

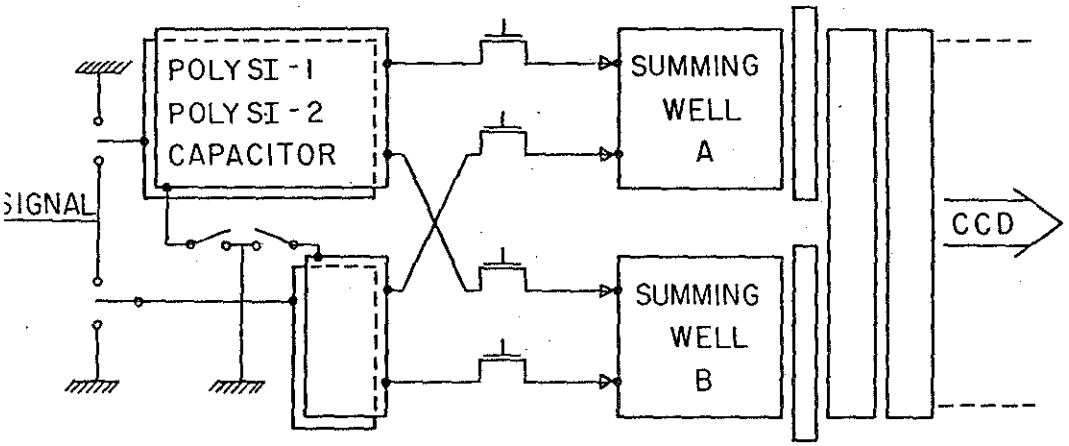


Fig. 11 Antialiasing prefilter using weighted, interleaved oversampling implemented with double level polysilicon capacitors.

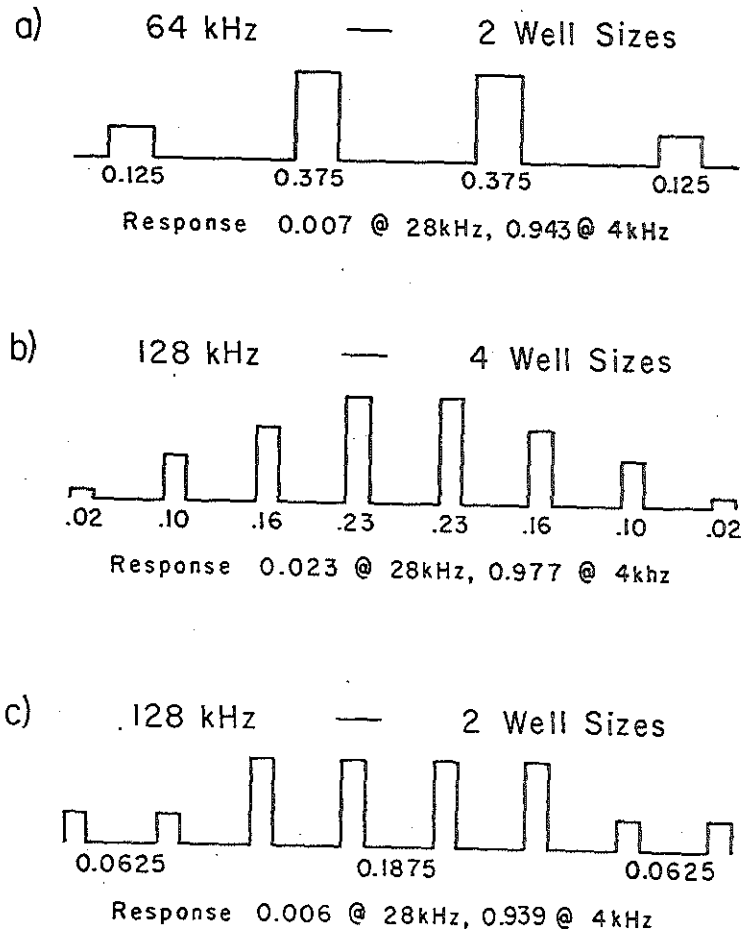


Fig. 12 Comparison of the responses at the passband edge (4kHz) and first stopband edge (28kHz) for 3 prefilters with different impulse responses: (a) 4 samples at $2f_c$, (b) 8 samples at $4f_c$, (c) 8 samples at $4f_c$, but using only two different well sizes.

SELF-CONTAINED CHARGE-COUPLED SPLIT-ELECTRODE FILTERS USING NOVEL SENSING TECHNIQUE

by

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Bell Laboratories
Murray Hill, New Jersey 07974

ABSTRACT

Self-contained charge-coupled split-electrode filters with 55 taps have been built with a double-level polysilicon n-MOS process. Operating at a sample rate of 32kHz, these devices provide a low-pass filter function with a passband from 0 to 3.2kHz and a stopband above 4kHz. The image charge on the sense electrodes is detected with a novel sensing circuit employing two on-chip operational amplifiers, one of which suppresses the common mode signal on the two sense buses while the other one integrates the difference signal. In addition, the chips carry antialiasing pre-filters, a sample-and-hold circuit to restore the output signal, and all the necessary peripheral logic and biasing circuitry so that the devices can be operated from a single master clock and two power supplies of +12V and -5V respectively.

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INTRODUCTION

The charge-transfer split-electrode structure 1) 2) makes possible an elegant and compact realization of transversal filters with fixed tap weights which can be calculated using efficient and convenient algorithms. 3) Experimental devices with up to 800 taps 4) have been demonstrated.

Normally a substantial amount of support circuitry is required to operate the basic charge transfer structure with its associated input section and charge sensing system. An attempt has been made to construct a practical device with complete on-chip support circuitry, so that it can be operated from a single clock and only two supply voltages. The next section of this paper presents the organization of this device and discusses some general design considerations. Section 3 discusses the special sensing technique employed in this device which uses an operational amplifier to suppress the common mode signal on the two sense buses. Section 4 briefly reviews a technique using oversampling and weighted summing to provide an anti-aliasing prefilter 5) and discusses the overall filter response. Experimental results and possible improvements of this device are discussed in the last sections of this paper.

II. Chip Organization and Overall Design Considerations

A block diagram of the self-contained low-pass filter chip is shown in Figure 1. The top row of blocks constitutes the analog signal path, which is controlled by the circuit shown in the lower row of blocks. Along the signal path the incoming signal is level shifted to the proper potential required by the "voltage input" used for the CCD main filter. Half the number of devices on each wafer are provided with a more complicated, anti-aliasing input which operates by oversampling and weighted summing 5). The main filtering function is performed in the split-electrode CCD with 55 taps. The charge sensing circuit converts the difference in image charge on the two sense buses into a corresponding voltage signal which is then put through a sample-and-hold circuit to reconstruct a continuous output signal. The control circuit performs a divide-by-four countdown from the master clock input to provide the timing pulses for the 4-phase CCD filter. These signals are properly amplified and shaped to drive the transfer electrodes of the CCD. The logic circuitry also controls the gates in the CCD input section and operates the reset and clamp switches in the output circuitry. In addition, synchronization circuits are provided so that several devices can be cascaded or operated in parallel. Each device can either act as a master for other devices, or can itself be locked to the master phase dictated by another device. The same synchronization circuits have also been used in a self-contained delay line 6). A picture of an actual chip, measuring 1.9 × 5.9 mm., is presented in Figure 2. The devices were fabricated on lightly

doped p-type substrates ($5 \times 10^{14} cm^{-3}$) using the same 6-mask process that had been developed for the above mentioned charge coupled delay lines 6). A selective oxidation with a self-aligned channel stop implant first outlines the active charge transfer areas and all MOSFETS. Two overlapping and thermally oxidized levels of polysilicon provide the transfer electrodes and two different types of MOSFET gate. A selective ion implant introduced before the deposition of the second level of polysilicon provides MOSFET's with a higher threshold voltage (1.1V without backgate bias) which are more suitable for use in the peripheral logic circuits. All source and drain diodes are formed in a self-aligned manner after the patterning of the second level of polysilicon without the need for a masking operation.

The two-level electrode structure leads naturally to a 4-phase approach in which all split sense electrodes can be placed in the same level. A highly symmetrical layout and carefully matched parasitic capacitances have been employed in order to minimize differential pickup signals. A small channel parallel to the main filter, dirven by the same electrodes, and carrying a constant signal corresponding to half-full buckets has been incorporated to balance the difference of the thin oxide areas under the two sense electrode systems 7). Otherwise in those filters with a dc response the bias charge will generate an output dc signal.

The sense electrodes are held at a fixed dc potential (V_{SE}), which is close to the middle of the range of active potentials

that drive the CCD electrodes, in order to obtain low-signal distortion and large signal handling capability. To keep the sense electrodes at that potential at all times rather than clocking them simplifies the sensing circuitry. The sense amplifiers can be permanently connected to the sense buses and there is no danger that they are driven into a condition from where they could only slowly recover. In order to reduce the amount of pickup on the sense electrodes, they are preceded by another dc electrode. This shield gate (SG) is held at a voltage that is one maximum signal swing (4V) lower than V_{SE}. So out of the 4 electrodes per call, only two (P1 and P2) are actively pulsed. When both, P1 and P2, turn on, the charge is drained from underneath the split sense electrodes towards P1 because the barrier under SG prevents the packets from spilling backwards. As P1 turns off, P2 holds all the charge packets. Finally, when P2 turns off, they are pushed over the barrier under SG into the next sensing wells. Thus, the shield gate (SG) acts to prevent a difference signal due to any differences in overlap capacitance between the P2 and the sense rails. There is no need to prevent the pickup resulting from the turn-on of P1 since at that time the output signal has already been sampled.

The gap in the split electrodes can either be blocked with a thick oxide region or it can be bridged with a small self-aligned diode produced during the source and drain diffusion. The first approach is not recommended in the context of the static sensing well preceded by a shield gate. During transfer of the charge packets into the sensing well each charge packet would be split in a dynamic manner as it is pushed over the barrier under SG.

Nonuniformities in this barrier potential would play a dominant role in determining the ratio by which the packets are split. Large and unpredictable tap weight errors might result. Thus, it is mandatory that the charges can equilibrate under the sense electrodes which requires a conductive connection between the two half-wells.

III. Sensing Circuitry

In the simplest implementation the two split-electrode systems act as floating-gate sensors. The major capacitances associated with one sense electrode are shown in Figure 3, which is a cross-section through the CCD channel. C_e represents the fixed oxide capacitance between the signal charge at the Si-SiO_2 interface and the sense electrode. C_d is the nonlinearly varying depletion capacitance between signal charge and substrate. C_p is the parasitic stray capacitance of the sense electrode. However, the effect of the latter can be neglected if the sense electrodes are held at a fixed dc potential V_{SE}, which can be achieved for instance, with an operational amplifier and proper feedback as shown in Figure 3. In this case the output voltage developed across the feedback capacitor C_f then becomes a linear function of the interface potential Ψ_s under the sense electrode.

In order to obtain a linear overall transfer function, a input structure is required that relates the interface potential Ψ_s, rather than the charge Q_s contained in the packet, in a linear manner to the input voltage signal. This condition is met by the voltage input shown schematically in Figure 4. The key elements are the input diode, the input gate and the metering well (MW). The input signal is applied to the input diode and thereby defines

the interface potential along the whole input section, including MW, as long as Φ_{IG} is high. When the input gate turns off, an amount of charge corresponding to that interface potential is isolated in MW and subsequently transferred through the CCD. If the wells under the sensing electrodes SE are made electrically identical to the metering well MW at the input, then the charge packet will reproduce, at every sensing node, the original interface potential established by the input signal. Thus, the sensing wells must have a layout identical to that of the MW and the electrodes above the two wells have to be held at the same potential V_{SE}. In order to match the metering well MW as closely as possible to the geometry of the sensing wells, it too was preceded by a shield gate SG. However, charge from the input diode has to equilibrate with the packet under MW and a slot in SG has to be provided for this purpose. This slot is automatically bridge by a self-aligned diode. This turns out to be fortunate since the area of this diode can be made to match that of the diode in the sensing well. Thus, the two well types can indeed be made almost identical.

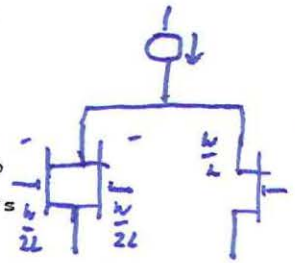
In principle the sensing electrodes could be completely floating were it not for leakage currents. The reset switch Φ_R is used to reset the sense electrodes to the proper potential once every clock cycle. It can be of minimum dimension if operated at the right time since the sense electrodes and the feedback capacitor C_p will automatically discharge to their original values when the charge packets are removed from underneath SE.

In a charge-coupled split-electrode filter the output signal is derived from the difference of image charge on the two sense electrodes. Baertsch et al. 7) have studied the approach

shown in Figure 5a using only a single off-chip operational amplifier. Although the feedback around this amplifier restores electrodes SE^- to the same potential as SE^+, the two sense electrode buses will jointly float to a potential that depends on the total amount of charge under all the SE^+ half-electrodes. Because of this interaction, crosstalk between subsequent packets takes place. As discussed previously, these nonlinearities can be avoided if both sense buses remain at a fixed potential during the sensing process. One way to achieve this is shown in Figure 5b. The two sense electrode systems are individually clamped to a virtual dc reference voltage V_{SE} with two operational amplifiers used in the charge integrating mode. A third amplifier forms the difference between the output voltages of the first two amplifiers. This approach has the disadvantage that the desired output signal is derived as the often small difference between two relatively large signals originating from the two clamping amplifiers. Furthermore, the noise of the two clamp amplifiers is added incoherently to the output signal.

It is preferable to integrate the difference signal directly in a single amplfier where the feedback capacitor can be adjusted to obtain a desired device gain, or to match the maximum expected difference signal to the output swing of the operational amplifier. These requirements are met in a novel sensing circuit using only two operational amplifiers (Figure 6). Amplifier A_D senses the difference in image charge on the two buses in the same manner as the amplfier in Figure 5a, and produces a corresponding

signal voltage across the MOS feedback capacitor C_D^-. Amplifier A_C has been added to suppress the common mode signal on the two buses. Its output is applied through two identical capacitors (C_C^+, C_C^-) to both sense buses, and it will therefore not affect the difference signal. This amplifier has been provided with two inverting inputs by simply splitting one of the two input MOSFET's of the differential input stage into two equal halves, each with half the channel width of the input transistor of the noninverting input. These two inputs sense the arithmetic mean of the potentials SE^+ and SE^- and restore this mean to the desired sensing potential V_{SE}. Since amplifier A_C simultaneously suppresses the potential difference between SE^+ and SE^-, both sense buses will be restored to V_{SE} after both amplifiers have settled.



This approach has the advantage that the feedback paths around the two amplifiers can have different gains. The feedback capacitors C_D^+, C_D^-, C_C^+ and C_C^- are adjusted so that the respective maximum signals can just be handled by the maximum swing of the amplifier output stages. In this particular device the C_C's are about seven times larger than the C_D's.

The noise of amplifier A_C imposes only common mode signals onto the sense buses and it does therefore not enter the output signal. On the other hand, the noise generated when the two reset switches are opened is uncorrelated and will disturb the output signal. This noise component can be suppressed by using correlated double sampling to clamp the output signal to a desired

reference voltage V_{ZERO} before the actual signal charge is sensed when P2 turns off. In a first approach we tried to implement this function directly in amplifier A_D. For this purpose A_D was ac coupled to the sense buses through capacitors C_0^+ and C_0^-, and the dc restoring MOS switches associated with A_D were used to perform the clamping operation. They were kept turned on until after the reset switches had been turned off and were only opened before the signal charge packets were transferred under the sense electrodes.

Unfortunately, the reset noise associated with the operation of the clamp switches themselves is amplified by the closed loop gain around A_D, which is about 10; and the dominant noise component in the circuit as shown in Figure 6 is due to this operation of the clamp switches. Figure 7 shows the modifications that were introduced in order to suppress that clamp noise. A second double correlation network has been added at the output of A_D consisting of the coupling capacitor C_S and the switch CORL to the reference level V_{ZERO}. All four reset switches associated with the two amplifiers are now operated with the same reset pulse.

This sensing circuitry can be followed by a sample-and-hold circuit to provide a continuous output signal. This circuit consists of a sampling gate, a holding capacitor C_H and amplifier A... The ratio of the capacitors C_S/C_H has been made large enough s... at the signal is only attenuated by about 5%.

The operational amplifiers used on this chip were derived from a circuit developed by Tsividis and Gray 8). The amplifiers are all MOS and operate with power supplies of +12V and -5V for a power consumption of 30mW. The dc gain of the amplifier was

increased to 1400, the unity gain point lowered to 2MHz, and the area reduced to 0.25 mm^2.

Most of the capacitors are realized between poly I and poly II electrodes. However, the feedback capacitors C_D^+ and C_D^- which are the gain determining elements in conjunction with the oxide capacitance of the sense electrodes were implemented as MOS structures in poly I, the same level as the sense electrodes, to compensate for global variations in the oxide thickness. Furthermore, a fingered structure with the same line width as the split electrodes has been used, so that geometry charges due to over-or underetching would compensate to first order. However, these capacitors change their value slightly as a function of applied voltage, and are therefore a source of nonlinearity in the signal.

IV. Overall Filter Function and Anti-Aliasing Input

CCD's are sampled data filters and as such have to satisfy the Nyquist theorem, i.e., the clock rate has to be at least twice the highest signal frequency of interest. In selecting the element-rate of the main filter, a tradeoff has to be made between the stronger aliasing effects generated at lower sample rates and the greater length of the main filter imposed by higher clock rates.

A clock rate of 32 kHz constitutes a suitable compromise for this low-pass filter with a passband of 3.2kHz. The main transversal filter with 55 taps is of reasonable length and the prefilter, required to roll off 30kB between 4kHz and the first reflection of the passband at 28kHz, could be implemented with a

second order active filter. A spare operational amplifier has been provided on this chip, which could be used with external components to realize such a prefilter.

Half the devices on each wafer use another approach to prefiltering. They have a special input structure to the CCD main filter, which samples the incoming signal at a higher rate and combines these subsamples in a suitably weighted manner to generate the signal charge packets that are injected into the CCD. In this particular device the effective sampling rate of this antialiasing input is 64kHz, and the respective weights are 1/8, 3/8, 3/8, 1/8. Thus each charge packet injected into the main filter is composed of four subsamples in a summing process that stretches over 2 full clock cycles. The weighted subsamples are generated by four separate voltage inputs using four metering wells of different sizes. The subsamples are combined in two summing wells from where they are injected alternately into the main CCD. A detailed discussion of such antialiasing inputs is given in another paper in this issue (5).

This prefilter provides a very good rejection of the first repetition of the passband at 32kHz, since the particular prefilter function chosen has a third zero at this frequency. In the passband, on the other hand, this prefilter produces a droop of several percent. To maintain the required flat response throughout the passband, the tap weights in the main filter are suitably adjusted to boost the transmission of this filter towards the upper edge of the passband (Figure 8). This predistortion is carefully chosen to compensate

for the combined roll-off due to the prefilter and due to the sample-and-hold restoration circuit at the output of the device. The program developed by McClellan et al. (3) can readily be used to find the proper tap weights for the CCD main filter.

The unavoidable rounding errors in the implementation of the tap weights will lead to a predictable deviation from the ideal filter response. The limiting accuracy is given by the incremental addressing step for the positioning of the split in the sense electrodes with respect to the overall channel width. The masks for this device were generated with an Electron Beam Exposure System (9) which provides 0.5 μm addressing steps. The channel width of the main CCD was 250 μm leading to a maximum rounding error of 2×10^{-3} of the largest sense electrode length, which corresponds to an absolute accuracy of about 11 bits (including sign) for this filter. Since the maximum tap weight is about 0.25 and the splits can be placed right up to the edge of the channel, this leads to a filter tap weight accuracy of 5×10^{-4}.

In many cases these predictable errors will be dominated by random errors in the tap weights due to misalignment or processing nonuniformities. Tap weight changes resulting from misalignment of the split electrodes with respect to the transfer channel are particularly serious, since they combine in a coherent manner and produce a frequency response

$$\Delta R(f) = 2 \cdot \Delta x \cdot \frac{h_{max}}{W} \cdot N \cdot \frac{\sin N\pi f/f_c}{N\pi f/f_c}$$

where Δx is the misalignment perpendicular to the channel axis, h_{max} is the normalized coefficient of the largest tap weight, W

is the channel width, fc the clock frequency and N the number of tap weights. This response ΔR is superimposed onto the desired frequency response. The largest error occurs at dc, and in this device is is about ±11% for a misalignment of ±1 μm.

V. Results

Filters with a normal voltage input and with anti-aliasing inputs were built on the same wafers so that an easy comparison was possible. Figure 9 shows the reproduction of the passband just above and below the clock frequency f_c when the normal voltage input is used. The only attenuation of this band results from the $(\sin \pi f/f_c)/(\pi f/f_c)$ function associated with the sample and hold circuit at the output. The triple zero at the clock frequency f_c produced by the anti-aliasing input, on the other hand, completely suppresses the reproduction of the passband. The latter figure also shows that the predistortion of the main filter function is effective and produces a flat response in the passband and in the stopband up to the Nyquist limit.

Blown-up views of the passband in the fundamental branch are shown in Figure 10. The stopband rejection meets the design goal of 32 dB for his filter. The passband ripple meets the specification of ±1/8 dB only marginally.

Second and third harmonic distortion have been measured - function of signal amplitude. At a 1V rms level both these harmc ics are 50 dB below the fundamental. A main source of this remaining small nonlinearity is attributed to the voltage dependence of the fingered MOS feedback capacitor around amplifier A_D.

The noise of this self-contained filter measured over a bandwidth of 15kHz is 1mV rms thus giving a signal to noise ratio in excell of 60 dB for the largest signals that can be handled by the device (1.2 V rms). Major noise sources are the turn-off of the input gates in the voltage inputs and reset noise of the clamp switches. The above numbers have been measured with a setup using an external correlated double sampling system to minimize the reset noise of the switches in the feedback path around A_D. It is expected that these results will improve somewhat when this function is also performed by on-chip circuitry.

VI. Conclusion

A self-contained 55-tap low-pass split-electrode filter has been built to provide a practical component in a 16-pin dual-in-line package that can readily be used by the systems designer without the need for peripheral support circuitry. The device has been fabricated with a "standard" two-level polysilicon gate process combining charge transfer channels, analog circuit elements, digital logic blocks and n-MOS operational amplifiers on the same chip. It shows that the employed 6-mask process offers sufficient design freedom to provide all these elements with good performance and high yield. The split-electrode transversal filter approach is very flexible and can quickly lead to custom-made filter functions. Only one mask level has to be changed in order to obtain a modified filter function with the same number (or fewer) taps. A well-designed chip can thus provide the basis for a mask programmable filter technology.

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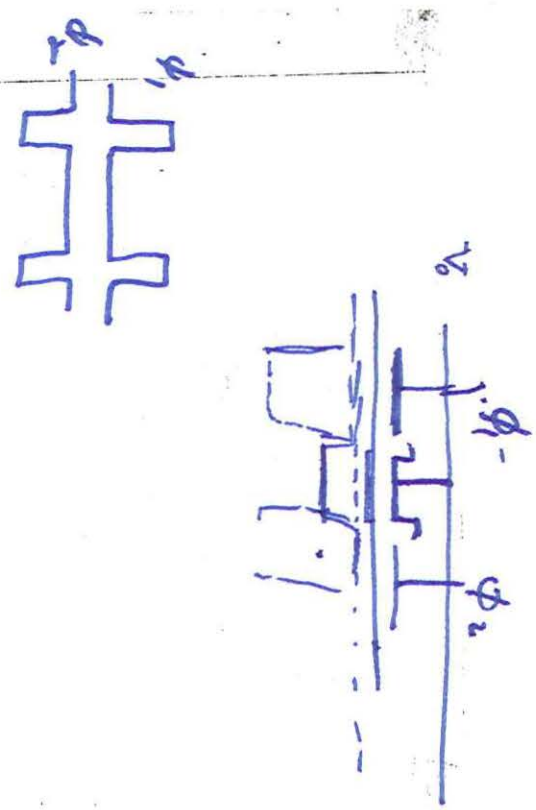

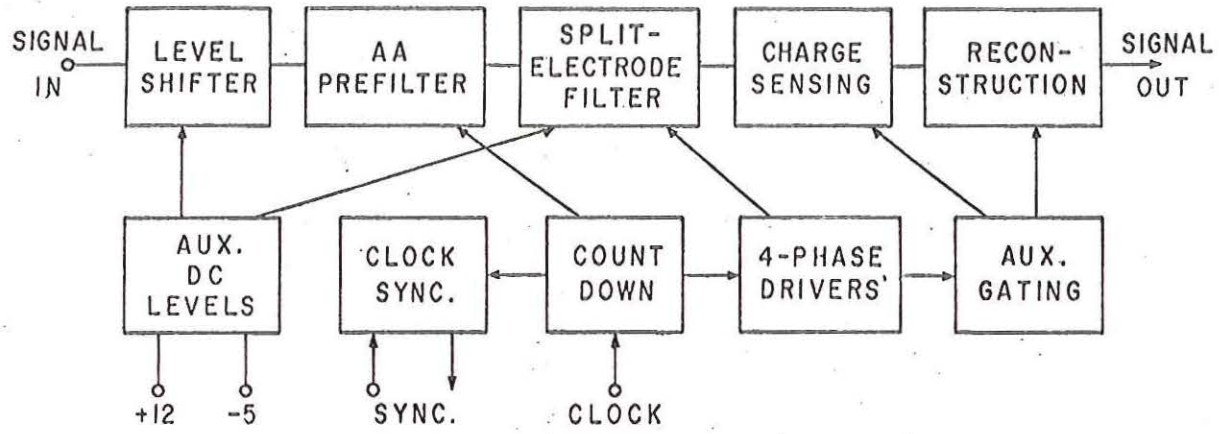

Fig. 1 - Functional blocks of self-contained charge-coupled split-electrode filter.

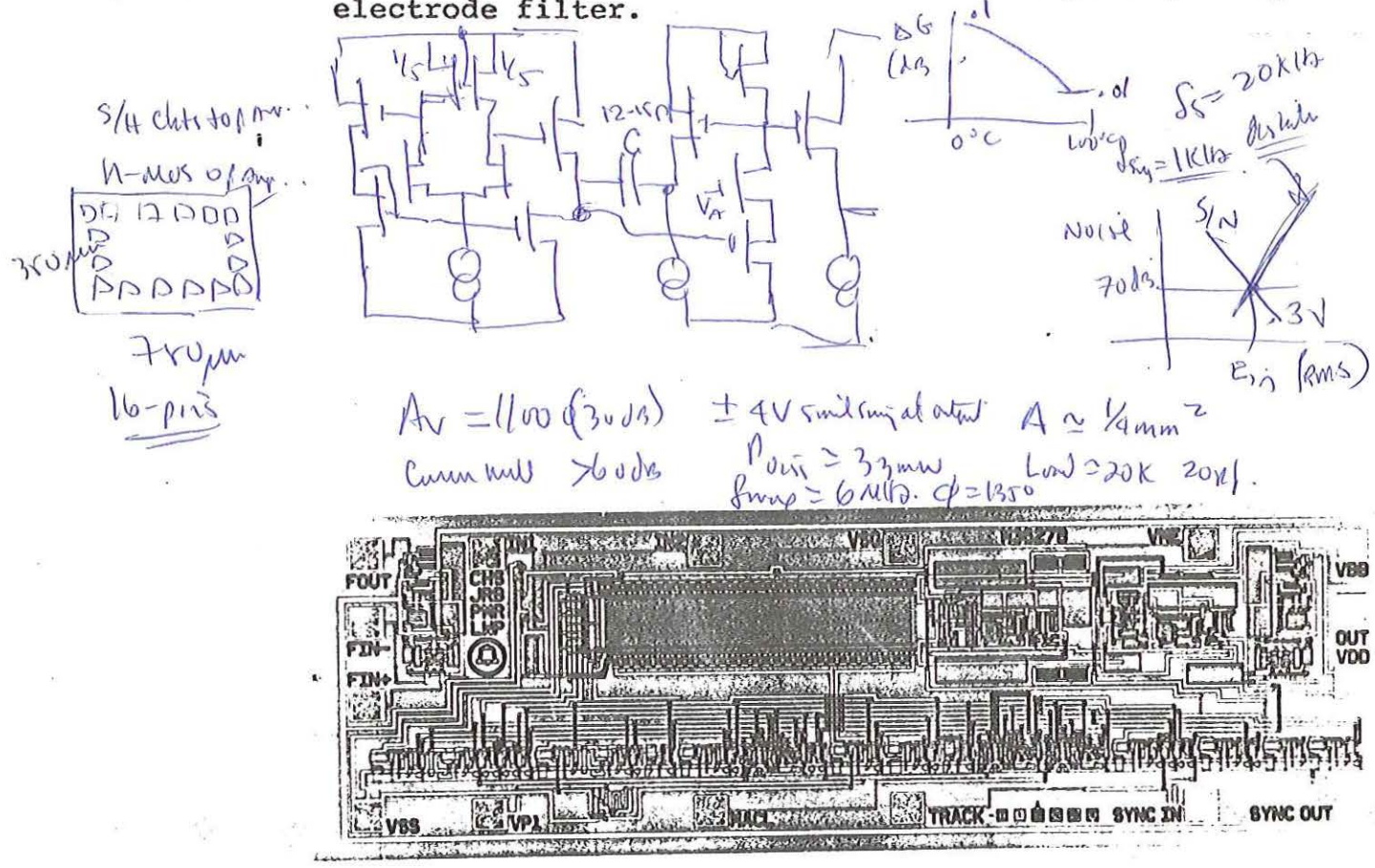

Fig. 2 - Photograph of the self-contained 55-tap split-electrode low-pass filter. The chip measures 1.7 mm x ~4 mm.

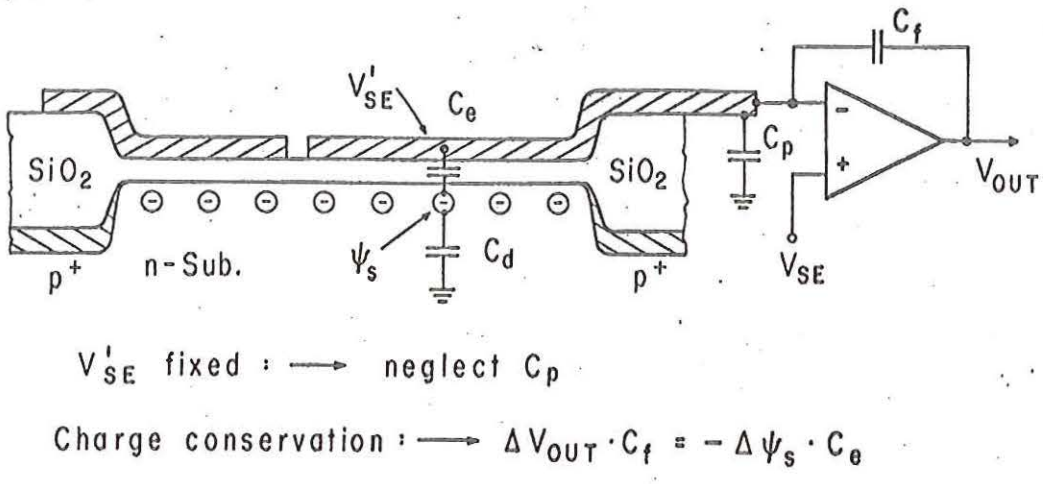

Fig. 3 - Cross section through transfer channel and split electrode showing basic arrangement to sense image charge on a virtually clamped electrode.

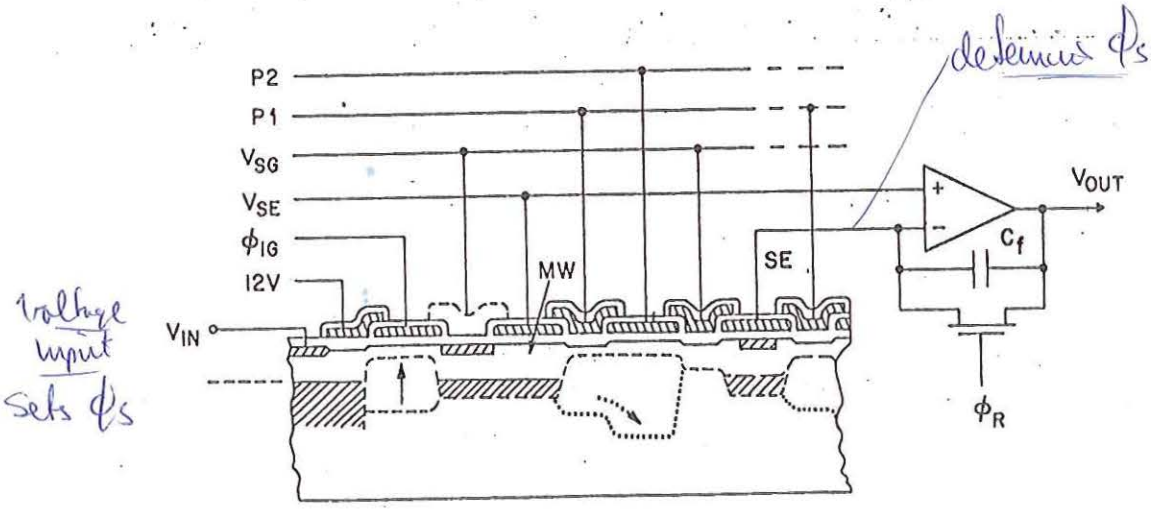

Fig. 4 - Basic input output arrangement for split electrode filter with linear transfer function. The metering well (MW) associated with the voltage input is electrically matched to the sensing well under the split sense electrodes (SE).

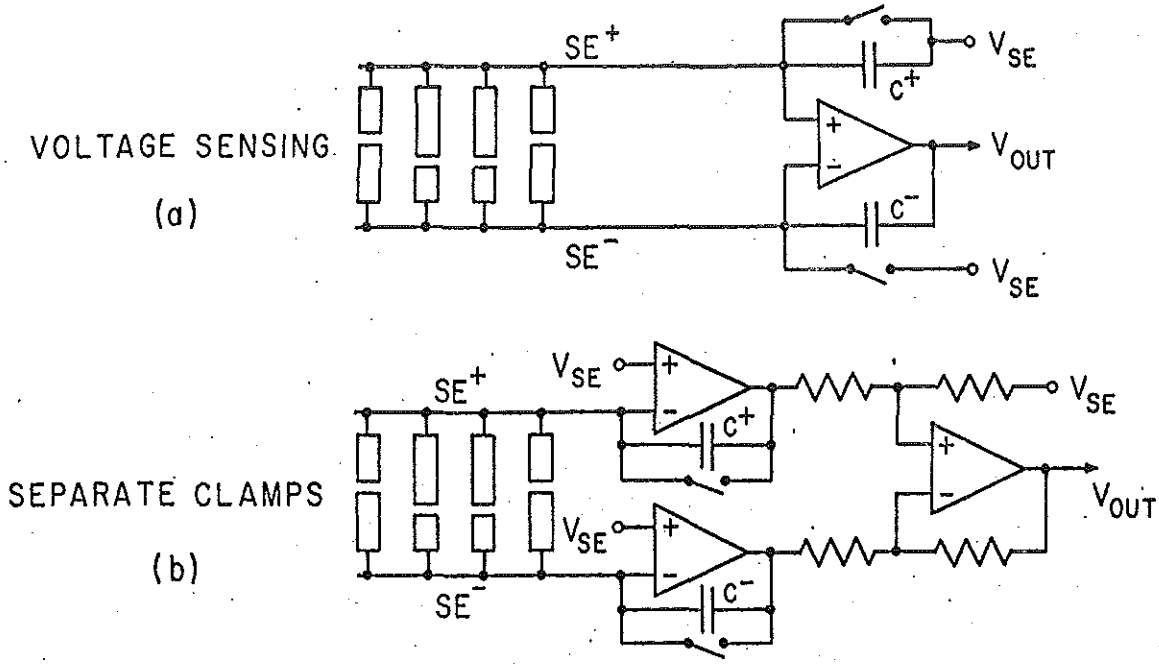

Fig. 5 - Differential sensing circuits for split-electrode filters. (a) Voltage sensing on floating sense electrodes. (b) Difference sensing with individually clamped sense buses.

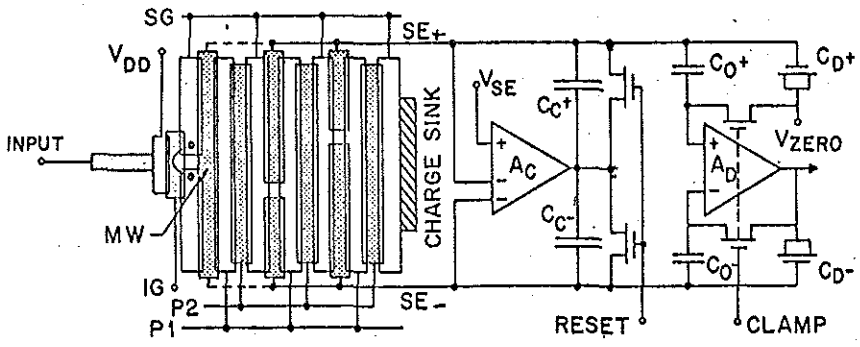

Fig. 6 Schematic view of split-electrode filter with common mode voltage suppression and voltage difference sensing.

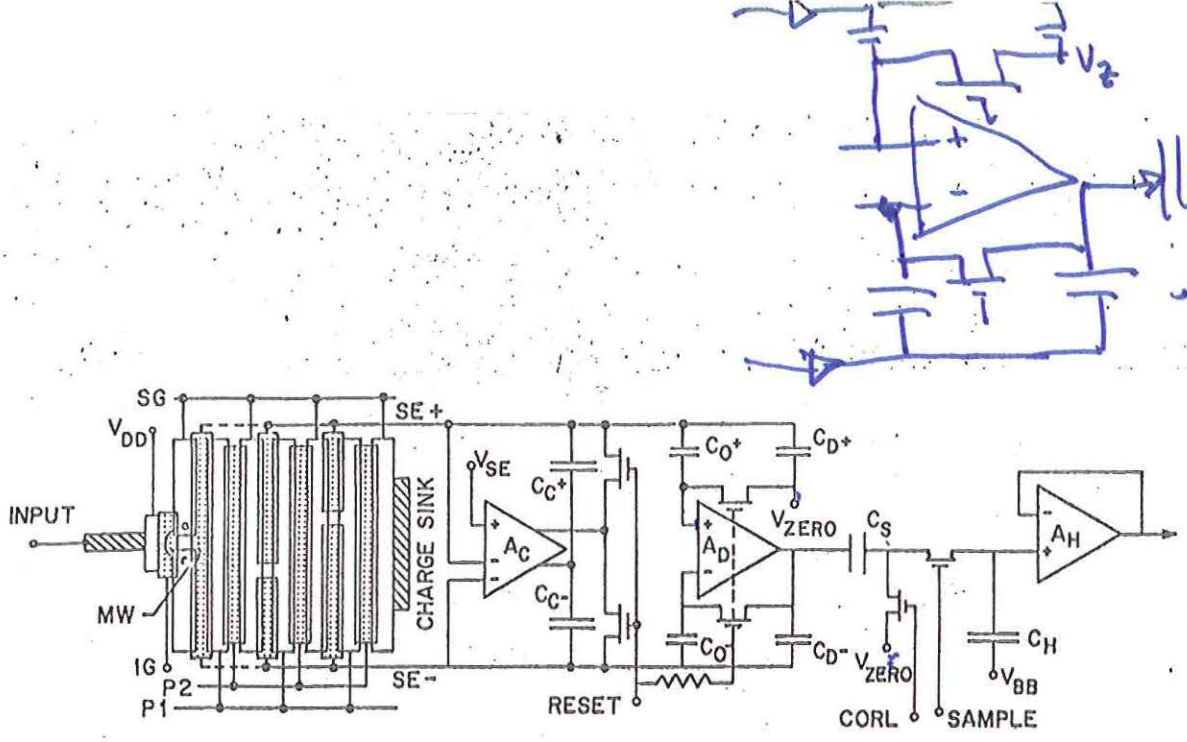

Fig. 7 Schematic view of split-electrode filter with common mode voltage suppression, voltage difference sensing and correlated double sampling.

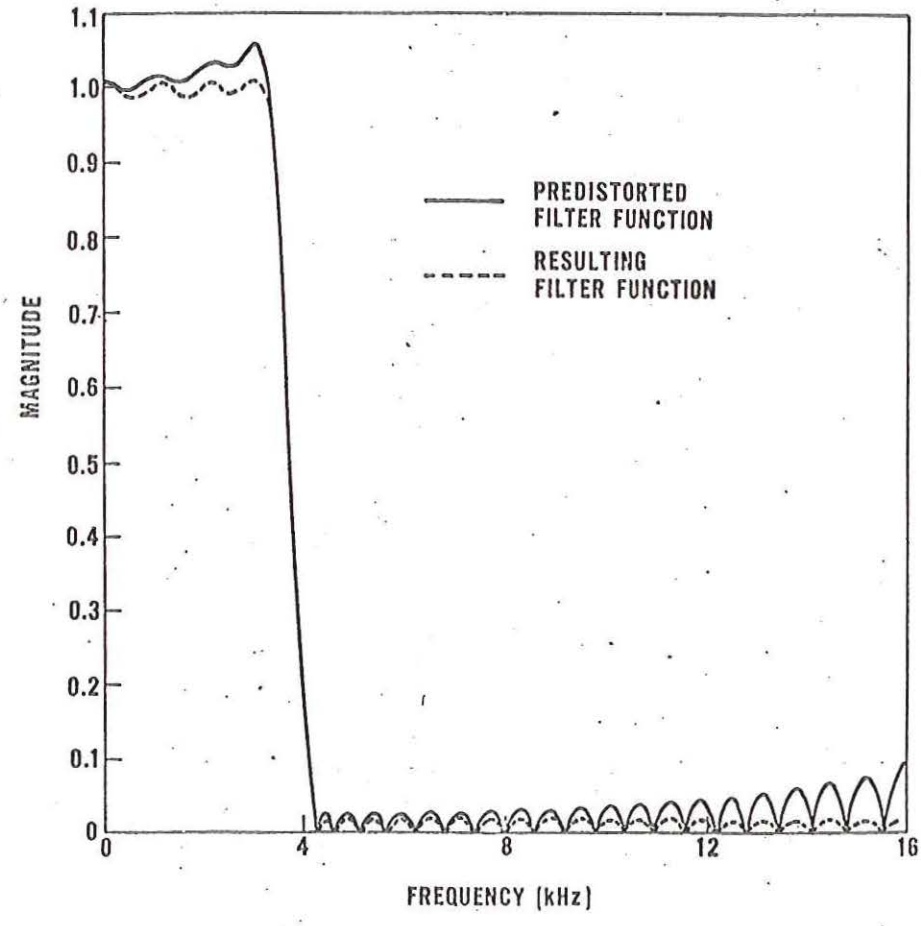

Fig. 8 - Predistortion of frequency response of main filter to compensate for the combined roll-off of antialiasing input and sample-and-hold output.

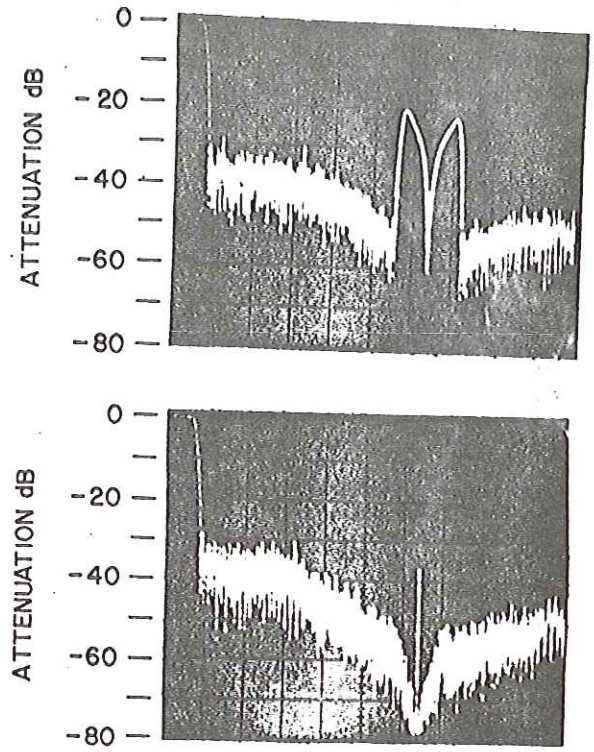

Fig. 9 - Comparison of the frequency response of normal voltage input (top) and antialiasing input (bottom). Clock frequency is 32kHz, horizontal scale 5kHz/div.

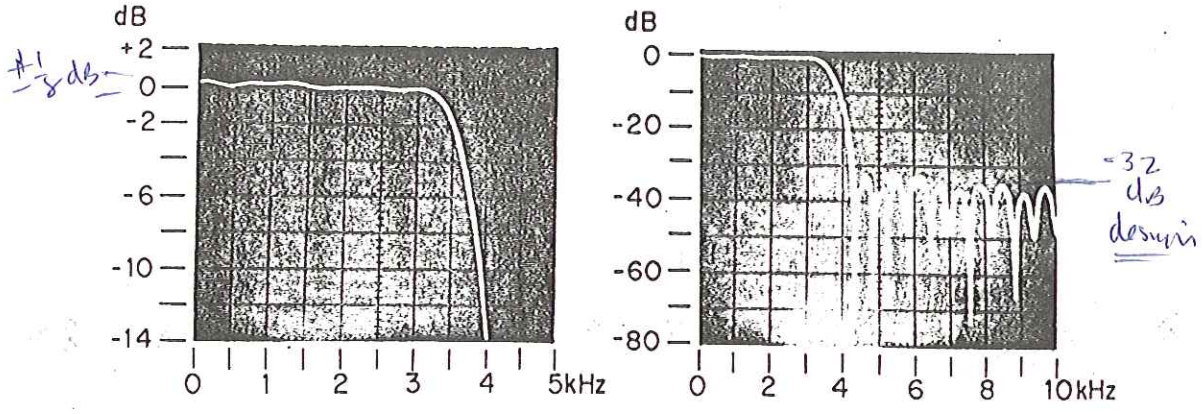

Fig. 10 - Fundamental branch of the frequency response of the low-pass 55-tap filter on two different scales: (a) 500Hz/div., 2 dB/div.; (b) 1kHz/Div., 10 dB/div.