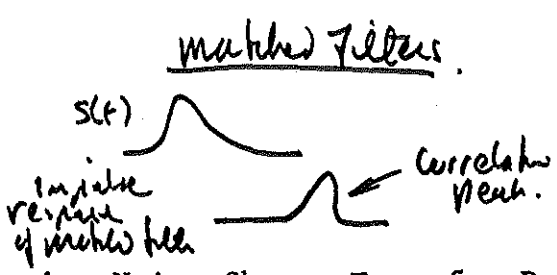

Radar Signal Processing Using Charge Transfer Devices

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I. Introduction

With the advent of medium scale integration (MSI) and large scale integration (LSI) digital signal processing has rapidly become the preferred approach for modern radar systems. One major disadvantage of high performance digital systems, however, has been the expense, complexity and power consumption of analog-to-digital (A/D) conversion whenever a large dynamic range (8 bits or more) is required in conjunction with a large bandwidth (5 MHz or more). A second disadvantage of the digital approach is the weight and power consumption of the required digital hardware. An ideal solution to the problem is to use charge transfer devices (CTD's) as low cost analog sampled data processors, thereby eliminating the need for A/D conversion entirely.

CTD's are analog, sampled data signal processing devices that incorporate the memory function on the same chip with the signal processing. The analog signal is sampled and charge packets proportional to the analog signal are manipulated in the CTD device. Hence, CTD's utilize a continuous range of amplitude, and are inherently large dynamic range devices. The

bandwidth of a serial CTD, in addition to being Nyquist limited to one-half of the input sampling rate, may be further limited by the overall charge-transfer efficiency of the device. In applications that require many samples to be stored, therefore, the use of parallel or series-parallel architectures may be necessary. Other considerations, such as the linearity of the input-output relationship, or the effect of thermally generated dark current, or the pattern noise that can result from the non-uniformity of such dark current also have a bearing on the design of each particular application.

II. Pulse Compression

A. Linear F-M Coded Waveforms

Most modern radars use pulse compression to obtain maximum range resolution for fixed transmitted power. Typically the transmitted waveform is a sinusoid in which the frequency varies linearly with time (LFM code). The pulse compression is similar to matched filtering except that the filter response is apodized to minimize sidelobes.

In many radar systems this pulse compression function can be performed using CTD fixed tap weight split electrode transversal filters.[1-3] An example of matched filtering using CTD split electrode filters is shown in Fig. 1.[4] This example does not represent the state of the art in CTD pulse compression,

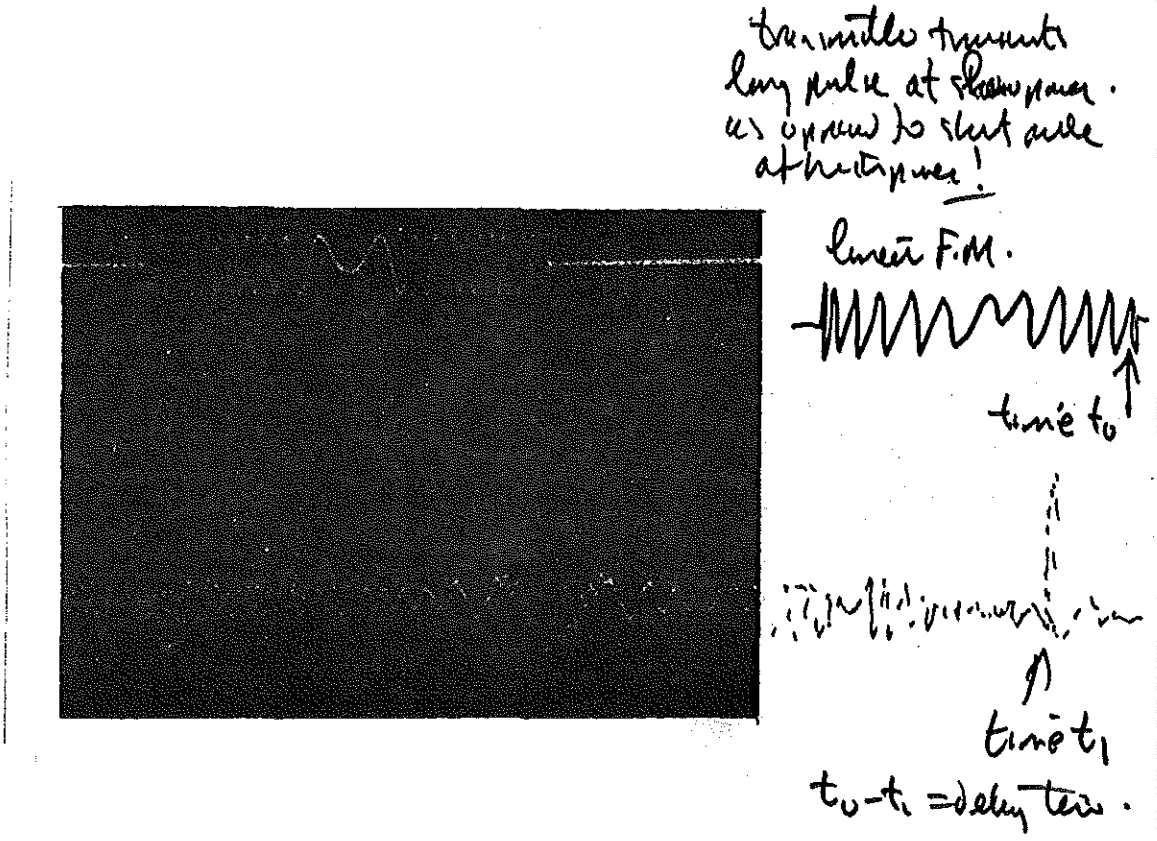


Fig. 1 Pulse Compression using a CCD transversal filter a) input LFM waveform, b) compressed output

since the filter tap weights were not apodized to achieve minimum sidelobes.

The suitability of CTD filters for pulse compression is determined by the time-bandwidth (BT) product and the actual bandwidth required for a particular application. Assuming the bandwidth of the CTD filter is limited to the Nyquist bandwidth ($B = f_c/2$), the BT product may be evaluated as

$$BT = \frac{f_c}{2} \frac{N}{f_c} = \frac{N}{2} \qquad (1)$$

Where N is the number of stages and f_c is the clock frequency. The bandwidth of the CTD will be $f_c/2$ for $N\epsilon = .18$. Substituting for N in (1) gives

$$BT = \frac{.045}{\epsilon} = 450 \qquad (2)$$

for $\epsilon = 10^{-4}$. Here ϵ is the transfer inefficiency per transfer. The actual bandwidth that can be achieved in a CTD filter will usually be limited by the circuitry used to recover the voltage difference on the split electrodes rather than transfer inefficiency.

Weighting coefficient error will not limit the performance of CTD pulse compression filters.[5] Since the filter is "matched" to the signaling waveform "noise" associated with random tap weight errors will not be a limitation.

B. Pseudo-Random Binary Coded Waveforms

In some modern radars it is desirable to modulate the radar signaling waveform with a pseudo-random binary sequence. The pseudo-random sequence may or may not be repetitive. For this application an electrically programmable matched filter for a binary sequence is appropriate and has been implemented in CTD technology.[6] Rather than the serial architecture used in the CTD split electrode filter, the programmable filter uses a parallel architecture which is shown schematically in Fig. 2.

In this chip, charge packets are not clocked along as they are in the serial transfer approach. Instead, each charge packet is placed in an isolated region where it stays until replaced. This is accomplished by the scan shift register, which sequentially opens the gate regions between each of the isolated cells and the analog input bus. A single binary "one" in this shift register causes each gate to be opened as it progresses down the shift register. Once a charge packet has been inserted into a storage reservoir, it is non-destructively read by controllably transferring it back and forth under three readout electrodes which serve all cells in the system and which provide a choice of two tap weights. The displacement currents that accompany these transfer operations are sensed by external circuits, and in this way, multiplication by binary tap weights, which are normally chosen to be ± 1, followed by a summation over cells is accomplished.

It is possible to extend the correlator function performed by the structure described above to a large number of chips without degrading accuracy. The interconnections required are shown in Fig. 3. The active bit in the scan shift register is simply passed from one chip to the next so that analog samples will be inserted in the following chip as soon as each chip is full, and the binary signals are similarly passed from chip to chip.

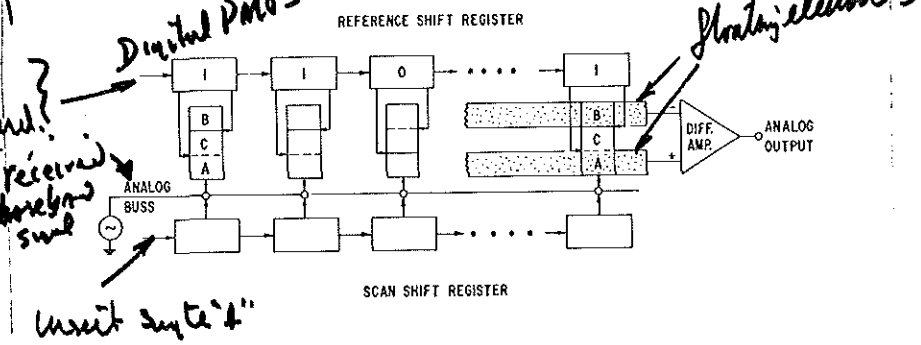


Fig. 2 Block diagram of correlator architecture.

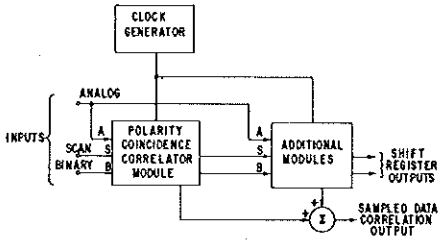


Fig. 3 Method of cascading correlator chips.

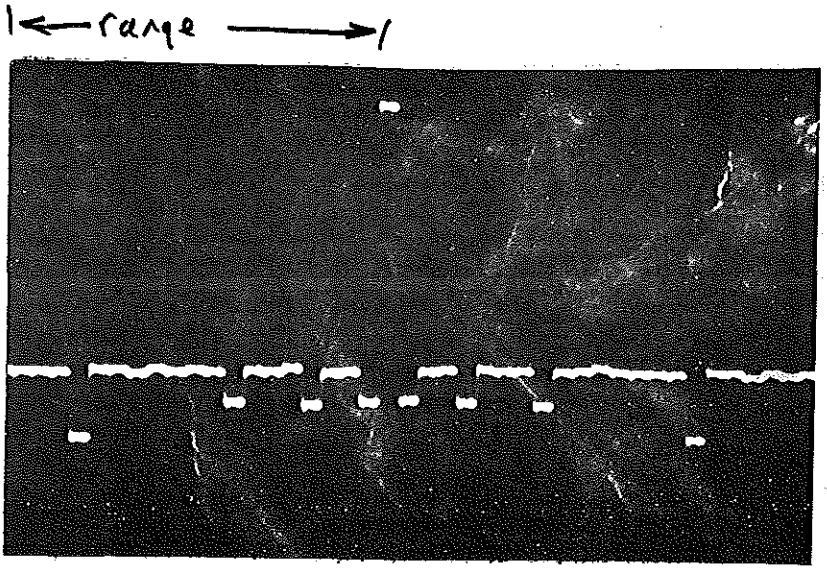


Fig. 4 Correlator output for 32 bit p-n code.

Summation of the output signal from several chips is accomplished simply by connecting the corresponding output electrodes of all chips together. Since the analog samples remain fixed in position and only the digital signals propagate from stage to stage and from chip to chip, and since these are regenerated at every stage, there is no degradation in signal accuracy in the parallel transfer approach as more samples or more chips are added. An example of the correlation peak obtained with this device for a 32 bit binary coded sequence is shown in Fig. 4. This 32 bit device has also been cascaded to obtain a programmable matched filter for a 256 bit sequence.

In contrast to the serial charge transfer approach charge transfer inefficiency does not limit the performance of this device. Since each charge sample is stored in its own cell and merely "sloshed" back and forth under control of the clock electrodes, any charge left behind on one transfer will be recollected on the next clock cycle. The bandwidth of this device is primarily limited by the signal recovery circuitry associated with the non-destructive readout of the charge "sloshed" in each cell and sampling rates of 10 MHz have been achieved. Since the time bandwidth product of this approach is not limited by charge transfer inefficiency BT products of 10^6 have been realized.

III. Moving Target Indicators[7]

In many radar systems an MTI is used to enhance the signal-to-clutter ratio of the received signal by reducing signals due to sea or ground clutter. There are two basic MTI systems that may be used for this purpose, viz., a delay line canceller whose operation is based on the difference in Doppler shift of near-stationary clutter returns and moving targets, and a range-gated MTI that examines segments of the total range with Doppler filter banks to discriminate against stationary target returns and obtain target velocity signatures. In this section the implementation of a delay line canceler using CTD's is described and experimental data are presented.

The basic form of a delay line canceller is shown in Fig. 5(a). Functionally, the delay line canceller subtracts the radar return of one pulse repetition interval (PRI) from the return obtained during the previous PRI. The delay period T is made equal to the reciprocal of the radar pulse repetition frequency (PRF), which results in a frequency response magnitude characteristic such as is shown in Fig. 5(b). Spectral components of radar returns that occur around dc and at harmonics of the PRF are suppressed, thereby attenuating the clutter energy which exhibits a low Doppler spectral spread around the PRF lines (corresponding to returns from fixed or stationary targets), while passing the higher Doppler energy from moving targets.

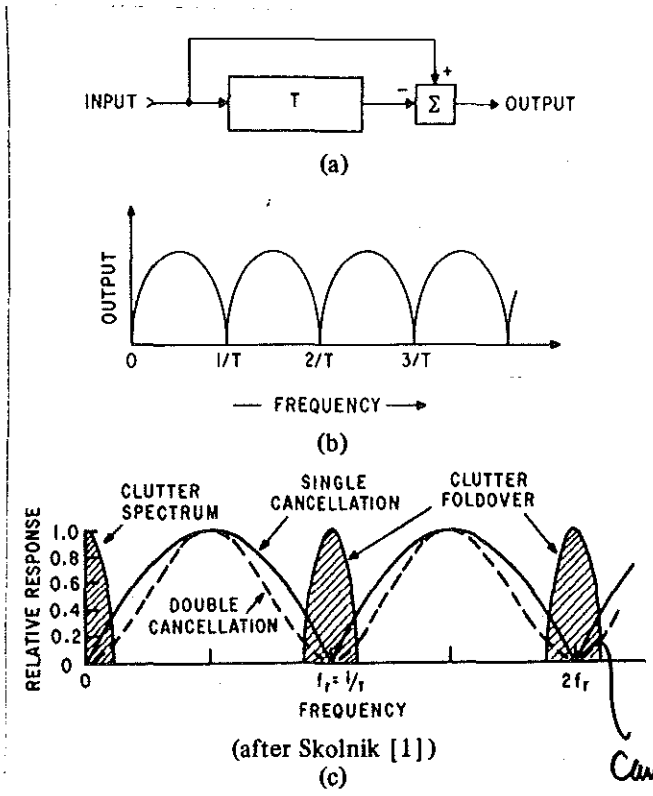


Fig. 5 Block diagram and frequency response of MTI filter.

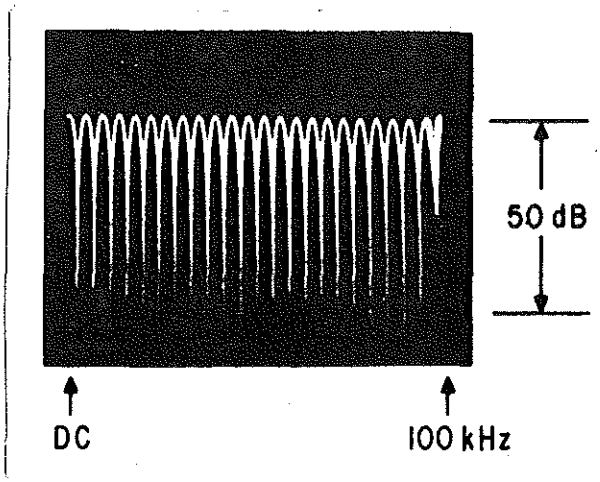
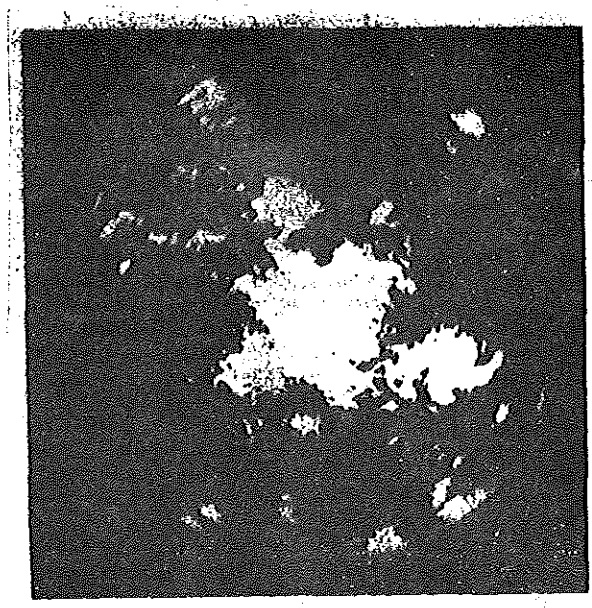


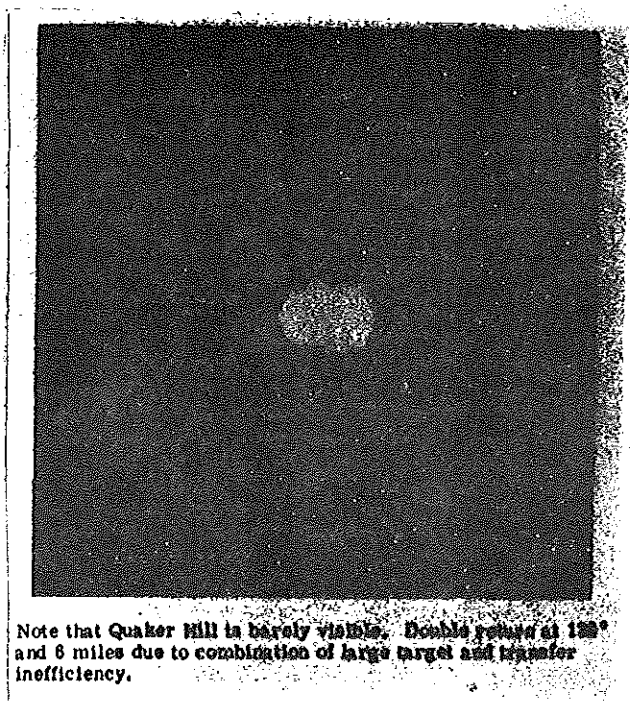
Fig. 6 Frequency response of MTI filter.

Can also be PRF jitter, as well as slowly moving targets.



Range: 14 miles
Quaker Hill at 335° to 355° and 5 to 8 miles approx. 60 dB above noise. Rain storm from 310° to 335° at 10 to 12 miles

Fig. 7 Clutter map with MTI bypassed.



Note that Quaker Hill is barely visible. Double return at 120° and 6 miles due to combination of large target and transfer inefficiency.

Fig. 8 Clutter map with MTI activated.

The characteristics of the delay line will determine the extent to which the suppression can be maintained over the bandwidth of the radar signal and, therefore, the total clutter power reduction that can be achieved. For example, the frequency response function of a single delay line canceller [such as is shown in Fig. 5(a)] may not have as broad a clutter rejection notch as desired. The notch can be widened by placing two cancelers in series. This configuration processes three pulses simultaneously, and is, therefore, known as a three-pulse canceler. The improved response is that of a squared sine wave as is shown in Fig. 5(c).

A major problem in the use of conventional analog delay lines has been the matching of delay elements to the system PRF, particularly in the case of three-pulse cancellers where the first delay line usually controls the PRF, the second is slaved to the first, and complex temperature-controlled ovens surround the delay media which is normally quite temperature sensitive. Insofar as a CTD can be operated as an analog delay line, the delay period of which is accurately controlled by a digital clock, it is well suited to the implementation of an MTI filter. A charge-transfer MTI was designed as a direct replacement of an acoustic delay line canceller in a burst radar system. The technical performance parameters of the canceler are listed in Table I.

TABLE I

MTI Parameters

Type:	Three-pulse vector canceler
Cancellation:	50 dB
Dynamic Range:	> 50 dB
System Waveform:	Multiple burst, 250 us PRI
Pulsewidth:	1 us
IF Bandwidth:	1 MHz
Input Format:	In-phase (I) and quadrature (Q) baseband video

The required bandwidth for the I and Q channels was 500 kHz. In practice, the input signal is usually sampled somewhat above the Nyquist rate, and in this instance, a sampling frequency of $f_s = 1.6$ MHz was selected. For a serial CTD of N stages, the total delay T is determined by the clock period and is given by

$$T = \frac{N}{f_c} \tag{3}$$

where the clock frequency $f_c = f_s$. For $f_c = 1.6$ MHz, the number of stages required for the memory is 400.

Individual double-delay channel achieved 58 dB of cancellation. The system performance level decreased to approximately 51 dB (as shown in Fig. 6) due to residual unbalances between channels. Figs. 7 and 8 demonstrate actual system performance. The hill in Fig. 7 (PPI display without MTI) is approximately 60 dB above noise. This hill is barely visible in Fig. 8 (PPI display with MTI activated). Although a little time elapsed between the change over to the MTI mode, several targets (at 60^{o}, 120^{o}, etc.) previously inundated in clutter can be easily correlated. Note that several discrete returns due to the site location, plus a rain storm, have been eliminated.

IV. Charge Transfer Analog Memory for ECM[7]

The objective of a radar ECM memory system is to generate synthetic or false targets. This is achieved by acquiring the radar pulse of interest (linear FM chirp), storing it for a maximum of one or more PRI's, and recalling and retransmitting it on command at any time within that storage period. The characteristics of some typical radar pulses are listed in Table II.

TABLE II

ECM Memory Signal Characteristics

Signal	Bandwidth (MHz)	Length (usec)
1	4.5	20
2	6.0	12.8
3	1.5	60
4	0.078	200
5	1.0	6

Preliminary design objectives were to achieve a 3 millisecond storage time over an operating temperature range of -55°C to +75°C. All spurious signal components due to harmonic or intermodulation distortion were to be at least 34 dB below the desired signal level. Having stored any one of the signals listed in Table II for up to 3 milliseconds, and subsequently processing that signal with a pulse compression filter, a final system performance objective was to incur no more than 5 dB degradation in the main to sidelobe ratio of the compressed pulse.

In order to take advantage of the d.c. restoration capability and the inherent temperature insensitivity of a differential device, a 68-stage dual-channel device was designed for this application. Each channel of this device is serviced by an identical set of upper and lower electrodes with the exception of the third lower electrode, which provides the necessary analog input control

of the charge transferred along each shift register, and is therefore brought out to a separate pad. Similarly, separate output stages are provided for each channel. The input scheme used for this device is the so-called "fill-and-spill" linear method similar to that proposed by Tompsett. The output of the device is obtained by measuring the charge dumped into an isolated output diffusion.

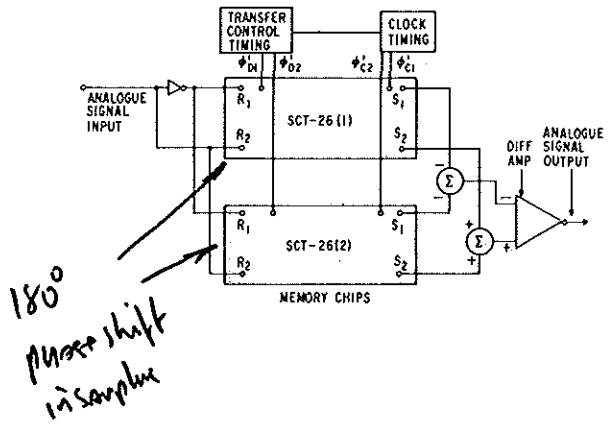


Figure 9: Push-pull Differential System Configuration

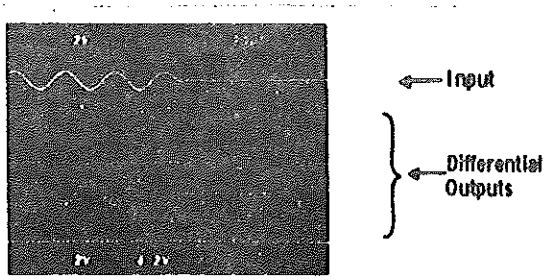
A push-pull differential configuration of CTD's (such as is shown in Fig. 9) was used, since it has been established that such an arrangement makes good use of available device signal bandwidth, reduces clock feedthrough and hence relaxes post-memory

filtering, and in addition provides automatic compensation for dc offset caused by uniform buildup of dark current during signal storage.

Experimental results from a single dual-channel device are shown in Fig. 10, where separate channel and differentially summed outputs are shown, and in Fig. 11 where the output from a push-pull differential quad is shown.

The effectiveness of push-pull operation is shown in Fig. 12, where the suppression of the clock, and in particular, the lower sideband of the clock is sufficient to allow the device to be operated with a clock frequency less than twice the bandwidth, of the input signal. In the push-pull mode, of course, the input sampling rate is twice the clock frequency, so that the Nyquist sampling applies in all cases.

Typical storage characteristics are shown in Fig. 13, where the upper or lower photographs show performance at $T = 25^{o}C$ and $T = 75^{o}C$, respectively. In each case, the lower trace shows the input signal which consists of eight cycles of a sine wave. The upper trace shows the output sampled data from the memory. The first 64 samples to be read out (covering three cycles of the sine wave followed by a dc segment) represent data which has been stored in the memory for the 3 millisecond storage time during



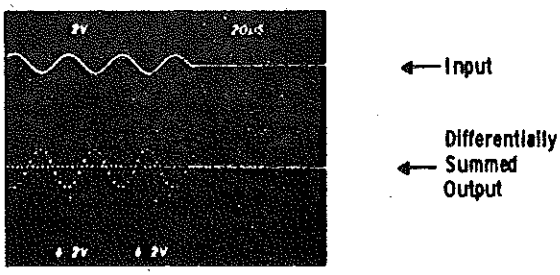


Fig. 10 Separate and differentially summed outputs of ECM memory device.

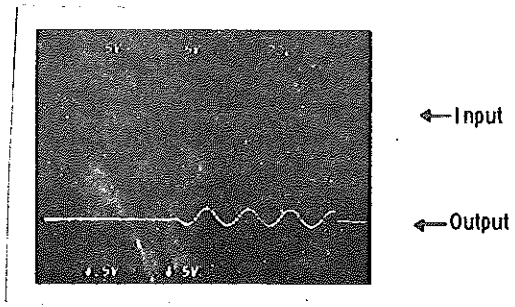


Fig. 11 Output of push-pull differential quad.

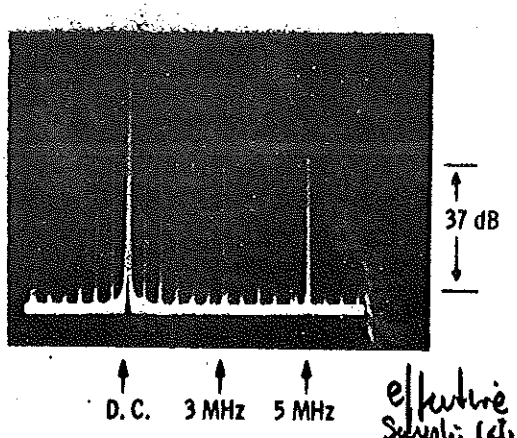


Fig. 12 Push-pull operation; output frequency spectrum.

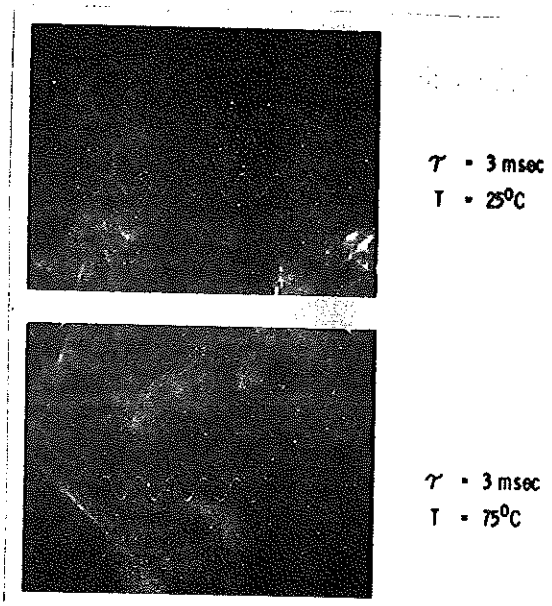
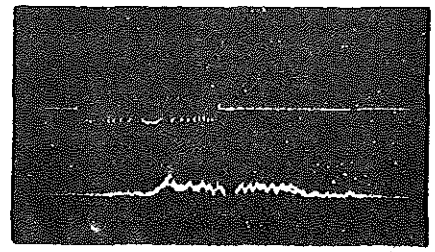


Fig. 13 Storage characteristics of SCT device.

which time the clocks have been interrupted. The remaining samples (corresponding to the 4 1/2 cycles of the sine wave on the R.H.S. of the trace) represent data that has been sampled, and clocked straight through the memory without interruption. Thus, the effect of turning off the clocks for 3 milliseconds can be observed by comparing the three cycles on the left side of the trace to the 4 cycles on the right side of the trace. At T = 25°C very little degradation is visible. At T = 75°C the pattern noise that results from the non-uniformity of the dark current is noticeable, but is still relatively small.

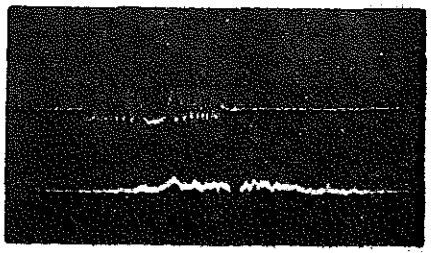
System experimental results are shown in Fig. 14 and 15. In Fig. 14, is shown the compressed pulse with and without the memory for the 4.5 MHz, 20 μ-second signal. For these data, the pulse compression system was capable of providing a compressed pulse with 20 dB main/side lobe ratio. No further degradation in this ratio occurred when pulse was stored in the memory for 3 milliseconds. In Fig. 15 is shown similar experimental results for the 6 MHz, 12.8 u-second signal. In this case, the system was capable of providing a main'sidelobe ratio of 32 dB without the memory. By storing the signal for 3 milliseconds the main/side-lobe ratio was reduced to 28 dB.



EXPANDED PULSE

COMPRESSED PULSE

WITHOUT MEMORY
(M/S ≈ 20 dB)

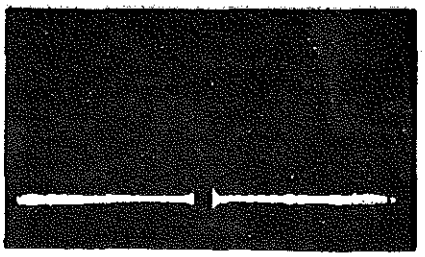


EXPANDED PULSE

COMPRESSED PULSE

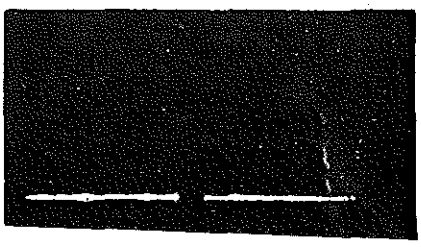
3 millisecond STORAGE
(M/S ≈ 20 dB)

Fig. 14 ECM memory test results; no degradation of compressed pulse is evident.



COMPRESSED PULSE

WITHOUT MEMORY
(M/S = 32 dB)



COMPRESSED PULSE

3 millisecond STORAGE
(M/S = 28 dB)

Fig. 15 ECM memory test results; 4 dB degradation in M/S ratio occurs after 3 millisecond storage.

V. Radar Pulse-Doppler Processing[5]

Much of the signal processing in a modern radar is concerned with the enhancement of targets that compete with clutter in the detection process. In many applications the radar cross section of land and precipitation clutter is much larger than the actual target cross section. Thus the amplitude of the clutter signal will often exceed the actual target in a given range bin. Since the target is usually moving with respect to the clutter sources, a moving target indicator or doppler processor can be used to separate targets from clutter.

In the classical MTI canceller a few (usually two to four) sequential pulse returns are delayed in a digital or analog delay line and subtracted to suppress the stationary returns. The effectiveness of this approach depends on the actual clutter characteristics near zero doppler and on the overall radar system stability (e.g. pulse to pulse timing stability).

In contrast the range gated pulse doppler technique is implemented by looking at many radar returns (20 to 100) in a single range bin. This technique can be visualized by imagining a signal processor which sorts the video return into range bins and a bank of bandpass filters connected to the output of each range bin. The output of each filter must be detected and integrated over a number of pulses. An output from any filter indicates a target in that range bin. Since the integration is performed coherently from pulse to pulse the doppler frequency is preserved

in the spectrum and is a measure of target velocity. By using very narrow band filters and integrating over many pulses an improvement in signal to noise ratio or clutter can be obtained. Since the pulse-doppler signal processor typically uses a filter with a narrower bandwidth than the MTI canceller it is used in radar systems which require detection ofsignals which are small compared to broadband noise and clutter.

In the past, a digital implementation of a discrete Fourier transform has been used to perform spectral analysis of range gated pulse doppler video signals. Unwanted signals due to stationary objects or other sources of clutter appear in doppler bins near zero frequency and can be discarded while processing doppler target signals from the same range bin.

Charge transfer devices can be used to implement the discrete Fourier transform using the chirp-Z algorithm.[8] Since the CTD implementation uses the analog signal directly without digitization it promises the advantage of lower weight, power and cost in many radar systems.[9]

The chirp-Z transform is derived from the definition of the discrete Fourier transform.

$$F(k) = \sum_{n=0}^{N-1} f(n)\, e^{-j2\pi nk/N} \qquad k = 0, 1, \ldots, N-1 \qquad (4)$$

where f(n) are the N samples of the analog data to be processed.

In the pulse-doppler radar, these are the N sequential samples from a given range bin. Substituting

$$nk = 1/2\ [n^2 + k^2 - (k \ominus n)^2] \tag{5}$$

produces the expression,

$$F(k) = \underbrace{e^{-j\pi k^2/N}}_{\text{post multiply}} \left[\sum_{n=0}^{N-1} \underbrace{f(n)e^{-j\pi(k-n)2/N}}_{\text{convolution}} \underbrace{e^{-j\pi n^2/N}}_{\text{premultiply}}\right] \tag{6}$$

The expression above has been factored to illustrate the three operations used in the chirp-Z algorithm. These are: 1) premultiply by a chirp waveform, 2) convolution in a chirp filter, and 3) post multiply by a chirp waveform.

A block diagram of the chirp Z transform for a complex signal (I and Q baseband video) is shown in Fig. 16. The pre and post-multiply by a chirp waveform are shown at the input and output, respectively. The convolutions shown can be performed with charge transfer transversal filters. Typically the pre and post-multiplies are performed with multiplying digital to analog converters (MDAC's) with the coefficients being stored in a digital ROM.[10] For spectral analysis the post-multiply is not required since $e^{-j\pi n^2/N}$ is merely a phase term with a magnitude of unity. The spectrum is obtained by taking the magnitude of the two complex outputs shown at the right side of Fig. 16. The spectrum obtained using a chirp Z transform implemented with four 500 tap CCD transversal filters is given in Fig. 17.[10]

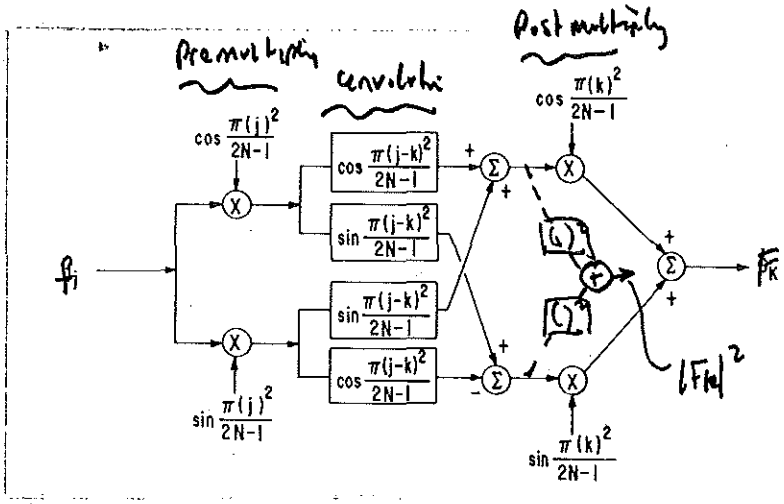


Fig. 16 Block diagram of complex chirp-Z transform implementation.

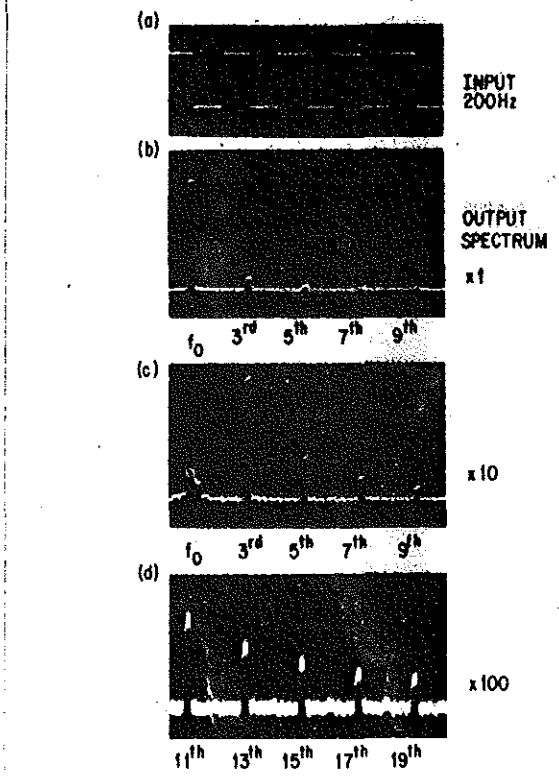


Fig. 17 Power spectrum of square wave obtained using chirp-Z algorithm and 500 tap CCD transversal filter.

A. CTD Analog Multiplier[11-12]

In many cases the use of digital ROM's and MDAC's for the required pre and post-multiplies limits the application of the chirp-Z algorithm in performing the discrete Fourier transform.

This section will describe a CCD premultiplier in which the output is a set of charge packets thus eliminating the need for an intervening voltage to charge conversion.[11-12] Furthermore this premultiplier stores the multiplier coefficients in the form of a set of analog tap weights and thus replaces the function of the digital ROM. The multiplier is a serial transfer structure where an analog multiplication coefficient can be stored at each stage of the device. Although the actual device is a four quadrant multiplier its operation can best be explained in terms of a simpler one quadrant device. Fig. 18 illustrates a three stage one quadrant multiplier. Each stage consists of two poly-silicon charge storage electrodes and two aluminum overlapping electrodes (not shown). The first charge storage region in each stage is divided into two parts by a channel stop, the location of which defines a multiplier coefficient as explained below. The lower portions of each divided stage can be connected to a lateral drain by turning "on" a lateral gate as shown in Fig. 18.

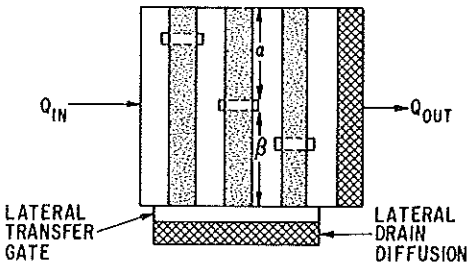


Fig. 18 Schematic of 3-stage one-quadrant multiplier.

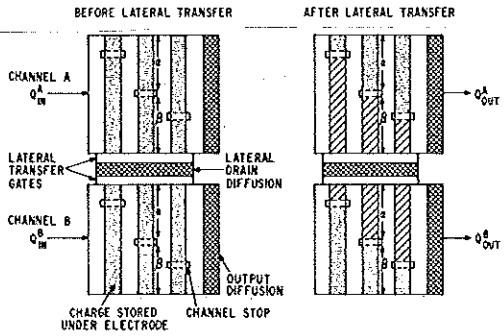


Fig. 19 Schematic of 3-stage four-quadrant multiplier: (a) After loading the input data but before lateral transfer, (b) After lateral transfer but before data output.

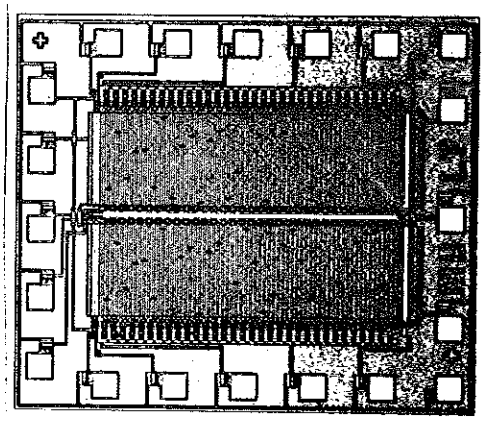


Fig. 20 Photomicrograph of 32 point four-quadrant multiplier.

Operation of this hypothetical one-quadrant device proceeds as follows. A continuous positive analog signal (one quadrant) is sampled at the input of the charge transfer device and charge packets proportional to samples of the analog signal are transferred along the shift register. (The channel stops do not impede this transfer.) When the three samples of interest have been clocked into the multiplier, the clocks are stopped. The lateral gate is opened and a fraction of the charge, determined by the location of the channel stop, drains into the lateral drain which is set at very negative potential (p channel device). The charge remaining is blocked from draining by the channel stops. The charge samples remaining are the original samples multiplied by the fractional coefficients determined by the location of the channel stops. The lateral gate is then closed and the resultant charge packets are clocked to the end of the shift register. As this charge is clocked along it spreads along the full length of the electrode.

For four quadrant operation, two parallel registers A and B are used as shown in Fig. 19. The multiplication coefficient at each stage of the device is W_n where $W_n < 1$. The channel stops in the nth cell divide both cells into lengths α_n and β_n where,

$$\alpha_n = \frac{1+W_n}{2} \tag{7}$$

and

$$\beta_n = \frac{1-W_n}{2} \tag{8}$$

Note that $\alpha_n + \beta_n = 1$, and $\alpha_n - \beta_n = W_n$. In register A the β sections are adjacent the lateral drain while in the B register the α sections are adjacent the drain. In operation an analog signal is added to a dc bias in the A register while the inverted analog signal is added to the same dc bias in the B register. The charge at any stage is $Q_{bias} + Q_{sig}$ in the channel A and $Q_{bias} - Q_{sig}$ in the channel B. After the draining operation, the charges remaining in the A and B registers are

$$Q_A = \alpha(Q_{bias} + Q_{sig}) \tag{9}$$

and

$$Q_B = \beta\,(Q_{bias} - Q_{sig}) \tag{10}$$

To recover the correct output the charge packets from the two registers must be summed yielding

$$Q_{out} = Q_{bias}\,(\alpha_n + \beta_n) + Q_{sig}(\alpha_n - \beta_n) \tag{11}$$

Since $\alpha_n + \beta_n = 1$ and $\alpha_n - \beta_n = W_n$, this reduces to

$$Q_{out} = Q_{bias} + W_n\, Q_{sig} \tag{12}$$

which is the desired result. That is, the output is the analog signal multiplied by W_n with an added constant bias.

Two separate 32-stage devices were fabricated for use as the pre and post multiplier on a chirp Z transform system. The multiplication coefficients were

$$W_n = \sin\left(\frac{\pi n^2}{63}\right) \quad n = 0,\ 31 \tag{13}$$

and

$$W_n = 0 \qquad n = 0 \tag{14}$$

$$W_n = \cos\left(\frac{\pi n^2}{63}\right) \quad n = 1,\ 31 \tag{15}$$

The device with the cosine chirp tap weights is shown in Fig. 20. The input and output are at the left and right, respectively. On the particular chip shown there is no provision for on-chip charge summing, but other designs have incorporated on-chip charge summing by connecting the output diffusions. The width of each charge transfer channel was 10 mils.

B. Application to Chirp Z Transform System

A system for performing a 32-point odd discrete cosine transform (ODCT) using a chirp Z-transform algorithm was implemented using four analog multiplier chips and four 63-tap CCD transversal filters. The ODCT is a linear combination of N real input values to yield N real output coefficients. It is defined by

$$H(k) = X(0) + 2\sum_{n=1}^{N-1} x(n)\cos\left(\frac{2\pi nk}{2N-1}\right) \tag{16}$$

If we define a new sequence $g(n) = X(0)/2, X(1),\ldots,X(N-1)$, then

$$H(k) = 2 \sum_{n=o}^{N-1} g(n) \cos \left(\frac{2\pi nk}{2N-1}\right) = 2 \text{ Re} \sum_{n=o}^{N-1} g(n) \exp \left(\frac{j2\pi nk}{2N-1}\right) \quad (17)$$

which is the real part of the 2N-1 point discrete Fourier Transform (DFT) of the sequence g(n) padded with zeros.

Since the ODCT is a DFT, it can be computed using the chirp Z-transform algorithm,[8] which involves complex multiplication, convolution, and multiplication. Converting the above expression for the cosine transform to the chirp format gives

$$H(k) = 2 \text{ Re} \sum_{n=0}^{N-1} \underbrace{g(n)\, e^{\frac{-j\pi n^2}{2N-1}}}_{\text{premultiply}} \underbrace{e^{\frac{j\pi(n-k)^2}{2N-1}}}_{\text{convolution}} \underbrace{e^{\frac{-j\pi k^2}{2N-1}}}_{\text{postmultiply}} \quad (18)$$

which can be implemented with the real arithmetic architecture shown in Figure 16.

The actual hardware implemented consisted of four subsystems.

1) An input signal generator which read predetermined 32-point sequences from a ROM through a D/A converter, producing a well-controlled synchronized test input.

2) A complex premultiplier which used two multiplier chips.

3) A full complex convolution which used four transversal filters.

4) A complex, post-multiplier which used two multiplier chips.

Since the input and output sequences of the cosine transform are real, the multiplier boards require only a single pair of real multiplications.

The cosine transform of an input sinusoidal signal of the form

$$x(n) = \cos\left(\frac{2\pi kn}{63}\right) \qquad 0 \leq n \leq 31 \tag{19}$$

is a single positive value at k and zero elsewhere. Figure 9 shows the output of the total CZT system for a sinusoidal input $\cos \frac{4\pi n}{63}$. The output step of 1 volt amplitude at $k = 4$ is shown in Fig. 21. The fixed pattern noise shown in Fig. 21 is dominated by the pattern noise associated with the two output postmultipliers. Assume there is a random error $\mathcal{E}$ associated with the coefficients of the premultipliers, the convolver and the post multiplier. If the error at the output due to an error $\mathcal{E}$ in the post multiplier is normalized to unity, the output error due to the premultiplier will be 1/63 and the output error due to the convolver will be 1/125 for a cosine transform of length 32.[13]

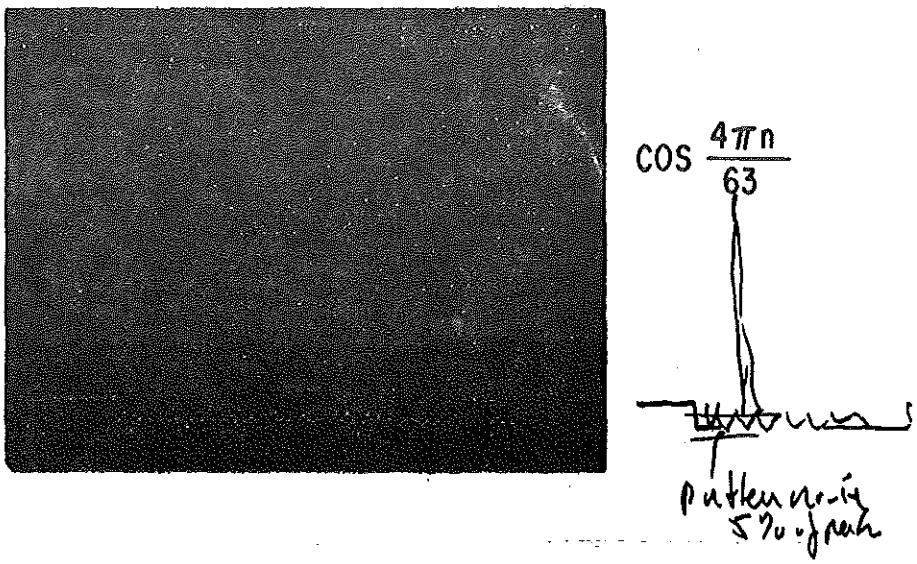


Fig. 21 Chirp Z-transform system output for a sinusoidal input $\cos\frac{4\pi n}{63}$

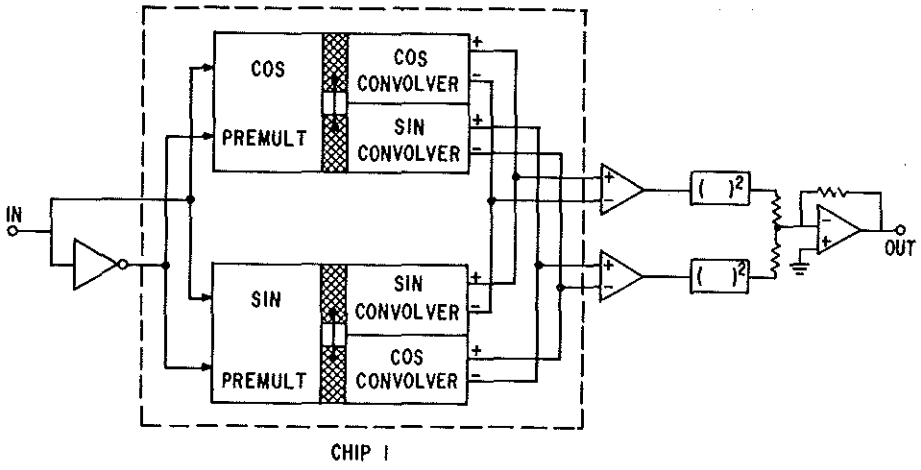


Fig. 22 Block diagram of single chip CCD spectrum analyzer.

The observed fixed pattern error was 75 mv peak to peak for this CZT system where a sinusoidal signal input would give $\pm$ 1 volt output. Thus the peak pattern noise error is 4 percent of full scale, while the RMS error is considerably less. The observed pattern noise was a factor of two larger than it need be since input dynamic range of the post multiplier was a factor of two larger than the actual linear output range of the convolvers. Thus a factor of two decrease in the fixed pattern noise of the overall system could be achieved by inserting a gain of 2 amplifier after the convolvers. This would increase the peak signal a factor of two, while leaving the pattern noise unchanged. Whether this level of performance would then be adequate would then depend on the particular system requirements.

In some applications, however, the output post multiplier is not required. In spectrum analysis for example, one is interested only in the magnitude of the Fourier transform of an input sequence. Since the magnitude of the post-multiplier $e^{-\frac{j\pi n^2}{63}}$ is 1, the magnitude of the complex convolver output is equivalent to the desired result. With the analog multiplier concept a one-chip spectrum analyzer is feasible. The architecture of such a chip is shown in Fig. 22. The chip would contain two premultipliers from which charge packets would be clocked directly into a set of four transversal filters with the magnitude taken externally.

This configuration would be free of post multiplier pattern noise and should provide 1 percent worst case accuracy.

VI. Video Signal Averaging

A very common signal processing function for repetitive waveforms in both radar and communications is a smoothing or averaging operation. The purpose of this procedure is to provide an estimate of a repetitive signal that does not reflect the random noise on any particular waveform specimen, but which can vary slowly in case of signal itself is not exactly repetitive. This function can be implemented recursively so that an exponentially decaying weighting factor multiplies past specimens of the repetitive signal. The recursive filter can be implemented in an analog fashion with a delay line memory whose output is fed back to the input where it is combined with the present sample of the signal waveform.

The attached paper[14] will describe a charge transfer device which overcomes the limitations associated with charge transfer inefficiency and implements a signal averaging function with an electrically programmable time constant on a single chip. Some applications of this device to signal averaging, signal accumulation and multiplexed filtering will also be described.

VII. Acknowledgments

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