

CCD's for Discrete Analog Signal Processing

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I. Introduction

CCD basic building blocks provide a flexible approach to discrete analog signal processing in systems. The Serial-In/Serial-Out (SI/SO) block provides pure time delay, time-base translation, and the possibility of signal encoding with the electrically alterable delay feature of the CCD. The Parallel-In/Serial-Out (PI/SO) block may be used for time-division-multiplexing (TDM) a number of parallel channels into a single serial data stream. In another mode of operation, the PI/SO block may be employed to provide time-delay and integration (TDI) which may be used in sensor-type systems to increase the effective exposure time. The Serial-In/Parallel-Out (SI/PO) block provides a nondestructive readout of tapped, delayed, signals which is suitable for convolution and correlation functions, low-pass and band-pass filters, and adaptive processors. Adaptive signal processing is achieved with electrically reprogrammable analog conductance weights at the tap positions of a SI/PO block. CCD applications are discussed for radar, sonar, speech communication, and medical systems.

II. SI/SO Blocks

A simplification of the CCD analog shift register is shown in Fig. 1. The timing is arranged so the switch toggling frequency is $\frac{1}{2}$ of the 4ϕ clock frequency. Thus, the input switch S_1 alternately samples data and zero reference to provide isolation of signals along the delay line. At the output, switch S_2 clamps during zero reference, samples during data, and holds otherwise. The output holding capacitor contains only the "time-stretched" data samples. In a SI/SO block with N pairs of stages, there will be N signal samples and N zero reference samples, each of duration $\frac{1}{2}T$. Fig. 2 illustrates some key waveforms which are applied to the CCD analog shift register. The waveforms ϕ_1 through ϕ_4 are the 4ϕ clocks which propagate charges down the delay line without dispersion. Waveform S_1 demonstrates the switch function at the input - data is sampled in the "up" position and zero reference

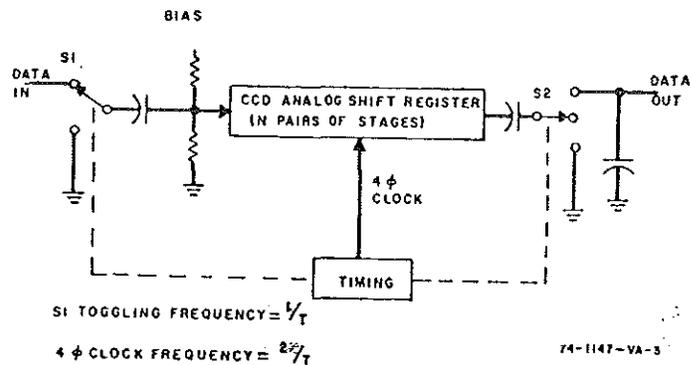


Fig. 1 CCD Analog Shift Register

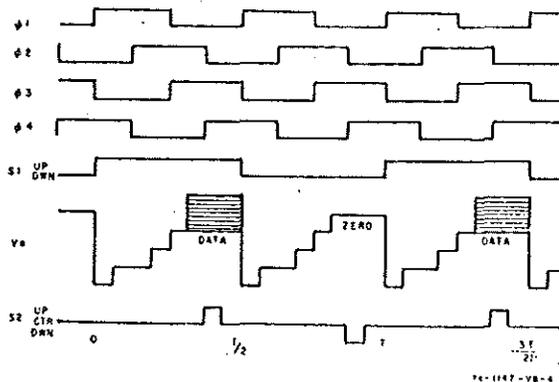


Fig. 2 Basic CCD 4φ Clock Timing

is sampled in the "down" position. S_2 demonstrates the switch function at the output - data is sampled in the "up" position and zero reference is clamped in the "down" position, and the data is held when it is not sampled (i.e. center position). The interval from data sample to data sample is T and the total transport time is NT , where N is the number of pairs of stages. Thus, the signal delay for a SI/SO block is,

$$\tau = NT = N/f_c \quad (1)$$

which illustrates the electrically alterable delay feature of the CCD delay line. Since the Shannon sampling theorem requires the analog signal to be sampled at a rate at least twice the highest frequency component of interest, we may write

$$f_s \leq \frac{1}{2T} = f_s(\text{max.}) \quad (2)$$

and the time-delay-bandwidth product becomes,

$$\tau f_s \leq \frac{1}{2}N \quad (3)$$

The low frequency limit is determined by the thermal leakage accumulation in each stage of the shift register and the upper frequency limit is set by input injection and transfer efficiency considerations - assuming the peripheral analog circuitry and clock waveforms do not limit the performance.

A typical broadband, dynamic range (i.e. pk.-pk. signal/r.m.s. noise) is about 80-100 dB. for present-day devices. The linear dynamic range (i.e. the level at which the 2nd harmonic reaches the system noise level) is about 50-60 dB. for a 1 volt input signal. Clock requirements vary from TTL to MOS drivers, however, to obtain suitable dynamic range and frequency response CMOS-type levels (i.e. 10-18v.) are generally needed. At the present time, CCD require the generation of clocks and timing pulses with off-chip circuitry. In addition, analog clamp/sample and reconstruction circuitry is needed to process the output signals. A number of companies are at work to provide more of these peripheral requirements on the CCD chip. A CCD chip should have protective networks of the resistor-diode or MOS-type to limit the clock displacement currents and charge build-up on the gate electrodes. In operation, the CCD may require some type of pre and post-filter to suppress aliasing due to the sampling operations at the input and output of the CCD. Fig. 3 illustrates an analog output, swept frequency response of a SI/SO block with sample/hold and 7-pole Butterworth filter (-3 dB. at 750 KHz) to filter the clock $f_c = 2$ MHz and limit aliasing of frequencies higher than $\frac{1}{2}f_c$ into baseband.

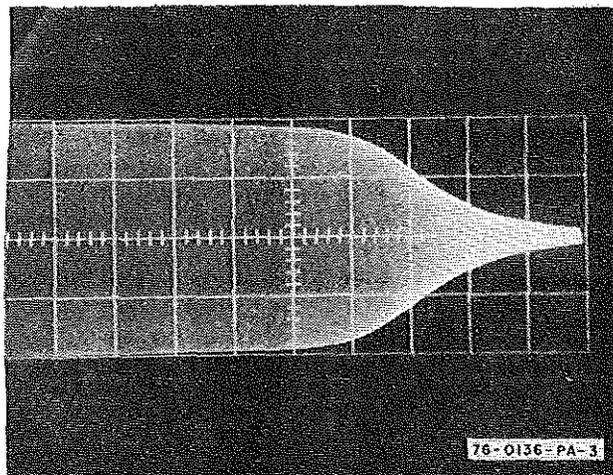


Fig. 3 Frequency Response of Sampled Data
CCD Analog Shift Register (100 KHz/Div.)

There are several techniques to inject signal charge into a SI/SO block and the best method for low harmonic distortion is called the clocked source or "fill" and "spill" technique. Fig. 4 illustrates the method where charge prefills a "well" under the G_2 electrode, followed by scuppering or spilling backwards into the source which has now become a drain. The remaining charge is determined by the difference between the voltages on G_1 and G_2

and a threshold voltage mismatch which can be less than 10mv. for double-polysilicon electrodes over a $\text{Si}_3\text{N}_4/\text{SiO}_2$ dielectric. The input signal charge may be written as,

$$q_s = C_2(V_{G1} - V_{G2} \pm \Delta V_{th}) \quad (4)$$

where C_2 is the effective capacitance under the G_2 electrode.

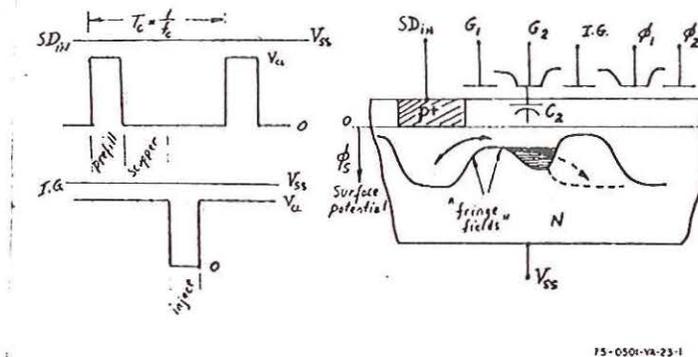


Fig. 4 Charge Injection with the Clocked Source or "fill" and "spill" method.

The transfer function for the CCD at d-c. depends upon whether the signal is applied to the non-inverting electrode G_1 or the inverting electrode G_2 as illustrated in Fig. 5. Analogous with differential/operational amplifiers the CCD provides common-mode rejection which typically may be -80 to -100 dB. for a 1 volt input signal. A preferred configuration for low harmonic distortion is to fix G_1 at a d-c reference potential and apply the input signal to G_2 .

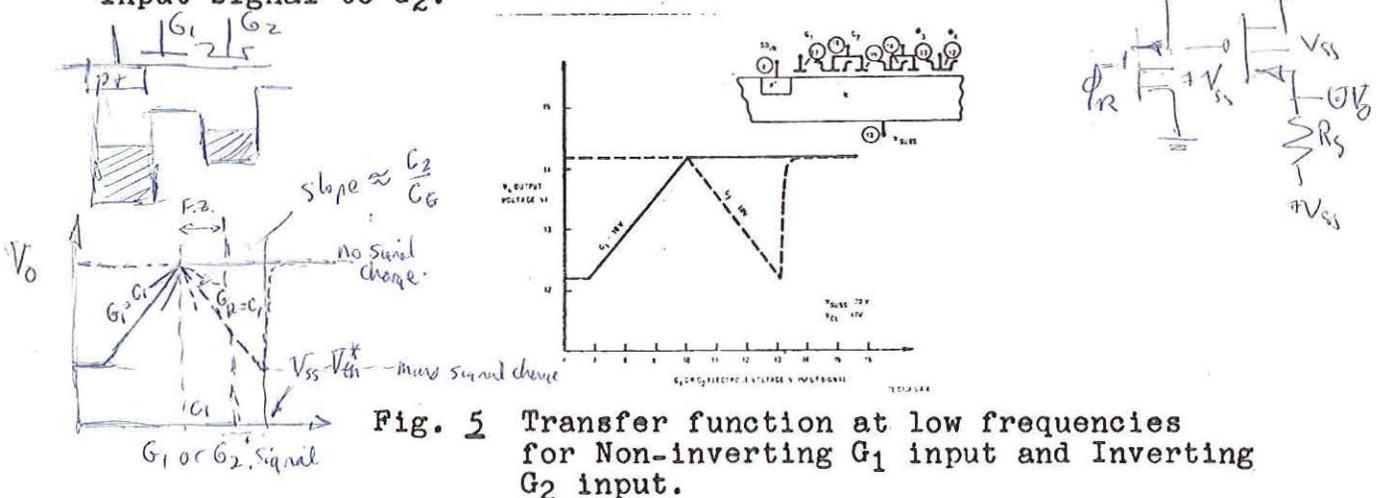
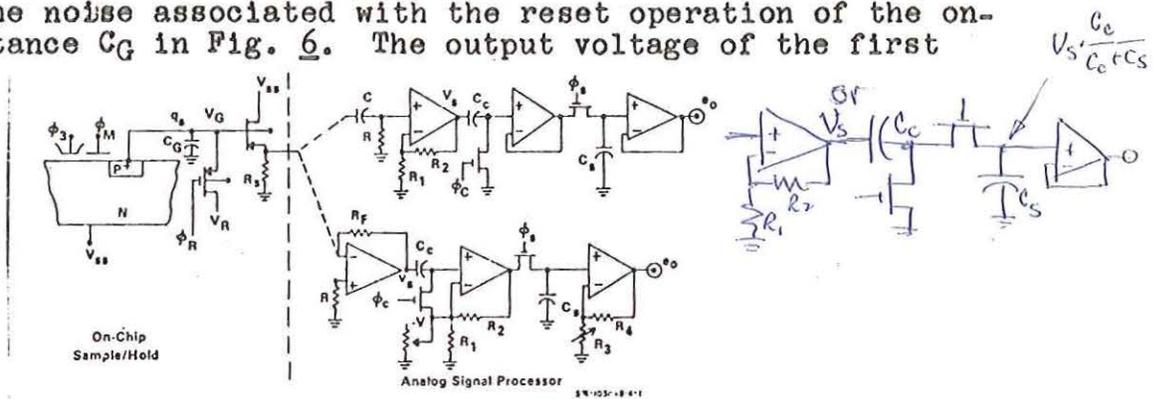


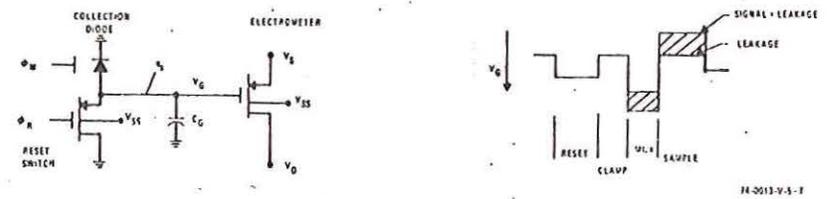
Fig. 5 Transfer function at low frequencies for Non-inverting G_1 input and Inverting G_2 input.

In SI/SO operation the signal is sensed destructively at the output with a reverse-biased diode connected to a gated-charge integrator MOS amplifier. Almost all types of CCD's employ some

form of on-chip gated charge integrator. In effect, this output circuit performs an on-chip sample/hold operation to convert the signal charge to voltage. Fig. 6 illustrates two types of analog reconstruction circuits which are connected to the on-chip gated charge integrator (sometimes called the "precharge and float" technique). Fig. 7 illustrates a set of clock waveforms to insert the signal into the CCD, transport the signal charge with a "push-clock" technique, and perform correlated-double-sampling for analog reconstruction of the output signal. The latter method is required to remove the noise associated with the reset operation of the on-chip capacitance C_G in Fig. 6. The output voltage of the first



(a) Current and Voltage Sensing Circuits for Signal Readout and Reconstruction



(b) Schematic of Output Gated-Charge Integrator to perform on-chip sample/hold function.

Fig. 6 CCD Analog Signal Processor Operation

preamplifier V_s may be written as,

voltage sensing :
$$V_s = \frac{q_s g_m R_s (1 + R_2/R_1)}{C_G (1 + g_m R_s)} \quad (5)$$

current sensing :
$$V_s = \frac{q_s g_m R_F}{C_G}$$

and combining equations (4) and (5) we have the static transfer function of the CCD, neglecting transfer inefficiency losses.

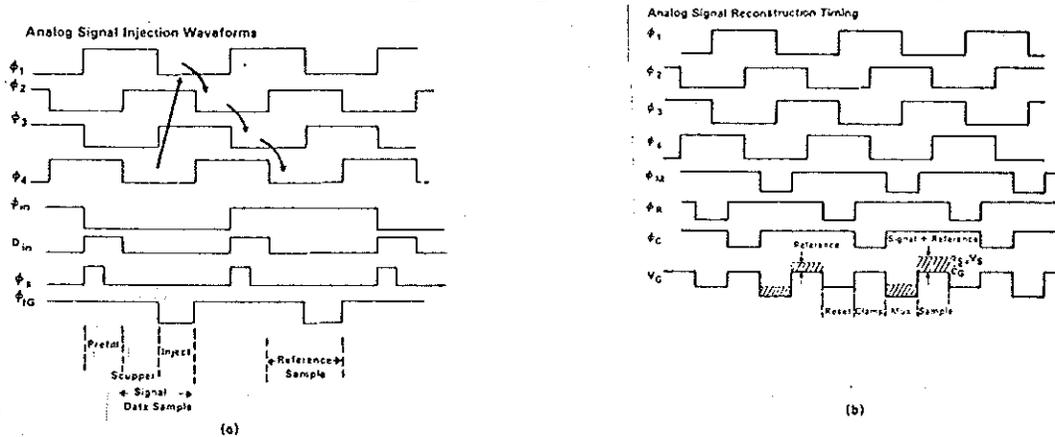


Fig. 7 SI/SO Timing Diagram with Correlated Double Sampling Operation (See Fig. 6)

Applications of SI/SO Blocks

A time multiplexed CCD filter bank is illustrated in the design of a 2-pole recursive filter network as shown in Fig. 8. In this arrangement processing of the data samples $X(Z)$ includes weighting by four constants which determine the gain, center frequency, and bandwidths of the filters. Delays are indicated in Z-transform notation by Z^{-1} and are equivalent to the sampling interval. The relation between the weighting constants and filter parameters is given as,

$$K1 = e^{-\Delta\omega T/2} \cos \left(\left[\omega_0^2 - \left(\frac{\Delta\omega}{2} \right)^2 \right]^{1/2} T \right)$$

$$K2 = e^{-\Delta\omega T} \tag{6}$$

$$L = K1/2$$

and when the zero is selected to be in line with the poles as indicated in Fig. 9 a considerable reduction in hardware results, at the expense of the filter response not being exactly zero at zero frequency. Fig. 10 illustrates the CCD filter bank block

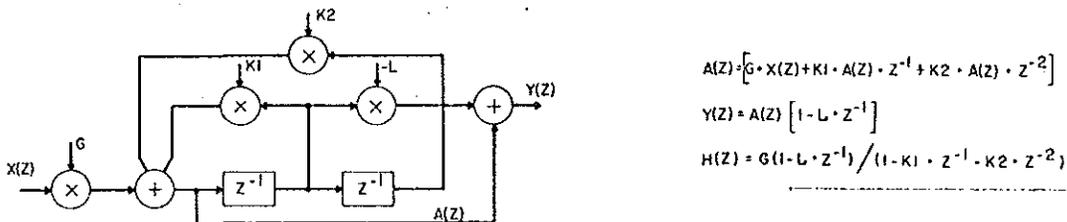


Fig. 8 Basic 2-Pole Recursive Filter

diagram in which the storage and sequencing of the constants is accomplished in a digital manner with programmable read-only-memories (PROM's), although electrically alterable ROM's with MNOS memory transistors could be employed for adaptive filter bank applications. The analog signals are weighted by the filter constants which are obtained by means of 4-quadrant multiplying digital-to-analog converters (MDAC's). The serial output data is demultiplexed onto N lines by the output sampler which stretches each sample to a width $T_s = NT$. Timing circuitry provides the CCD clock waveforms, the PROM addresses, and the sampler address. Fig. 11 illustrates a set of uniform filter characteristics with measured center frequencies to within 1 Hz of design values. The variations of K_1 and K_2 determine the accuracy of center frequency and bandwidth, respectively. Applications of this filter bank

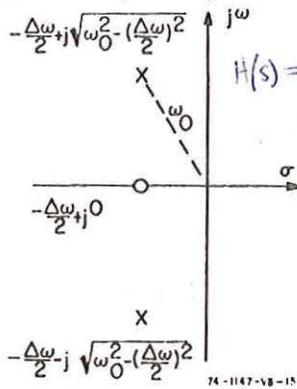


Fig. 9 Pole-Zero locations of Recursive Lerner Filter.

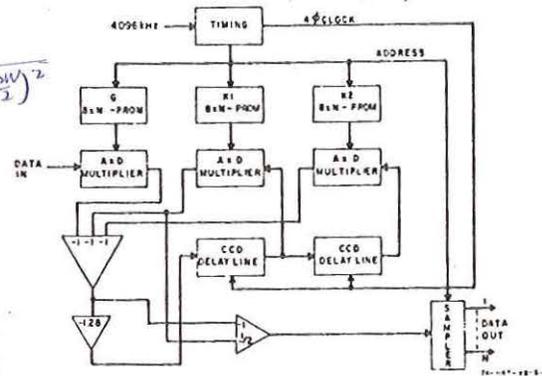


Fig. 10 Block Diagram of CCD Filter Bank with N-Channels.

include Doppler spectrum processing in radar, sonar, and communication systems with advantages of low integrated circuit count and reprogrammable filter parameters.

CENTER FREQUENCY IN HZ	BANDWIDTH IN HZ	G	K1	K2
150	5	1.00	0.75	-0.96
170	5	1.00	0.46	-0.96
190	5	1.00	0.15	-0.96
210	5	1.00	-0.15	-0.96
230	5	1.00	-0.46	-0.96
250	5	1.00	-0.75	-0.96

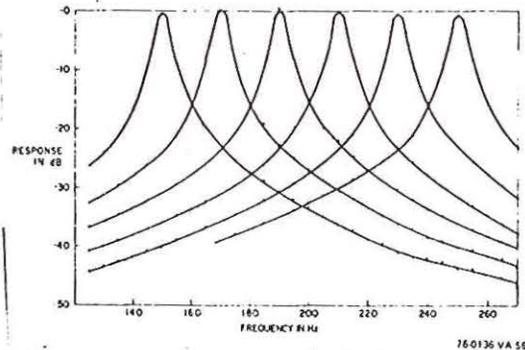


Fig. 11 Uniform Filter Characteristics for Filter Bank of Fig. 10.

In order to prevent overloading of Doppler filter banks by stationary clutter returns and to insure adequate rejection of

the clutter it is necessary to precede the filter with a MTI clutter canceller. The cascaded 2-pulse canceller configuration is best suited for an analog application with CCD's as the accuracy requirements are least for a specified level of performance. For example, in the cascaded canceller a 40 dB. clutter notch results when the individual 2-pulse cancellers have 20 dB. notches. Fig. 12 illustrates a block diagram of a 2-pulse MTI clutter canceller with appropriate sampling and velocity response shaping by positive feedback constant K. Fig. 13 demonstrates the uneven response for the cascaded cancellers without feedback (K = 0) and good uniformity with feedback (K = 0.6). Thus, a 3-pulse MTI clutter canceller may be approximated with a pair of identical cascaded 2-pulse cancellers. To illustrate the effect of a MTI

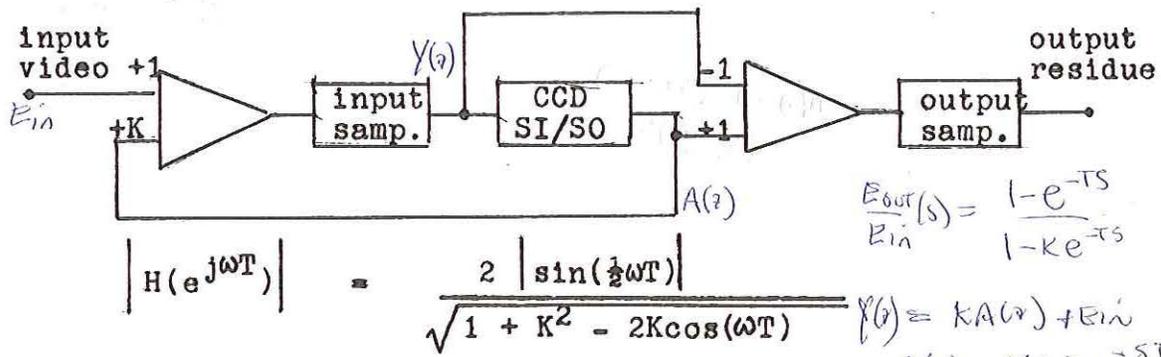


Fig. 12 Block Diagram of 2-pulse MTI Clutter Canceller with Velocity Response Shaping.

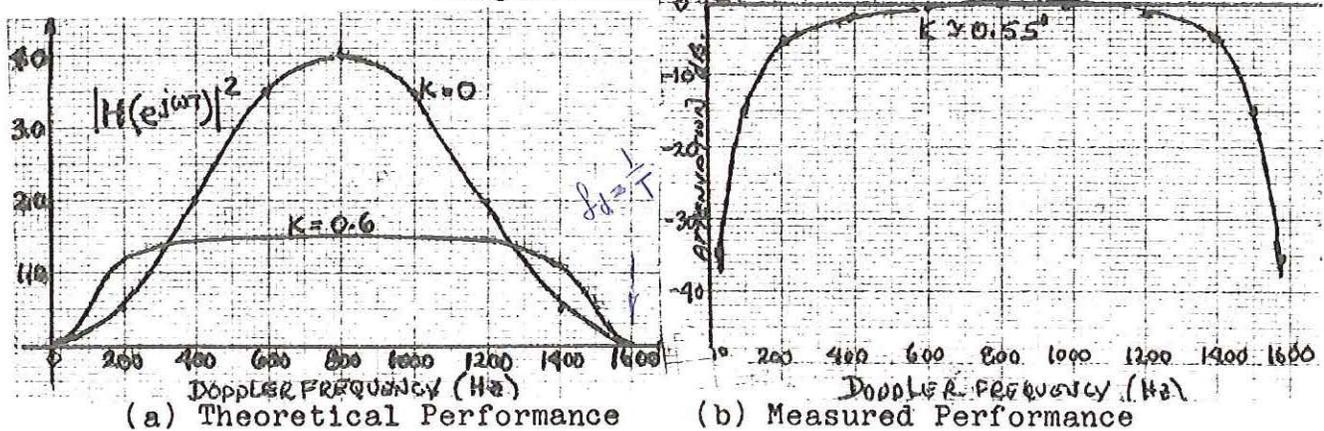


Fig. 13 Response of cascaded 2-pulse cancellers for 3-pulse canceller response.

clutter canceller Fig. 14 shows a PPI display of the unprocessed video (MTI clutter canceller deactivated) and Fig. 15 shows the PPI after activation of the MTI clutter canceller and a single

scan. The display is essentially free from noise and clutter with differences in target strength appearing as a persistence in the display.

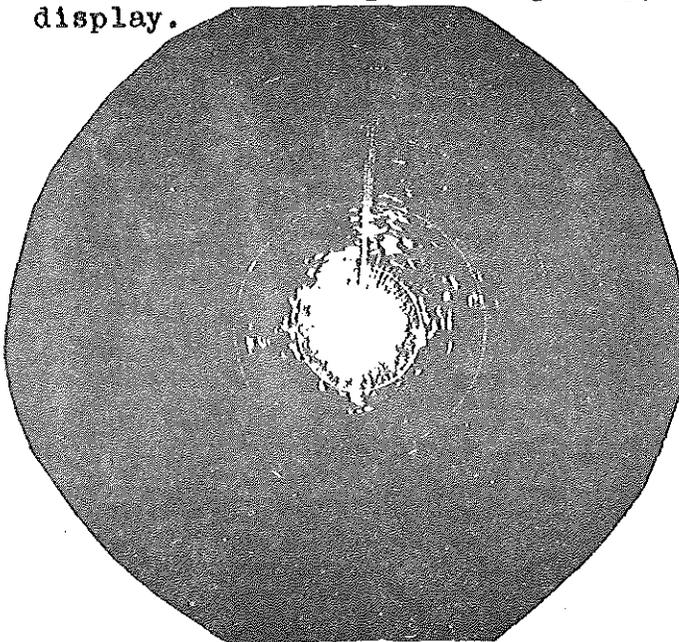


Fig. 14 Unprocessed Video
(MTI clutter canceller is deactivated)

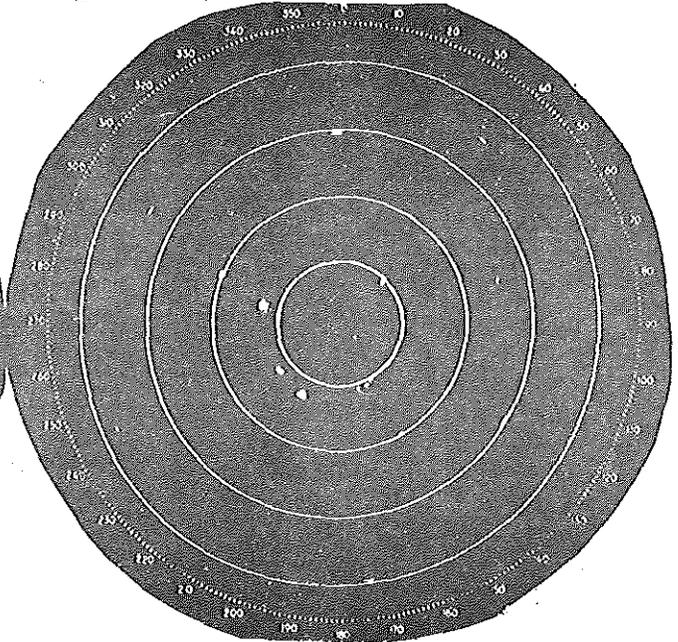


Fig. 15 MTI Clutter Cancellor
activated to provide noise-less display.

II. PI/SO Blocks

The Parallel-In/Serial-Out (PI/SO) block is a particular configuration of the family of CCD basic building blocks shown in Fig. 16. The PI/SO block may be used to time-division-multiplex a number of low data rate signal channels into a high data rate output channel. Fig. 17 illustrates a schematic representation of the CCD block used as a TDM signal processor. The insertion

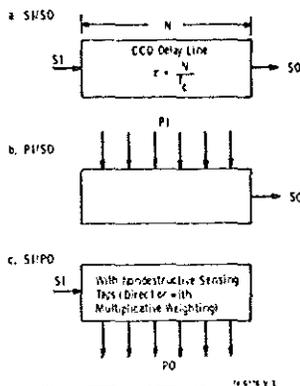


Fig. 16 CCD Basic Blocks

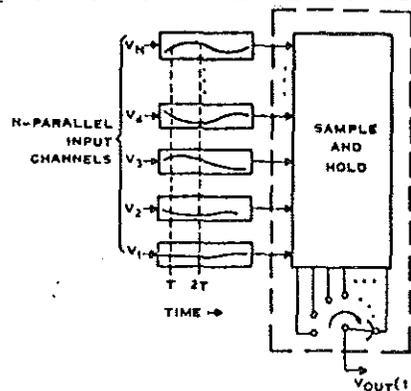


Fig. 17 TDM operation of PI/SO

of a zero reference into each parallel channel, similar to the discussion with the SI/SO block, permits removal of threshold voltage variations from channel to channel. Gain variations due to input capacitance cannot be removed. In order to handle the signal charge which increases along the SI/SO portion of the PI/SO block, the channel must be widened progressively towards the output detection diode. In addition, there is interaction between the output channel (i.e. the SI/SO portion of the PI/SO block) and the input channels. Thus, an alternative solution to "turning the corner" is to use a number of parallel SI/SO blocks of progressively different delays. This difference is illustrated in Fig. 18. An important advantage of this latter approach is the elimination of the corner-turn which becomes difficult as the output diode is approached since the channel widens. The corner-turn reduces quite drastically the transfer efficiency and increases the inter-channel cross-talk.

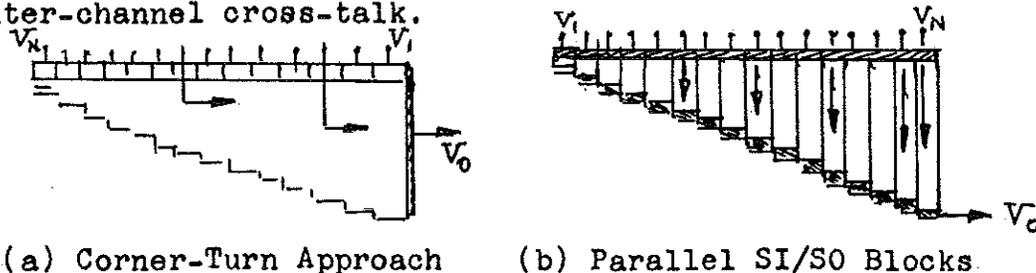


Fig. 18 PI/SO Configurations

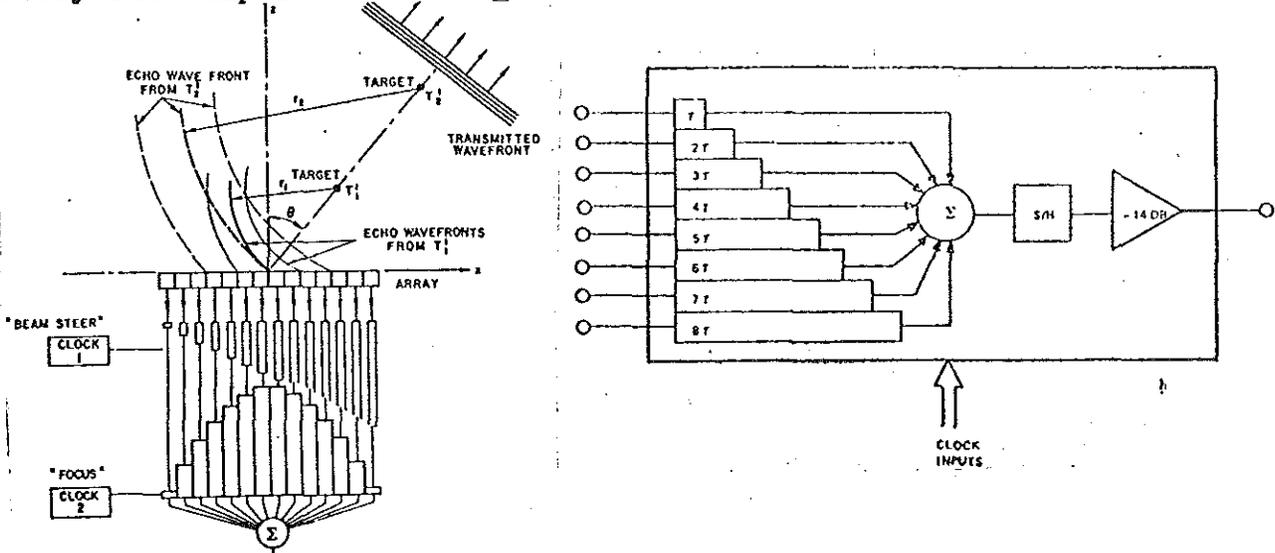
Sonar Applications

The ability to handle a number of parallel channels is an important feature of the PI/SO block. Sonar beamforming, steering and focusing can be accomplished with the PI/SO block. Fig. 19 illustrates the basic concepts of dynamic focussing and beam steering with a PI/SO block. The transmitted wavefront impinges upon the transducer (hydrophones) array which generates a sequence of electrical signals. This sequence is injected into a linear array of CCD's of the configuration shown in Fig. 18(b). The PI/SO block is clocked at a rate sufficiently high to insure adequate phase quantization along the wavefront. The electrical delay in a SI/SO column is adjusted to match the acoustical delay in the water. Thus, we may write

$$\frac{m d \sin \theta}{V_s} = N / f_c \quad (7)$$

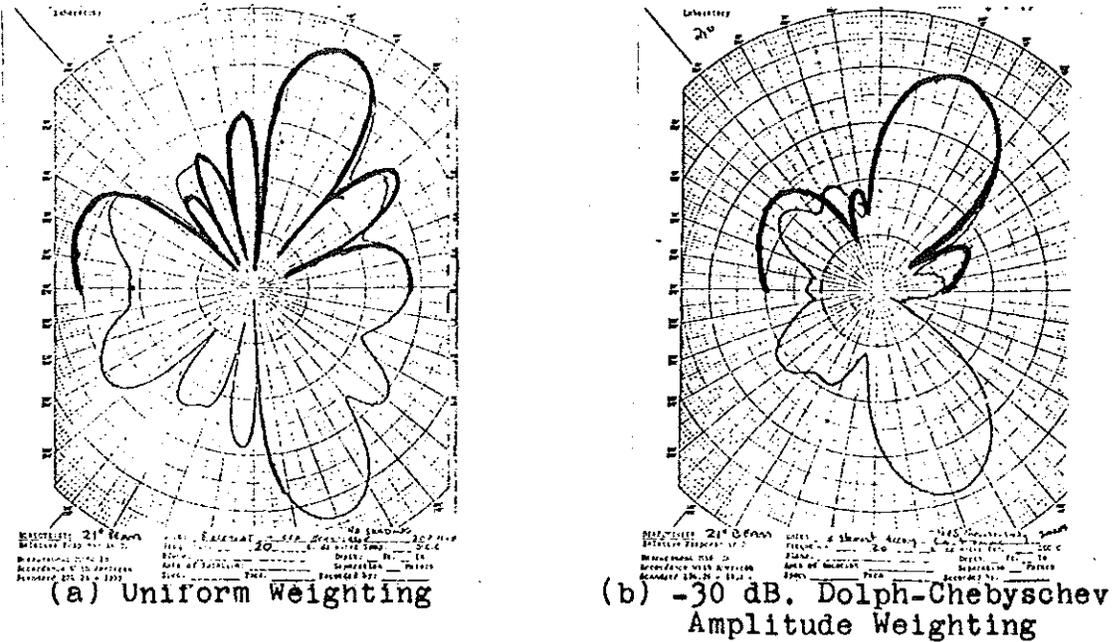
where m = the position of the SI/SO column, d = spacing of the hydrophone transducer elements, V_s the velocity of sound in water, and N the number of stages in the m^{th} column. Fig. 20 illustrates a beam pattern at $\theta = 21^\circ$ formed with 8 columns (i.e. m varies from 1 through 8) clocked at $f_c = 200$ KHz and an element spacing of $d = 1.25$ ". Fig. 20(a) represents the beam pattern without amplitude shading (i.e. all 8 transducer inputs are equally weighted)

and Fig. 20(b) represents the beam pattern with -30 dB. of Dolph-Chebyshev amplitude shading.



(a) Dynamic Focussing and Steering (b) 8-element CCD array

Fig. 19 CCD Sonar Beam Forming



(a) Uniform Weighting

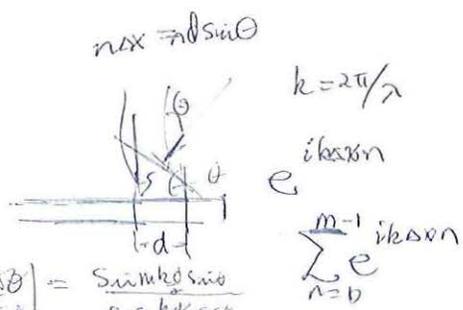
(b) -30 dB. Dolph-Chebyshev Amplitude Weighting

Fig. 20 CCD Beam Forming with an 8-element transducer array (transmit frequency $f_s = 20$ KHz)

$$\frac{I(\theta)}{I(0)} = \frac{\sum_{n=0}^{m-1} e^{ikd n \sin \theta}}{m \sum_{n=0}^{m-1} 1}$$

$$\sum_{n=0}^{m-1} e^{ikd n \sin \theta} = \frac{1 - e^{ikd m \sin \theta}}{1 - e^{ikd \sin \theta}}$$

$$|I(\theta)| = \left| \frac{e^{i \frac{k d m \sin \theta}{2}} \frac{\sin \frac{1}{2} m k d \sin \theta}{\sin \frac{1}{2} k d \sin \theta}}{e^{i \frac{k d \sin \theta}{2}} \frac{\sin \frac{1}{2} k d \sin \theta}{\sin \frac{1}{2} k d \sin \theta}} \right| = \frac{\sin \frac{1}{2} m k d \sin \theta}{\sin \frac{1}{2} k d \sin \theta}$$



The sonar beamformer array operates in the time-delay and integrate (TDI) mode in which the individual inputs are delayed and added to form the output signal. In essence, the beamformer performs a correlation function since all the inputs add coherently in the "look" direction θ . The result is as though the entire array of transducers were rotated by θ in the direction of the acoustic source. Fig. 18 illustrates the performance of a linear array of transducers, however, beams may be formed in 2-D and 3-D with suitable combinations of delays. If we consider a linear array with uniform amplitude weighting to the beamformer, then the theoretical response of the array is

uniform weights: $\frac{I(\theta)}{I(0)} = 20 \log_{10} \left[\frac{\sin(\frac{1}{2} m k d \sin \theta)}{m \sin(\frac{1}{2} k d \sin \theta)} \right]$ (8)

where $k = 2\pi/\lambda$ and $\lambda = f_s/V_s$ is the wavelength of the sound. The transducer array is basically a sampling array to reconstruct the acoustical field and the choice of transducer spacing is determined by sampling theorem, thus, $d = \frac{1}{2} \lambda$. The heavy solid lines in Fig 20 are the theoretical responses and the light lines are the chart recorder outputs. The non-isotropic radiator characteristics of the hydrophones cause low-level differences between theoretical and experimental curves. The side-lobes may be tapered or shaded with the Dolph-Chebyshev (Tschebyscheff) method which (1) for a specified beam-width gives the lowest possible side-lobe levels and (2) for a specified set of side-lobes relative to the main beam, gives the narrowest beam-width.

In general, most sonars are designed to receive signals from the "far-field" (i.e. they assume the signal wave front is a plane). This is a good assumption if the sound comes from a range $R > L^2/\lambda$, where L is length or diameter of the sonar array; however, in some high-resolution sonars beam-widths of 0.1° may be formed. In these cases the transducer array is shaped in mechanical arcs to match the wave front or in more sophisticated systems the signals are electronically phase-shifted along the receive line to focus the receiver on the range of interest. The focus is variable and it sweeps with time, matching the speed of sound as the transmit ping travels out through the water. Phase-shifting may be used in single frequency systems (i.e. the sonar actively transmits a ping of a single frequency), whereas, passive listening sonars are best implemented with delay lines since the delay required to form a beam in a given direction is the same for all frequencies. An electronically variable focus would be important for high resolution forward-look sonars with delay lines to form the beams, since phase-shifting results in range resolution degradation. This is because a ping returning from $\theta = 30^\circ$ off the axis of the transducer would have a length equivalent to the transmitted ping, and there would be several range cells of resolution variation across the array. Since the arriving wave fronts are spherical, the CCD's must correct the straight-line transducer array to match the spherical wave front. This may be accomplished with

a parabolic approximation in which the input taps are spaced in a quadratic arrangement as illustrated in Fig. 19(a). The focus clock controls the curvature of the quadratic delays to complement the curvature of the spherical wavefronts from targets T_1 and T_2 . The focus is swept with time by varying the clock speed which steps the signals through the CCD's. This requires a linear FM ramp (chirp) which sweeps, for example, from 500 KHz at 10% range to 5 MHz at 100% range. Although the previous discussion emphasized sonar signal processing, these techniques may be used in any applications where appreciable signal delay occurs in the medium and signal distortion is present. For example, ultrasonic imaging systems for medical research and acoustical imaging for seismology and earthquake engineering, including geological exploration for natural resources.

III. SI/PO Blocks

The SI/PO block features, independent, nondestructive, low-impedance voltage readouts of the analog signals at specified locations or taps corresponding to various delays through the CCD shift register. This block may be used to provide variable tapped delay or combined with weights positioned at each tap it offers the functions of filtering, correlation and convolution. Thus, the SI/PO block serves as a transversal filter where the signal voltage at each tap can be multiplicatively weighted with a conductance to give a current proportional to the product of the signal voltage and the weighting conductance. Summation of these product currents provides the various functions discussed. Fig. 21 illustrates the use of SI/PO and PI/SO blocks to obtain the basic filter expression for the output voltage in terms of a weighted, and delayed summation of the input signal voltage. The

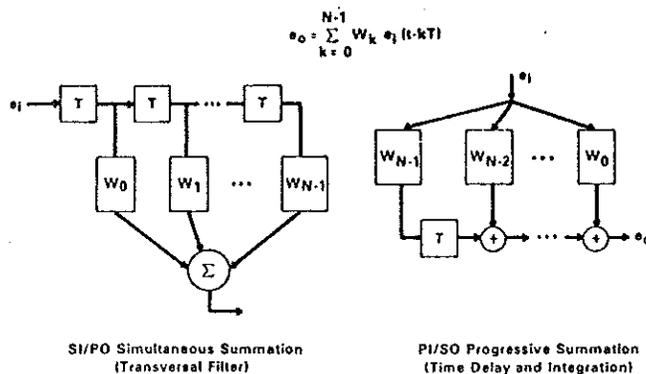


Fig. 21 Comparison of SI/PO and PI/SO Filter Methods

SI/PO block uses a simultaneous summation of delayed input signals which involve nondestructive tapping, amplification, and buffering at each tap position. The PI/SO block operates in the TDI mode

with the weighting performed prior to insertion of the signal into the array. The progressive summation described in Fig. 21 refers to the corner-turn approach shown in Fig. 18(a). The output of the SI/PO block may be expressed as a convolution of the tap weights with the input signal,

$$e_o(t) = \sum_{k=0}^{N-1} W_k e_i(t - kT) \quad (9)$$

where $t=mT$ corresponds to a discrete time index. To find the frequency response we let

$$e_i(mT-kT) = \exp [j2\pi(m-k)U/N] \quad (10)$$

where $U = NTf_s$ is the normalized frequency and f_s is the signal frequency. Insertion of equation (10) into (9) yields,

$$|e_o(U)|^2 = |W(U)|^2 = \left| \sum_{k=0}^{N-1} W_k \exp [-j2\pi kU/N] \right|^2 \quad (11)$$

where $W(U)$ is the discrete Fourier Transform (DFT) of the tap weights W_k .

The transversal filter may be used to synthesize, in principle, any linear function. In general, the input signal, tap weights, and signal output are complex functions of frequency. Low and high-pass filters as well as band-pass and band-stop filters may be synthesized. The tap weights for former are real so inphase and quadrature signal channels can be independent, whereas, the tap weights for the latter are complex and this requires "cross-coupling" between the inphase and quadrature signal channels. The bandwidths and center frequencies are normalized to the unit delay T and a given filter may be scaled from one center frequency and bandwidth to another by simply changing T . Thus, it follows the center frequency and bandwidth are limited by the minimum and maximum values of T . These filters have a linear phase versus frequency characteristic provided the tap weights have conjugate symmetry about the center tap of the weighting array. Thus, in a transversal filter we can exercise independent control over the amplitude and phase characteristics of the transfer function. In addition to the filter function described above, the correlation and convolution operations may be performed as indicated in Fig. 22 and described by the mathematical expressions,

$$\text{discrete convolution: } f * h = \sum_{k=0}^{N-1} W_k f_k h_{m-k} \quad (12)$$

$$\text{discrete correlation: } \phi_{fg} = \sum_{k=0}^{N-1} W_k f_k g_{m+k} \quad (13)$$

If we select the weights W_k to be uniform, such as with the design of identical MOS transistor triode multipliers, then equations (12) and (13) become the discrete convolution and correlation of two input signals. In practice, a major difficulty is the removal of d-c off-sets in the individual MOS multipliers which requires sequential operation of both SI/PO blocks and the insertion of zero reference signals. In addition, some thought must be given to the clock timing and off-chip analog reconstruction in order to obtain "true" 4-quadrant analog multiplication.

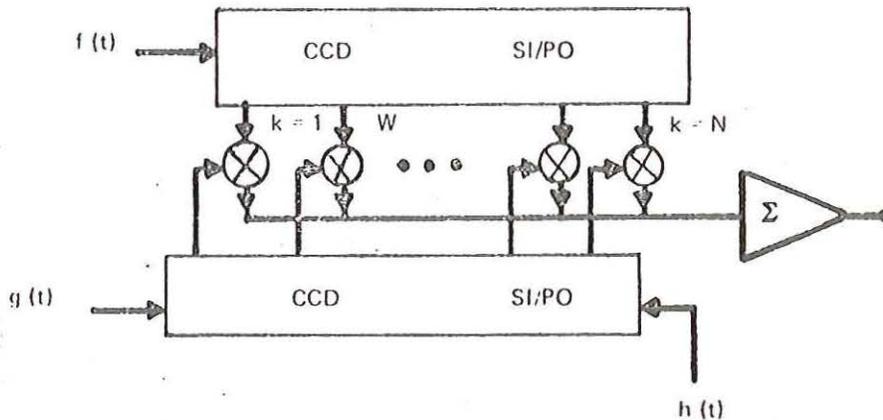


Fig. 22 SI/PO operation for Discrete Convolution and Correlation

The split-electrode weighting technique can provide accurate analog weighting for each tap position of the SI/PO block; however, the tap weight is fixed for a given design and limited to filter design. A technique, which has been applied to CCD structures to sense the analog signal in a nondestructive manner, is called the floating clock electrode sensor shown in Fig. 23. The analog signal charge is sensed, in the form of displacement current, as

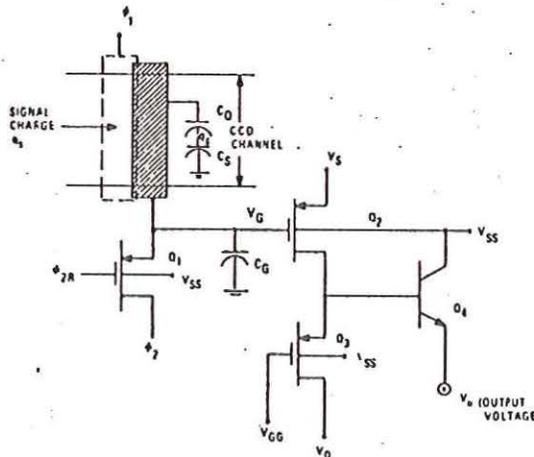


Fig. 23 Floating Clock Electrode Sensor

$$q_s = C_i V_i$$

$$V_G = \frac{\left(\frac{q_s}{C_s}\right) \cdot \frac{1}{C_o}}{\frac{1}{C_o} + \frac{1}{C_s} + \frac{1}{C_o}} = \frac{q_s C_o}{C_o(C_s + C_o) + C_s C_o}$$

$$V_o = q_m R_L V_G$$

$$= \frac{q_m R_L q_s C_o}{C_o(C_s + C_o) + C_s C_o}$$

$$\frac{V_o}{V_i} = \frac{q_m R_L C_i C_o}{C_o(C_s + C_o) + C_s C_o}$$

it passes beneath the floating clock electrode ϕ_2 and converted to a voltage drive by the bipolar emitter-follower. The circuit shown in Fig. 23 is a monolithic construction at each tap point of the SI/PO block. The low output impedance of the emitter-follower at low current levels is highly desirable from the viewpoint of minimizing distortion and inter-tap cross-talk while permitting low power dissipation operation of the SI/PO block. Fig. 24 illustrates a representative clock timing diagram for the SI/PO operation as well as a photomicrograph of a tap point in the SI/PO monolithic I.C. circuit. The clock waveforms are derived

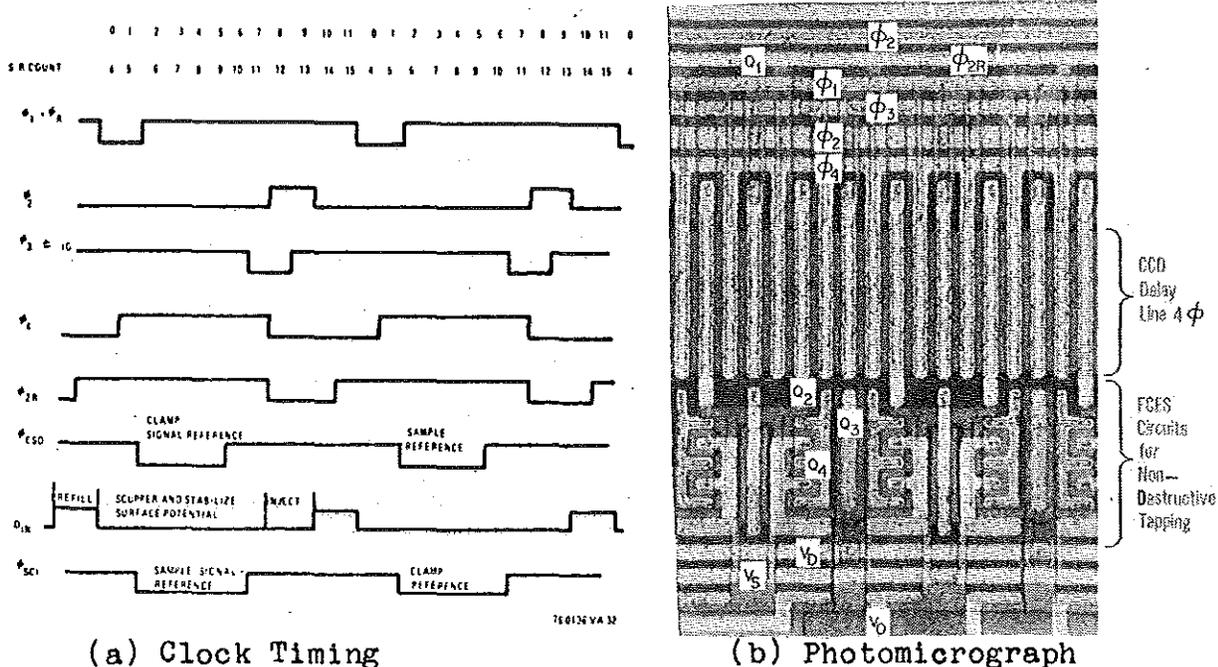


Fig. 24 SI/PO Block Operation and Construction (MOS/bipolar Output Ckt.)

from a divide by 12 countdown to contain the signal charge under the ϕ_2 electrode; however, a divide by 8 countdown may be used if the charge is shared between ϕ_1 and ϕ_2 during sampling.

SI/PO Transversal Filters

The SI/PO block described in Figs. 23 and 24 may be used with fixed, precision, resistors to realize various filter responses. The linear dynamic range is determined by the total harmonic distortion a signal incurs in passage through the SI/PO block. A fixed resistor may be inserted between the emitter in Fig. 23 and the summing node of an operational amplifier to determine the harmonic distortion for a specified input level to the SI/PO block. Fig. 25 illustrates the spectral components observed for a signal frequency $f_s = 1\text{KHz}$ of amplitude 1 volt

pk.-pk. applied to the input of the SI/PO block. With the bias levels used in this measurement the output signal of the bipolar emitter was approximately 0.25 volts pk.-pk.. The input signal was oversampled at a 25 KHz rate and a comparison made between a fixed resistor of $5K\Omega$ and a voltage-controlled MOS transistor whose conductance was adjusted in the triode-region to be about $5K\Omega$. A favorable comparison exists when the signal applied to the drain of the MOS triode multiplier is small, i.e. a -54 dB. 3rd harmonic distortion for the fixed resistor versus a -46 dB. 2nd harmonic distortion for the MOS triode multiplier. In addition, a standby d-c current must be re-directed from the MOS triode multiplier through a "bleed" resistance in order to maintain the operation of the device near $V_{DS} = 0$, where low harmonic distortion is achieved.

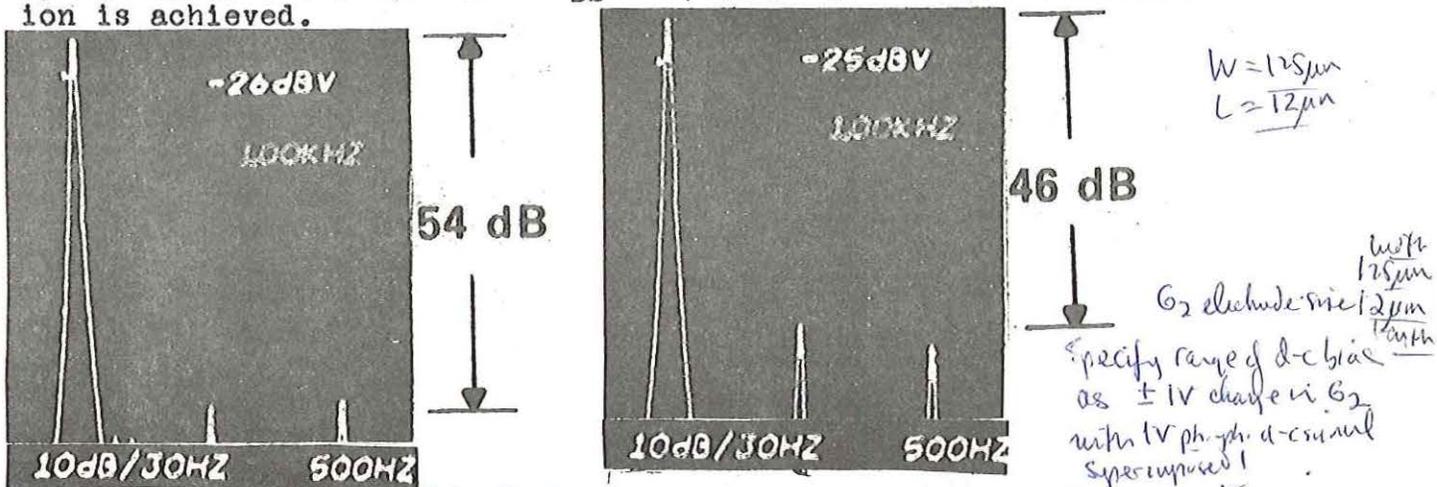


Fig. 25 Comparison of fixed resistor weight with MOS triode multiplier weight. ($e_o = 0.25$ v., $f_s = 1$ KHz, $f_c = 50$ KHz)

In order to evaluate the transversal filter we may select W_k as described in equation (11). Fig. 26 illustrates the frequency response obtained for Uniform and Hamming weights attached to a 20-tap SI/PO block. Thus, the resistor values are selected according to the following expressions,

$$\text{Uniform weights: } R_k = R_o/W_k \quad W_k = 1.0 \quad (14)$$

$$\text{Hamming weights: } W_k = 0.54 - 0.46 \cos \frac{2\pi(k-1)}{N-1}$$

where R_o is the minimum resistance value in the tap array. The index k denotes the tap position and varies from 1 through N . Fig. 26(a) indicates a first side-lobe of 13.2 dB. below the peak in good agreement with the theoretical value of 13.3 dB. for 20 taps in a Uniformly weighted array. Fig. 26(b) indicates a sidelobe suppression of -41.5 dB. in agreement with a predicted value of -41.6 dB. for 20 taps in a Hamming weighted array.

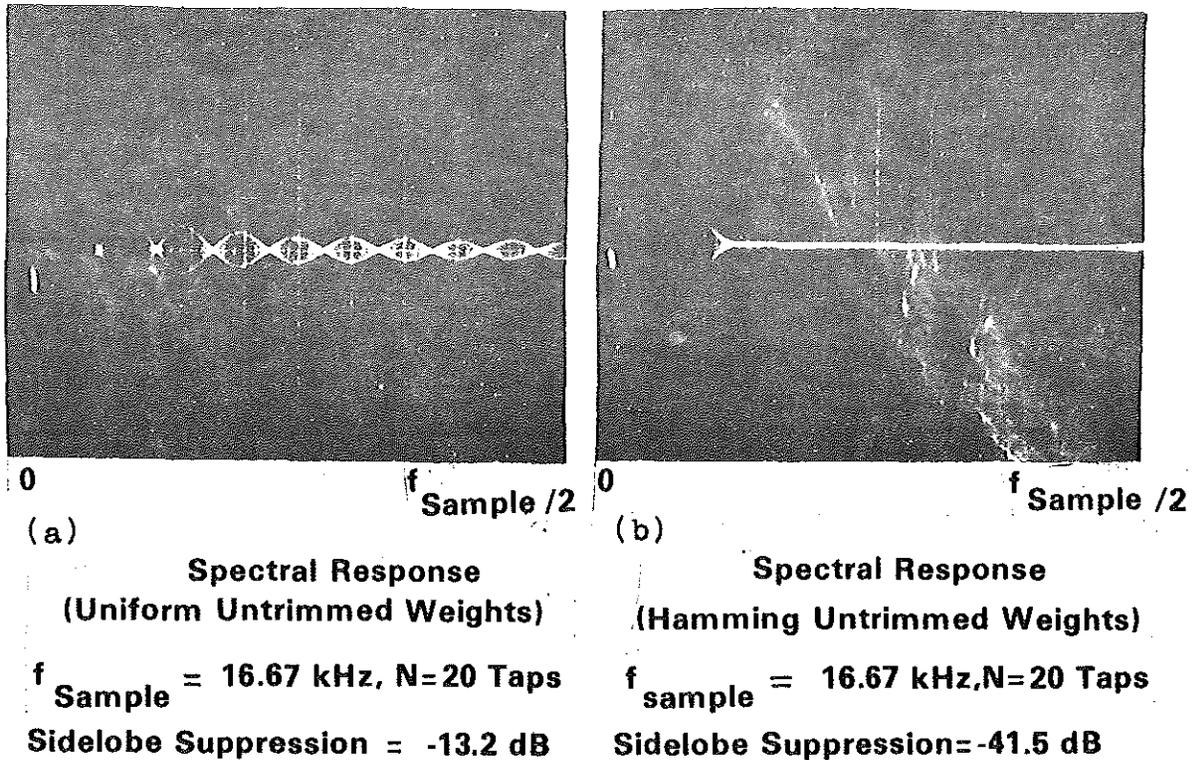


Fig. 26 Transversal Low-Pass Filter Responses for Fixed Resistor Weights on a 20-tap SI/PO Block

IV. CCD Adaptive Signal Processing with SI/PO Blocks

The combination of SI/PO blocks with electrically reprogrammable analog conductances can form a basic linear combiner which is the first step in the realization of an adaptive linear filter. The SI/PO block has already been described in the previous section and the use of MOS transistors as voltage-controlled analog conductances has also been mentioned. The conductance of a MOS transistor in the triode region is,

$$g_{DS} = \frac{\mu W}{L} C_o (V_{GS} - V_{th}) \quad (15)$$

where μ is the effective carrier mobility, W =width and L =length of channel region, C_o is the effective dielectric capacitance per unit area, V_{GS} the applied read voltage between gate and source, and V_{th} the threshold voltage of the device. One method to change the conductance is to alter the V_{GS} for a fixed V_{th} structure, whereas, another approach is to vary the V_{th} for a

fixed read voltage. This latter approach will be described with the use of a metal-nitride-oxide-silicon (MNOS) electrically reprogrammable analog conductance. The MNOS memory transistor is a thin-oxide tunneling structure which responds to erase/write programming voltages with a change in threshold voltage ΔV_{th} . Once the conductance is altered it will drift very slowly with a change of 0.1-0.5%/decade of time. Thus, the MNOS analog conductance provides long-term storage or integration as well as linear multiplication.

Fig. 27 illustrates an adaptive linear combiner and the simplified version of the adaptive transversal filter. The signals $X_1 \dots X_N$ are provided by the tapped CCD analog delay line, which we have called the SI/PO block and the adjustable weights $W_1 \dots W_N$ are the electrically reprogrammable MNOS analog conductance multipliers. The weights are adjusted according to the clipped-data least-mean-square (LMS) error algorithm which is a recursive algorithm to solve for the optimal weight vector. The LMS algorithm offers a real-time solution to the classical Wiener-Hopf equation without the need for a priori information on the statistics of the input signals or the need to invert an $N \times N$ covariance matrix and perform $N(N+1)/2$ auto and cross correlation measurements. The algorithm may be written as,

$$W_k(m+1) = W_k(m) + 2\mu \epsilon(m) \text{sgn} [X(m-k)] \quad (16)$$

where the subscript "k" refers to the kth tap, m = clock index, μ = convergence constant, $\epsilon(m) = d(m) - y(m)$ the difference between the desired and output signals, and

$$\begin{aligned} \text{sgn} [X(m-k)] &= +1 \quad \text{for } X(m-k) \geq 0 \\ &= -1 \quad \text{for } X(m-k) < 0 \end{aligned} \quad (17)$$

The implementation of this algorithm does not require the linear multiplication of (m) and $X(m-k)$ as in the original formulation of the LMS algorithm, but instead, a pair of switches to steer the quantity $2\mu|\epsilon(m)|$ to the proper terminals of the MNOS triode multipliers. Fig. 28 illustrates a schematic diagram of the CCD analog delay line and MNOS transistor implementation of the

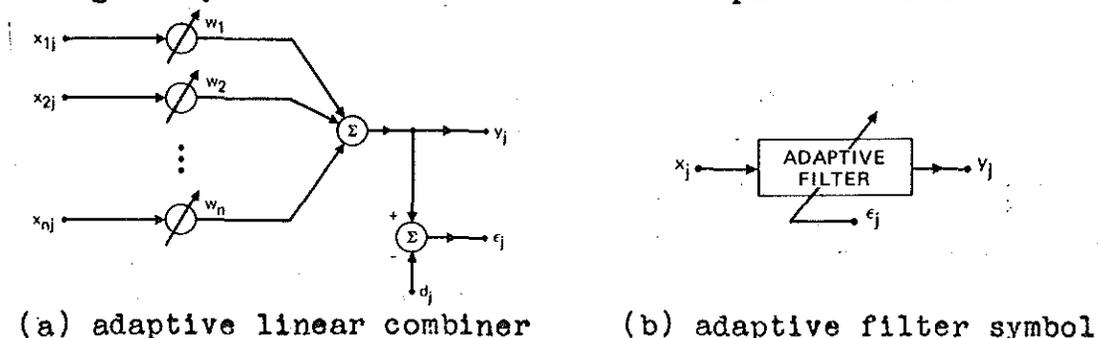


Fig. 27 Adaptive Linear Filter

adaptive filter with the clipped-data LMS algorithm of equation (16). In essence, the algorithm performs a cross-correlation between the error and the polarity of the tapped signal at each tap position until the error sequence is orthogonal to the data sequence. At this point the incremental adjustments to the MNOS weight average to zero over a cycle of the input data (i.e. no further adjustment of the weights is necessary and the weights are optimized in the mean-square sense). Thus, the adaptive filter is a practical exercise in least-squares estimation and amounts to the implementation of the orthogonality principle in N-dimensions, where N is the number of taps.

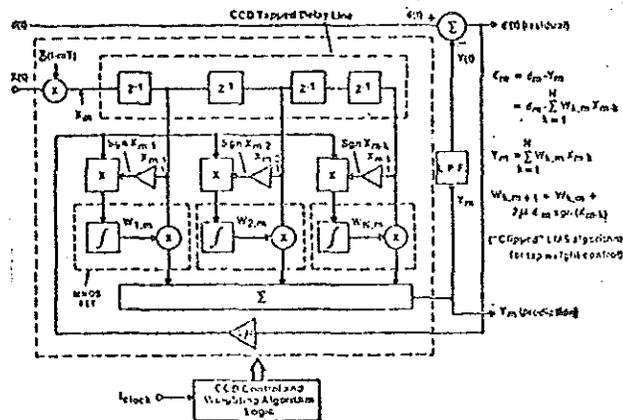


Fig. 28 Block Diagram of Clipped-Data LMS Adaptive Filter/Predictor

Adaptive Filter Applications

There are numerous applications for the adaptive filter described in Fig. 28. Perhaps one of the most useful is in the area of adaptive noise cancellation. In this application the desired signal consists of the signal to be extracted and the interference, whereas, the input signal (reference) to the filter is the interference. For example, the desired signal might be the ECG signal + 60 Hz interference in electrocardiography and the reference signal is obtained from the "wall-plug" outlet. In the case of a single frequency interference we only need 2 taps to correct for the phase of the interfering signal. Fig. 29 illustrates an experiment with a signal to be extracted at 50 Hz corrupted by a 250 Hz signal. Prior to adaptation, the signal to be extracted lies 16 dB. below the interfering signal, whereas, after adaptation the signal to be extracted is 16 dB. above the interfering signal. Thus, the interference has been rejected by 32 dB. with this adaptive notch filter. The sampling rate in this example is adjusted to provide a 90° phase shift between the two tap positions at the reference signal frequency. An advantage of the adaptive notch filter is if the interference signal drifts with time, then the notch will track because the reference

signal is the filter input. Other applications in noise cancellation are removal of aircraft noise in pilot's cabin, noise in speech communication systems, hearing-aids for the deaf, and the general area of separating broadband and periodic signals. The latter is accomplished with the insertion of delay in the reference path, which decorrelates the broadband components in the reference path from the desired or primary path; however, the periodic or narrowband components will remain correlated between the two paths. Thus, the filter output represents the periodic or narrowband components and the error represents the broadband components. This is illustrated in Fig. 30. The use of this method is excellent when no external reference input is available such as speech or music playback in the presence of tape hum or turn-table rumble. Other applications include the rejection of jamming signals in spread-spectrum communications and the enhancement of low-level signals buried in broadband noise.

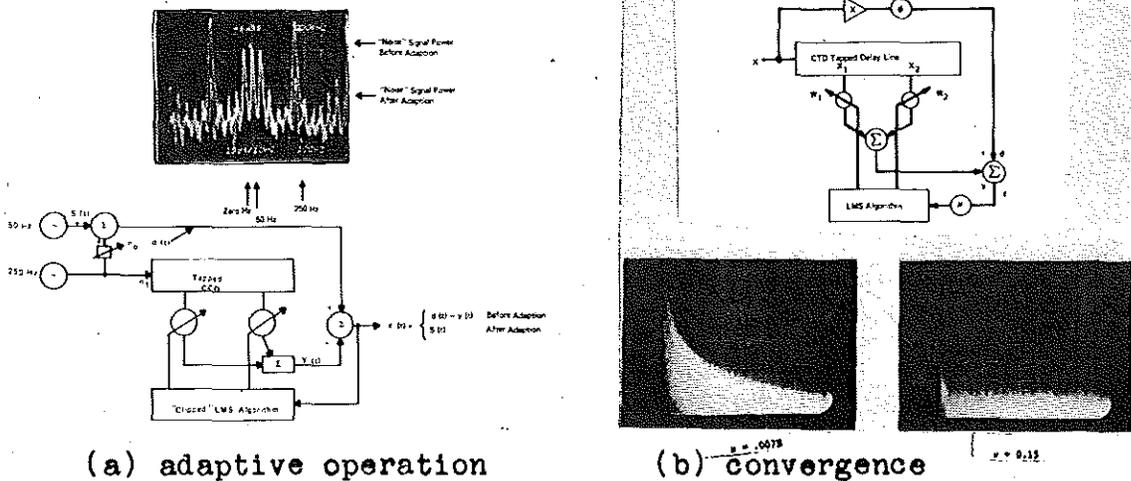


Fig. 29 Adaptive Noise Cancellation with 2-tap CCD/MNOS Clipped Data LMS Algorithm

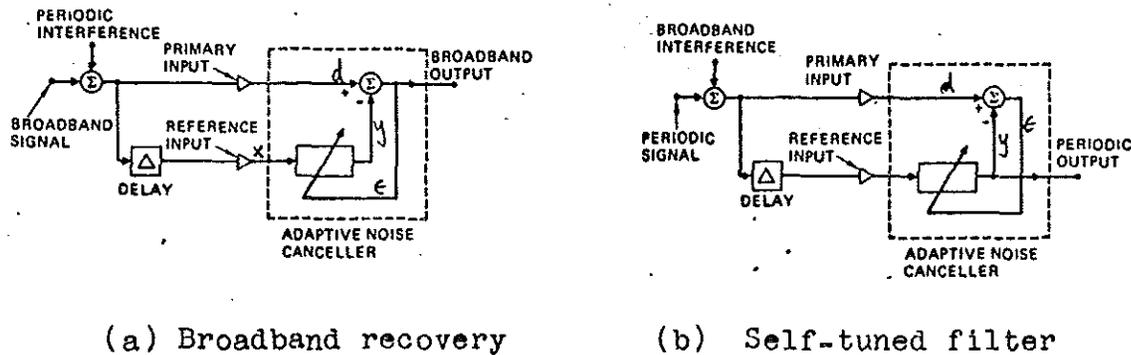


Fig. 30 Separation of Broadband and Periodic Signal Components

A promising area for CCD adaptive filtering is in speech processing where redundancy in the spoken word has long been recognized by researchers. Electrical processing of speech which takes this into account can reduce substantially the bandwidth required for speech transmission. If speech is sampled and quantized at 56 Kbits/sec (7 bits at 8K samples/sec) for acceptable fidelity and the channel bandwidth restricts the transmission to below 4 Kbits/sec, then a speech compression ratio of approximately 15:1 is attempted. In order to realize this ratio we must extract and encode key parameters which represent the speech samples. If we examine the block diagram of Fig. 28 with the inputs $x(t)$ and $d(t)$ connected together, then the resultant processor becomes a linear predictor with the optimal weights referred to as the prediction coefficients. These coefficients characterize the vocal tract resonances when the input is the sampled speech waveform and 10-12 weights are sufficient to describe or analyze the speech sample over a 20 msec frame time. In this frame time several hundred speech samples are examined and there results a set of redundant equations for the weights which is solved with the method of least squares. Such a method is used in the adaptive linear predictor described in Fig. 28. At the end of the speech frame time the filter is impuled and the output represents the prediction coefficients.

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