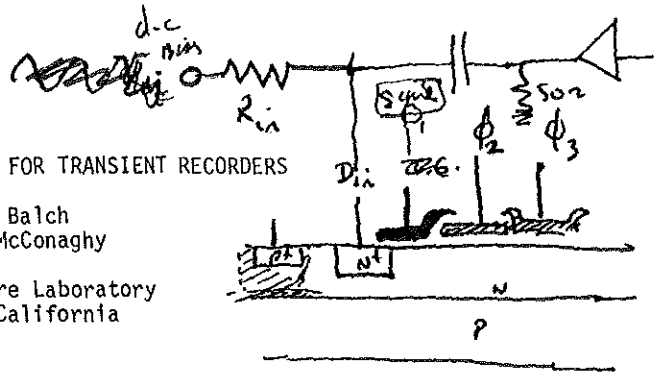

A CCD INTEGRATED CIRCUIT FOR TRANSIENT RECORDERS

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ABSTRACT

A 50 MHz CCD integrated circuit is described that has been developed for use in transient analog signal recorders to sample and time expand transient signals. The integrated circuit achieves an effective 200 MHz sample rate by using four 32 stage peristaltic CCDs to sample the transient signal four times each clock period. Dual frequency, 4ϕ clocking is used to sample and time expand the sampled data. The output signals of the four CCDs are multiplexed on-chip into a single low frequency output data line. When operated with 50 MHz/165 KHz 4ϕ clocks, this circuit has a 200 MHz sample rate, a record length of 640 nanoseconds, a time expansion factor of 303, and overall signal to noise ratio of 40:1. The signal to noise ratio is limited by fixed pattern noise of the four CCDs.

I. INTRODUCTION

A 50 MHz peristaltic CCD integrated circuit has been developed for use in transient analog signal recorders to sample and time expand transient signals before they are processed by a low speed A/D converter and digital memory. CCDs have previously been shown to be a useful element in this application (Ref. 1-3). This integrated circuit uses four CCDs to sample the transient signal four times each clock period to achieve a 200 MHz sampling rate. The time expansion operation involves clocking the electrical transient into the four CCDs at a 4ϕ clock frequency of 50 MHz and after some desired record length, switching the clock frequency to 100 to 200 KHz to read out the sampled data. The output signals of the four CCDs are multiplexed on-chip into a single output line.

II. CHIP DESIGN AND FABRICATION TECHNOLOGY

A. BURIED CHANNEL CCD TECHNOLOGY

Figure 1 shows the chip which consists of four 32 stage peristaltic CCDs positioned side by side so as to utilize a common 4ϕ clock structure. Each CCD is isolated from its neighbor and the rest of the chip by a 10 μm wide P+ channel stop diffusion. The devices have been constructed in a 4 μm thick N type epitaxial layer deposited on a P type substrate to achieve the very high speed charge transfer via large fringing fields (Ref. 4). The doping concentrations are 4×10^{14} and 6×10^{14} cm^{-3} for the epitaxial layer and substrate respectively. The 4ϕ clock electrodes are double layer polysilicon gates 11 μm long and span the four 250 μm wide channels. The channel oxide thickness under all the polysilicon gates is 0.15 μm. The overall chip dimensions are 2 mm by 2.8 mm.

B. INPUT STRUCTURE

Four N+ input diffusions and a common aluminum input gate comprise the input structure of the circuit as shown on the left side of Figure 1. The input gate is aluminum to allow it to overlap the first clocking electrodes which are on different levels of polysilicon for the four CCDs. The diffusions are staggered on a diagonal so that the first clocking electrode of each CCD is connected to a different clock phase to achieve four data samples per clock period. The transient signal can be applied to either the input gate or the diffusions. Most of our high speed measurements were made with the transient applied to the input gate and the input diffusions pulsed low for a very short time each clock period to inject a charge packet into the first potential well of each CCD. The input structure was d.c. biased to operate in a pulsed dynamic injection method with the transient signal on the input gate modulating the size of the charge packets introduced into the CCDs (Ref. 5). Figure 2 is a timing diagram of the significant input clocks for one representative CCD. The input diffusion clocks were phased so that they would inject a charge packet into the four CCD channels when a potential well existed under the first two clocking electrodes of each CCD.

C. OUTPUT STRUCTURE

The output section of the chip detects the charge packets in the four CCD channels and multiplexes the four parallel data signals into one output signal. Each of the four CCD channels uses a gated charge integrator consisting of a reset FET and an output source follower FET to detect the charge packets. The four floating N+ diffusions used for sensing the charge packets in the channels are staggered diagonally so that the last clocking electrode is a different phase for each of the CCDs. This organization, shown on the right side of Figure 1, permits each of the output FETs to sense the charge packets in different quarter segments of a clock period. The floating diffusions are separated from their respective last clocking electrode by a common aluminum output gate.

Aluminum was used in the same manner as for the input gate to permit overlapping of both levels of polysilicon used in the clocking structure with the common output gate. To multiplex the four output signals, the source terminals of the four output FETs were connected together on chip to a common bond pad and to an off-chip load resistor. Although this connection simplifies off-chip circuitry, the maximum voltage gain of the four output source followers operated in parallel is one quarter rather than unity. In addition, the reset gates were bonded together on chip and driven by a single reset gate clock operating at four times the frequency of the low frequency 4ϕ clock. The timing diagram for this common reset gate clock and the 4ϕ clocks operating at low frequency is shown in Figure 3. The timing of the reset gate signal was adjusted so that all reset gates were reset and turned off immediately before any clock phase goes to a low voltage state.

III. EXPERIMENTAL RESULTS

A. TEST CIRCUITS

Figure 4 shows a block diagram of the test circuits used for the time expansion mode of operation. For device diagnostic purposes the transient test pulse generator supplies a test signal to the input gate of the four CCDs in sync with the 50 MHz 4ϕ clock. The sync pulse is provided by a gate output pulse of a commercial oscilloscope. This sync pulse also starts a counter that counts the desired number of 50 MHz clock cycles before sending a trigger pulse to the frequency control and 4ϕ clock circuit that then switches the clock frequency from 50 MHz to a lower readout frequency. The frequency control and 4ϕ clock circuit uses a divide by four emitter coupled logic circuit (ECL) to generate the 4ϕ clock signals from a master clock signal supplied by either the f_{Hi} oscillator or the f_{Lo} oscillator. The ECL circuit maintains the phase integrity of all four clock phases at the instant of switching from 50 MHz to the readout frequency. Commercial pulse amplifiers increase the 4ϕ ECL level clock signals to 6 volts before the clock signals are applied to the CCD. Also, the 4ϕ ECL clock signals are used to trigger four additional clock generators that supply the input diffusion clock signals. The reset gate clock generator is synchronized to the f_{Lo} master oscillator so as to operate at four times the low frequency of the 4ϕ clock signals.

B. CCD PERFORMANCE

The performance of the CCD circuit when operated in the time expansion mode has been characterized by examining its response to rectangular pulse and linear ramp waveforms. Figure 5 shows an input pulse about 190 nanoseconds wide and the sampled output pulse time expanded to about 60 microseconds wide. The CCD clock frequency was switched from 50 MHz to 165 KHz for this result. The output signal voltage of this pulse is 34 mV with no fat zero having been introduced. The full well output signal voltage for the CCDs is about 55 mV. This corresponds to a measured full well charge packet of 0.23 picocoulomb. The charge transfer efficiency (CTE) of the CCDs has been measured to be greater than 0.9998 per transfer for a total of 128 (4 x 32) high speed transfers at 50 MHz. This CTE is sufficiently large that no output voltage difference can be seen between a single packet having 128 transfers at 50 MHz and a packet having only four transfers at 50 MHz and 124 low frequency transfers.

The response of the circuit to a linear ramp is shown in Figure 6. Figure 6a shows the input ramp applied to the common input gate electrode of all four CCDs and Figure 6b the time expanded output signal. As seen from the output signal waveform, the response of the circuit becomes increasingly nonlinear for low level charge packets. Consequently, we have found it necessary to bias the device into a more linear region of operation by introducing a background charge corresponding-to about 7 to 10 mV of output signal. For Figure 6b a 7 mV background signal was introduced to improve its linearity.

To obtain waveforms like those of Figures 5 and 6, we found it necessary to compensate any fixed pattern noise due to unequal response of the four CCDs by adjusting the individual d.c. bias levels of the four input diffusions. Some of the causes of unequal response of the four CCDs include (1) different clock voltages and waveshapes of the 4ϕ clocks and input diffusions clocks, (2) different electrode areas of the first clocking electrodes of the four CCDs and (3) different voltage gains of the four gated charge integrators. We have been able to compensate for these differences to the extent shown by the results of Figures 5 and 6 by individually adjusting the d.c. biases of the four input diffusions to obtain a smoothed output response to a linear ramp input. It has been possible to reduce this fixed pattern noise so that the ratio of the peak signal to the peak fixed pattern noise is about 40:1.

The fixed pattern noise among the four CCDs is much larger than the intrinsic noise of a single CCD channel as measured by a pulse height analyzer (PHA). The PHA was used to sample and record the output voltage distribution of a full well charge packet repeatedly injected into a single CCD channel. The noise distribution was nearly Gaussian and the signal to noise ratio was calculated as the ratio of the maximum signal to the full width half maximum. This number was repeatedly measured to be greater than 90:1. For this measurement, no prefiltering was done to remove any noise of the output FET or reset FET.

IV. CONCLUSION

Sampling of transients at a 200 MHz rate and their subsequent time expansion to output sample periods greater than 5 μs has been accomplished by operating four CCDs on a single chip at a 50 MHz 4ϕ clock frequency. The output signal amplitude, linearity and noise has been described. Further improvements are needed in the input and output sections of the CCDs to reduce the fixed pattern noise and improve the linearity of the circuit.

ACKNOWLEDGEMENTS

This work was performed under the auspices of the U.S. Energy Research and Development Administration under contract number W-7405-Eng-48.

The authors wish to acknowledge the fabrication assistance of F. Cook, K. Mayeda, W. Tindall and J. Trevino and the electronics assistance of L. Mendonca.

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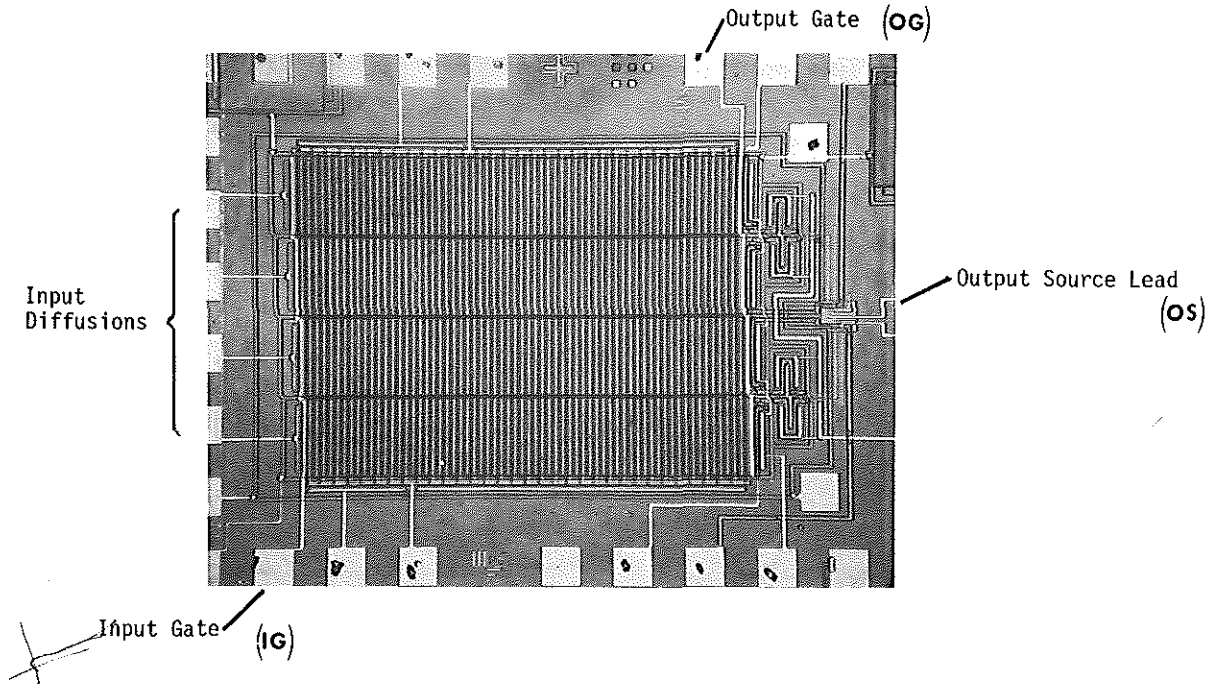

Fig. 1. Photomicrograph of Transient Recorder Chip

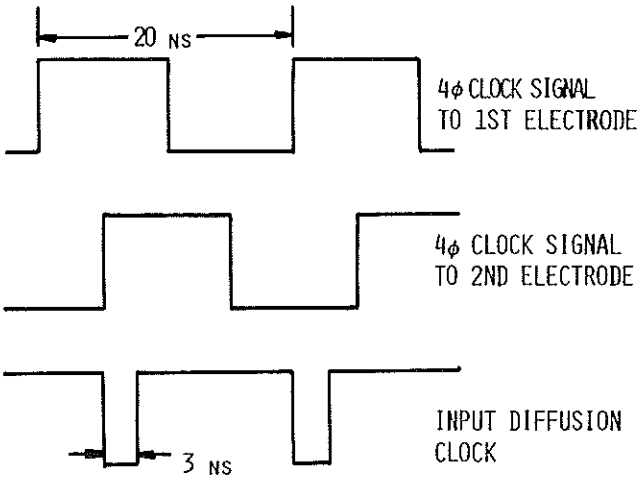

Fig. 2. Timing diagram of significant clocks at input structure of one CCD channel.

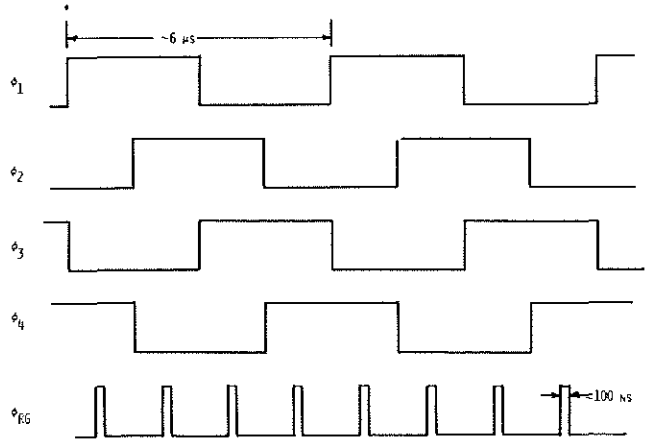

Fig. 3. Timing diagram of reset gate and 4 φ clocks operating at low frequency.

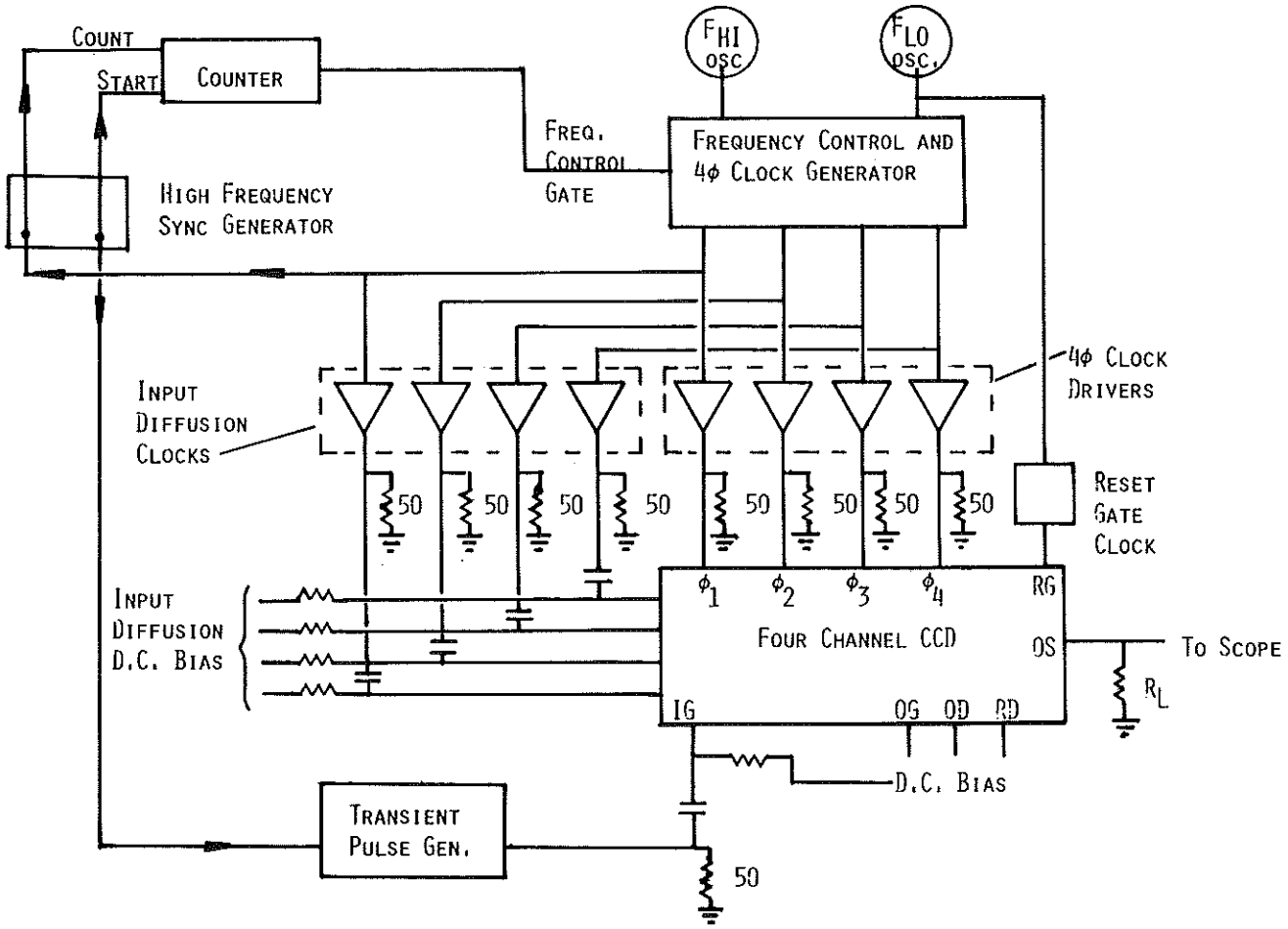

Fig. 4. Test Circuit for Time Expansion Operation

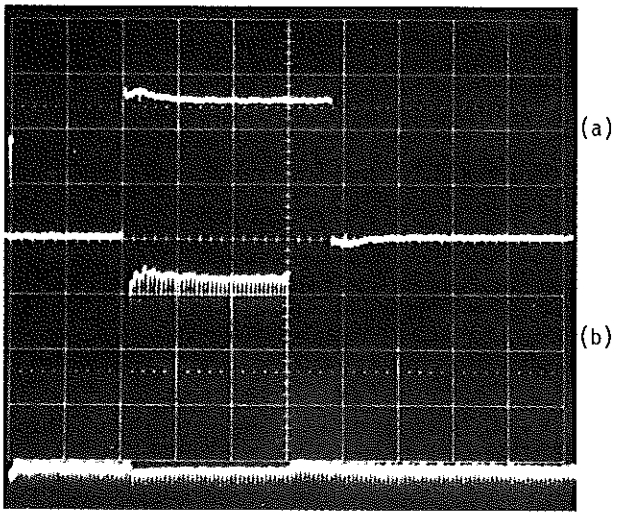

Fig. 5. Pulse response
(a) Input: 2V/DIV., 50 NS/Div.
(b) Output: 10 mV/DIV., 20 μs/DIV.

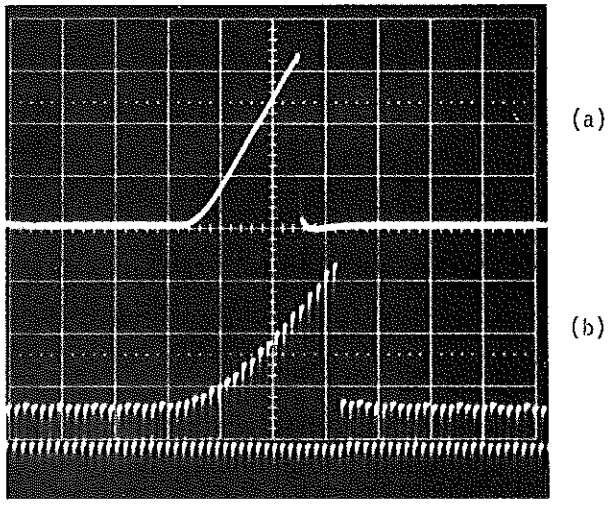

Fig. 6. Ramp response
(a) Input: 1V/DIV., 50 NS/DIV.
(b) Output: 10 mV/DIV., 10 μs/DIV.