A SUB-NANOSECOND CCD

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ABSTRACT

A 32-cell silicon n-channel PCCD was fabricated and tested for charge transfer efficiency vs. transfer time. Results showed that a charge transfer time of 550 picoseconds with a 0.9998 transfer efficiency could be obtained when operated in the uni-phase mode. These conditions correspond to an operating rate of 900 MHz when operated as an analog data or digital device.

I. INTRODUCTION

The CCD is becoming a very significant electronic device and is finding uses in many digital, analog and imaging applications. As with most electronic devices, the frequency of operation is one of the most important features. In the case of the CCD, the ability to transfer data at a rapid rate is one of its paramount features. Surface or buried channel CCD's which are presently available have been limited to operating speeds below 20 MHz. This is due to the limitations of the materials and photolithographic technology. Esser (Ref. 1), however, introduced the modified bulk channel CCD (peristaltic CCD) which transfers charge deep within the material where the transverse electrical field is large and the transfer efficiency is, therefore, higher. Theoretically, it has been estimated that charge transfer in a Si PCCD is sufficiently fast that it can be operated into the GHz range (References 2 and 3).

Lately, PCCD's have been operated over 200 MHz with good transfer efficiency when operated in the fast/slow mode (Ref. 4). The purpose of this present work was to determine quantitatively how rapid charge transfer can be in a silicon PCCD. The devices used in these experiments were made on n-type, epitaxial silicon grown on p-type substrate material. These devices showed extremely good transfer efficiency with charge transfer times between gates as short as 550 picoseconds.

II. EXPERIMENTAL DEVICE

The devices which were tested were 32-cell PCCD's. These devices had the same basic structure and design parameters as reported before (References 1 and 4), and as shown here in schematic detail in Figure 1. The devices were fabricated on a 5-micron epi layer which was grown on a (100) silicon substrate doped with 5×10^{14} boron/cm^3. The epi layer was doped 1×10^{15} phosphorous/cm^3. After the channel stop, input and output diffusions were grown; the CCD channel region was implanted with a phosphorous implant at a dosage of 1×10^{12}/cm^2.

The post-implant anneal and drive-in was performed for one hour at 1000°C. By means of spreading resistance measurements, it was shown that 80 percent of the implanted phosphorous ions were activated. The profile of the substrate wafer after the anneal stage is shown in Figure 2. Two layers of aluminum were used to form the four-phase CCD drive gates. For the gate structure, which consisted of 5 micron wide gates, a 2200 A layer of Silox was used as insulation between the two gate layers. The overlap between gates was designed to be 0.5 microns. This overlap was used to minimize intergate capacitance and to reduce the probability of gate shorts due to pinholes in the Silox in the overlapping areas.

The completed devices were packaged in 16-pin TO-8 cans. A packaged device is shown in Figure 3. Notice that all four driving gate pads are bonded to the package with two 1-mil aluminum wires in order to reduce lead inductance and its effects at the higher frequencies. In addition, one more lead was wire-bonded to gate 3 in order to provide access in monitoring the gate waveform at the device itself.

III. DEVICE OPERATION

Although the initial intent was to operate this device in a two-phase mode, it was found that operation in the uni-phase mode was much simpler to implement since only one driving pulse was required and there were no synchronization problems which could be difficult at high speeds. The timing for uni-phase operation is illustrated in Figure 4. Initially, at $t = t_o$ the potential well configuration is biased like a staircase and the charges are stored under gate 4. When a pulse arrives, the gate potential increases. At $t = t_1$ the potential barrier of gate 1 is still high and no transfer of charge occurs, even though the potential profile under the gates has changed. When the (negative) gate voltage increases further, charges start to move from under gate 4 to a position under gate 2 as shown in the potential diagram for $t = t_2$. At the peak of the pulse, the charge transfer is in its final stages. As the gate voltage is reduced, a potential bucket will be formed after time $t = t_2$ but before $t = t_4$, as shown in the sketch for $t = t_3$. As the potential drops, a well starts to form under a gate 4 and the charge stops flowing. Any residual charges will remain in that well. As the potential drops further, a second transfer occurs as illustrated for $t = t_4$ and t_5. This process completes the charge transfer. Although the actual charge transfer time, T, is less than the width

of the driving pulse (i.e., t_4-t_1), this value is more easily defined and more convenient. In the case of two-phase operation the corresponding clock frequency is 1/2T.

IV. EXPERIMENTAL SETUP

As in most high frequency experiments, difficulties are always encountered in driving a large capacitance to high voltages with short pulses. One of the solutions to this problem is to reduce the load resistance of the line so that the RC time constant is smaller than the rise time of the applied pulses. Under these conditions the driver will require more power. In order to overcome these requirements for vhf large amplitude drive pulses, a Tektronix-type 109 line discharge pulse generator with low repetition rate was used. This pulse generator can reproduce pulses at a 700 Hz rate. The pulses which are generated have a 250 picosecond rise and fall time and can have an output voltage as high as 50 volts into a 50-ohm line using the internal voltage source in the instrument. Because of the high power output of this generator, a large attenuation can be tolerated. This feature makes it very desirable for this experiment. Since this type of pulse generator uses a mercury relay switch to discharge the pulse generating line, the output is not stable and has a large amount of time jitter associated with it. Pulses from the generator were stepped down on the CCD test circuit board into 8 ohms by means of a resistor attenuator. The total driven capacitance for each CCD gate was approximately 15 picofarads. This resulted in an RC time constant of 120 picoseconds. The equivalent circuit of the gate structures and the associated drivers is shown in Figure 5. In order to determine the exact pulse width as it was actually applied to the CCD gates, an additional bond was made to the phase 3 pad and a wire taken out in order to monitor the gate 3 waveform. This additional bonding wire can be seen in Figure 3. A 500-ohm attenuator was used so that a 50-ohm coaxial cable could be connected to the signal of the gate to the scope, without loading the driving signal to the gate. Additional signals were also picked off at the input side of the circuitry in order to provide triggering for the sampling scope and a clock signal to the CCD tester. The CCD test boards provided all the CCD bias voltages to the CCD, the reset pulses required for the output operation and a countdown of 256 which was used to synchronize the signal and to trigger the input signal pulse generator. A block diagram of the overall setup is shown in Figure 6.

V. TESTS AND RESULTS

Because of the low repetition rate of the Tektronix 109 pulse generator and the thermal leakage current of the CCD's, the device had to be cooled down to -150°C. Before the device was operated at the lower temperature, a preliminary configuration using another pulse generator with higher repetition rate was used for the initial setup. After the initial operation at room temperature and adjustment of all bias voltages, the entire CCD test board with the 32-cell CCD was lowered into a liquid nitrogen transfer dewar. The driver circuits remained above the liquid nitrogen level because operation at nitrogen temperature was not required of these circuits. The temperature of the device was monitored at the back of the CCD using a platinum resistor thermometer and bridge. The driving pulses were applied to gate 3 and 4. The waveform is shown in Figure 7. The amplitude of the pulse was 9 volts and the pulse width was 500 picoseconds. Both input with and without fat zero had been tested. The transfer efficiency was about the same.

The output without fat zero is shown in Figure 8. The number of total charge transfers was 31 and the transfer efficiency was demonstrated to be better than 0.9998 per transfer.

VI. CONCLUSIONS

We have demonstrated that charge can be transferred within the silicon n-channel PCCD's in less than 550 picoseconds with a 0.9998 transfer efficiency. These results suggest the feasibility of operating the PCCD at 1/2T = 900 MHz for uni- or two-phase mode of operation. For four-phase mode of operation, the wave of the potential well is a continuous propagated movement; hence, the operating frequency will be doubled, i.e., 1/T = 1.8 GHz. At these transfer times we have not observed any degradation of the transfer efficiency. It is thought that this performance may be due to higher carrier mobility in the silicon at the lower temperatures at which the device was operated. This will be the basis for future investigations. The CCD input and output has not been investigated in detail. The highest rate of operation for the input has been 200 MHz. It is clear that the input circuitry may have less difficulty in operating at higher speeds because the higher power signal can be used to overcome the stray capacitance. The output circuitry does not have this advantage. Therefore, the output amplifier may be the most important factor which governs the maximum speed of the CCD. It should be noted, however, that since gigahertz FET operation has been achieved, the incorporation of gigahertz FET's into the CCD process and their utilization as an output device for the CCD makes a gigahertz PCCD feasible.

VII. ACKNOWLEDGMENT

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4. Y. T. Chan, B. T. French, and P. E. Green, "Extremely High Speed CCD Analog Delay Line", Inter. Conf. on the Application of CCD's, p. 29-31, Oct. 1975, San Diego, CA.

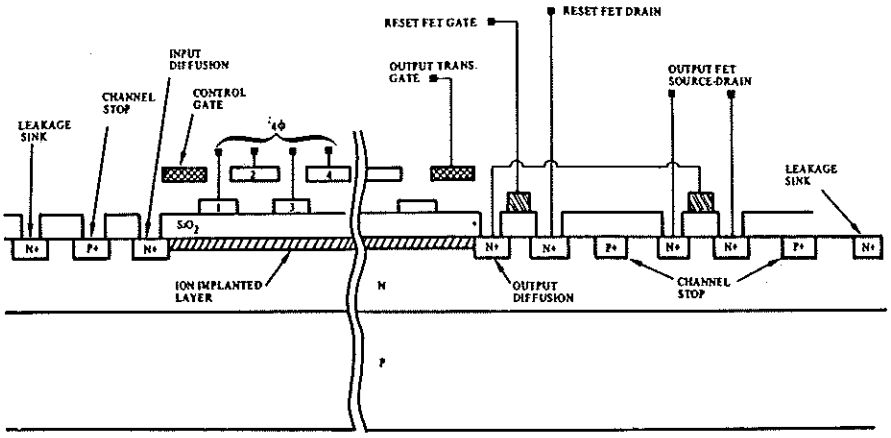

Figure 1. Peristaltic CCD - Cross Section (in Direction of Charge Propagation)

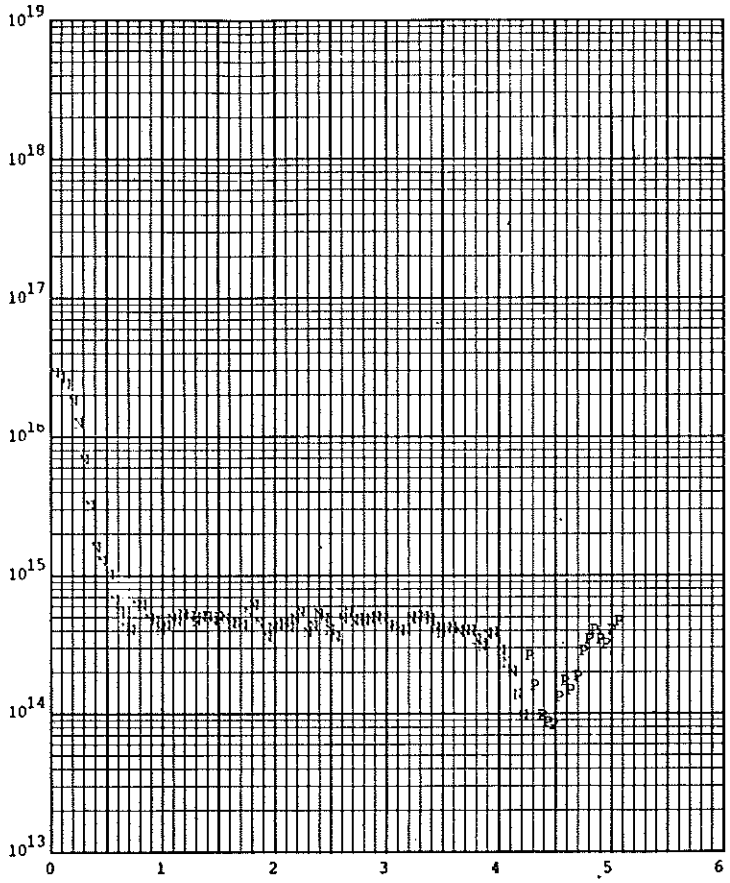

Figure 2. Device Doping Profile

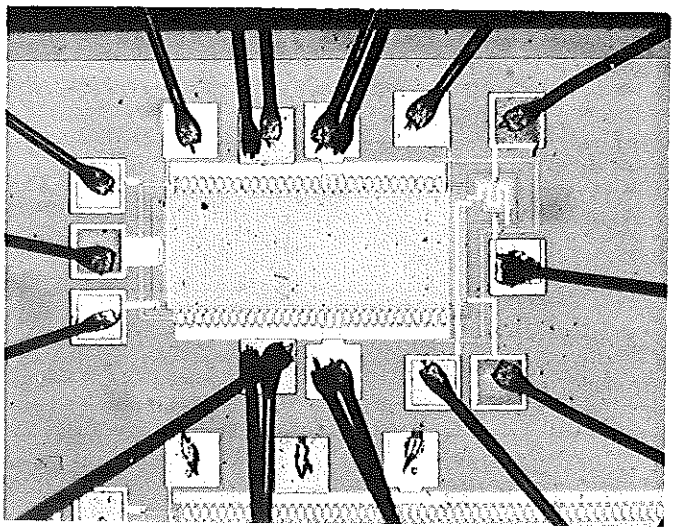

Figure 3. Photograph of a Tested Device

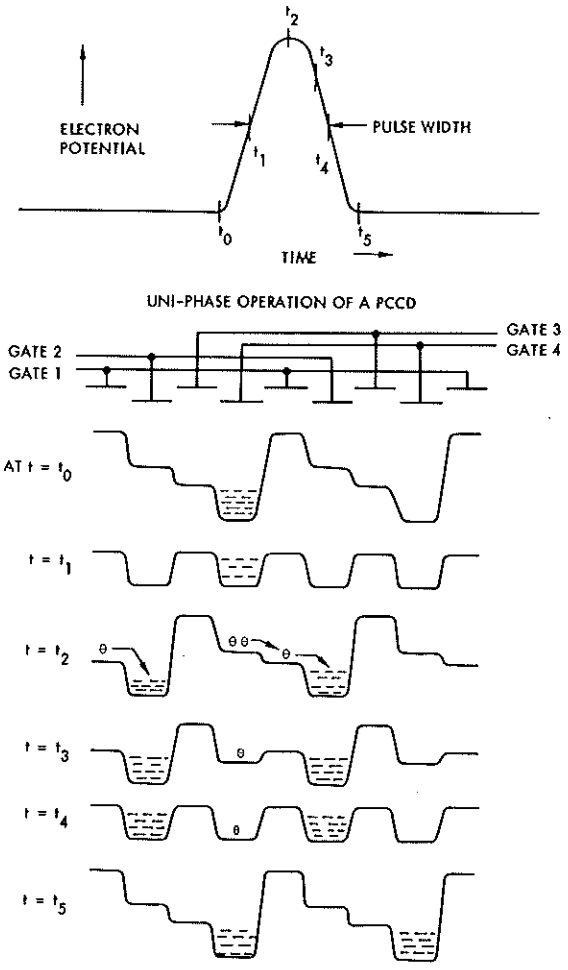

Figure 4. Uni-Phase Operation of a PCCD

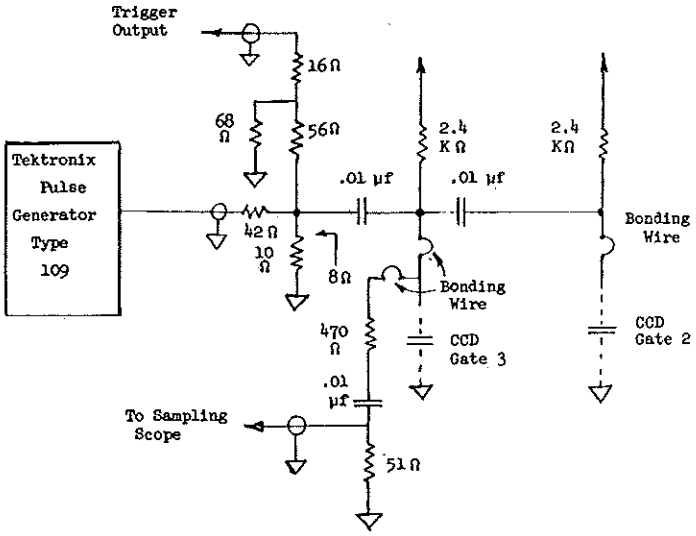

Figure 5. PCCD Driving Circuit

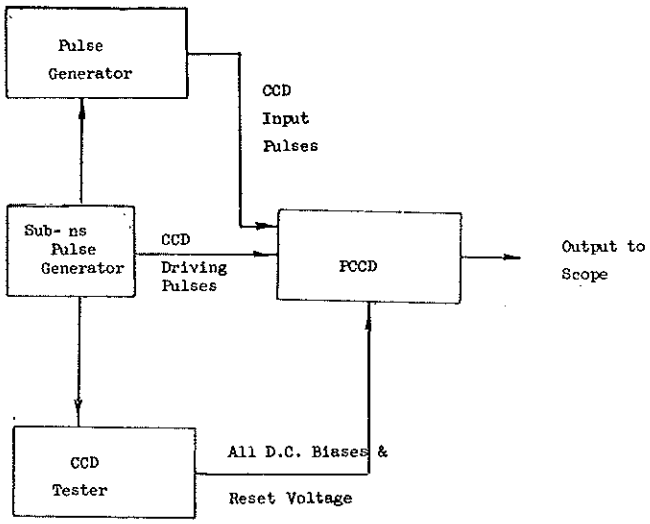

Figure 6. Block Diagram for Charge Transfer
Time Measurement Using Uni-Phase

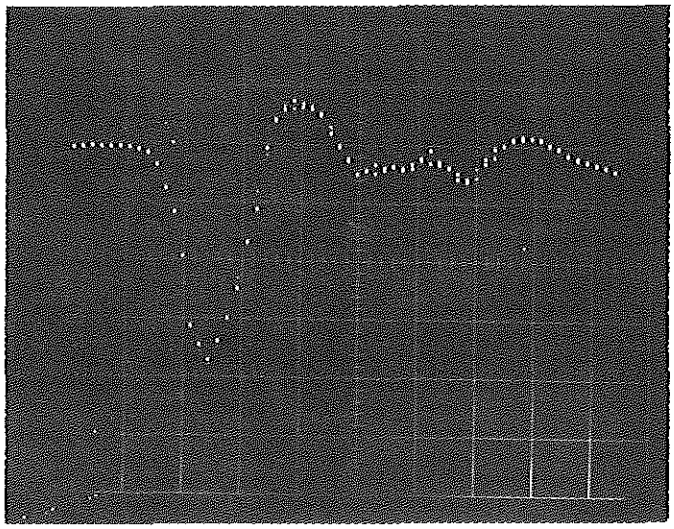

Figure 7. Waveform of CCD Driving Pulse

Vertical Scale: 2v/div.
Horizontal Scale: 500 ps/div.

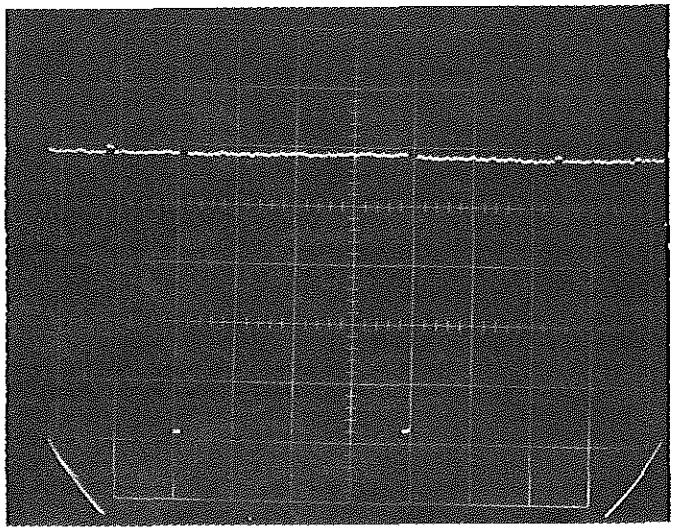

Figure 8. Output of PCCD at -142°C