LOW-NOISE VIDEO AMPLIFIERS FOR IMAGING CCD'S

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ABSTRACT

This paper describes various techniques developed by The Perkin-Elmer Corporation which will enable the CCD (charge coupled device) imaging array user to obtain optimum performance from the device. A CCD video channel is described, and detector-preamplifier interface requirements are examined. A noise model for the system is discussed at length and laboratory data presented and compared to predicted results. The paper concludes with a new preamplifier configuration that will yield improved performance.

I. INTRODUCTION

A typical CCD video channel (Fig. 1) can be broken down into two major components: on-chip and off-chip electronics. The on-chip electronics comprises the inner elements of the CCD detector, i.e., the detector elements, charge transport registers, bias electrodes, and output amplifier. The off-chip electronics contains a preamplifier and signal processing electronics. The preamplifier provides sufficient gain to amplify the detector's output to a level well above the inherent noise of the processing electronics, while the processing electronics extracts the video information and enhances the signal-to-noise ratio (S/N). Processing techniques to improve S/N consist of bandwidth control and synchronous sampling. Minimizing channel bandwidth prior to any signal sampling reduces the contribution of frequency-dependent noise sources. Sampling techniques, such as correlated double sampling (Ref. 1), can suppress correlated noise sources, among which are reset noise, dc offsets, slowly varying baselines, and 1/f noise.

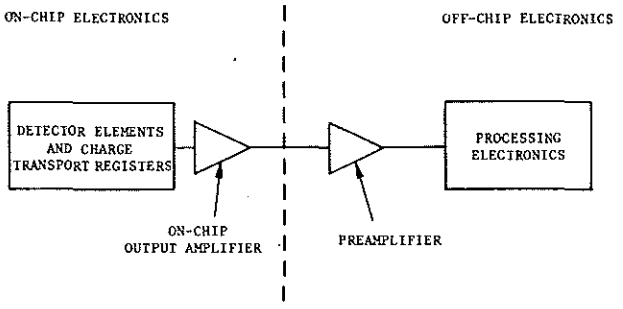
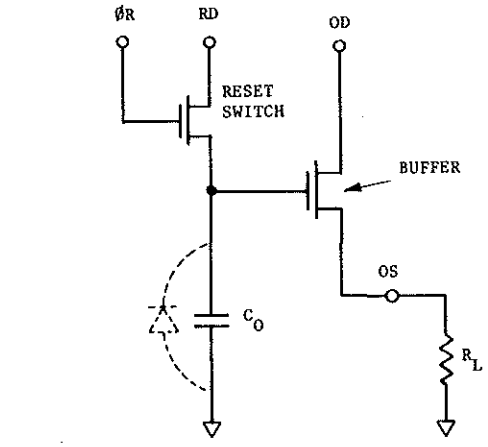


Fig. 1. Typical CCD video channel

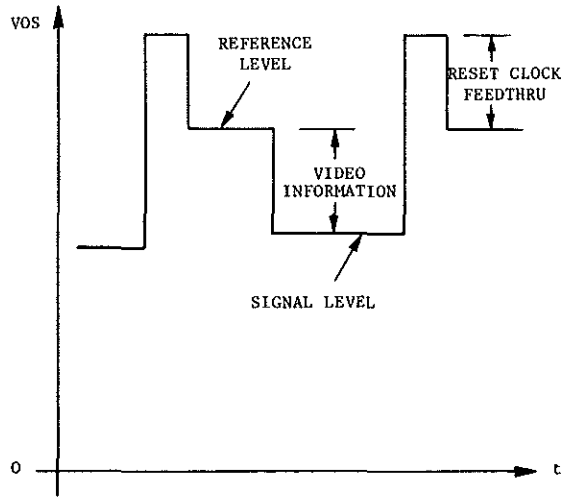
Since the interface between the detector and preamplifier can be critical if low-noise performance is required, the characteristics of the on-chip amplifier, the preamplifier, and any processing electronics must be established. To determine the combined effects of all noise sources in the channel, this paper covers various types of noises and provides a noise model block diagram to locate each source; methods to reduce their effects are also discussed. Laboratory results are presented and compared to the predicted values. Finally, based on the results obtained, this paper concludes with a new preamplifier configuration which will yield improved performance.

II. DETECTOR/PREAMPLIFIER INTERFACE COMPATIBILITY

The output amplifier commonly used on commercially available CCD detectors (Ref. 2) is the gated charge amplifier (GCA) which consists of two MOS (metal oxide semiconductor) transistors (Fig. 2a). One is used as a switch to reset the charge sensing capacitor (C_o), while the other is connected as a source follower to buffer the output. The signal present at the output of the detector is a three-level waveform approximately 0.2V to 0.3V peak-to-peak impressed upon a dc level of several volts. The three levels are defined as (1) reference level, (2) signal level, and (3) reset clock feedthru (Fig. 2b). The video information is equal to the difference in magnitude of the signal and reference levels.



(a) SCHEMATIC



(b) OUTPUT SIGNAL

Fig. 2. Gated charge amplifier

The reset clock feedthru signal presents a processing problem in low-noise applications due to its large amplitude, typically 200 mv. In amplifying the signal, the reset clock feedthru becomes amplified and this could possibly overload the preamplifier. To alleviate the problem, it is common to find another output available from the detector, known as the compensation output (Ref. 2). By using a differential input preamplifier, it is possible to cancel the reset clock feedthru at the preamplifier's input. Since the dc levels at the signal and compensation outputs may be different, direct subtraction of the two signals is not possible. A coupling capacitor must be used to block the dc component at each output. The functional schematic representing the detector-preamplifier interface is shown in Fig. 3, which includes a CDS (correlated double sampling) implementation.

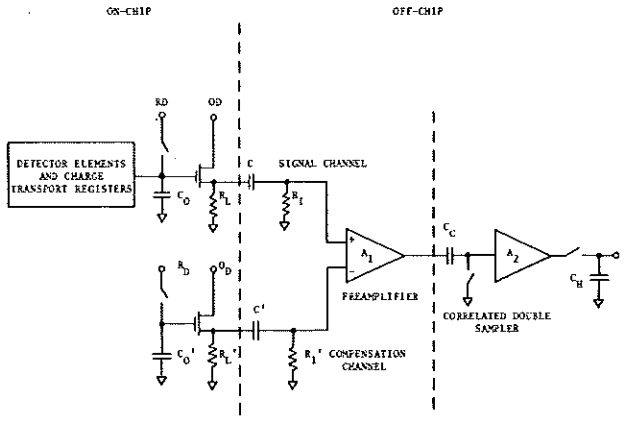


Fig. 3. Video channel functional schematic

III. NOISE MODEL

The noises likely to be found in the video channel are generated both in the detector and the off-chip electronics. A noise model block diagram locating each source is shown in Fig. 4.

A. DETECTOR NOISE SOURCES

1. Dark Current

Dark current noise is a result of thermally generated hole-electron pairs within a CCD cell. The magnitude of dark current noise, in electrons, is given by

$$N_d = \left[\frac{JA\tau}{q}\right]^{1/2} \quad (1)$$

where

J is the average dark current density

A is the total collection area

τ is the integration time

q is the magnitude of an electronic charge.

Dark current is generated in both the detector elements and analog transport registers. J is a function of temperature, doubling approximately in value for every 10^{o}C rise.

2. Reset Noise

A GCA requires precharging the collection capacitor C_o prior to receiving each new signal charge packet from the CCD registers. The noise associated with this resetting mechanism is given by:

$$N_r = \frac{1}{q}\left[k\,T\,C_o\right]^{1/2} \quad (2)$$

where K is Boltzmann's constant and T is the absolute temperature. Reset noise is correlated within a detector element period.

3. Bulk State Noise

Bulk state noise is produced by trapping states in the bulk of the silicon. At low light levels, the worst case magnitude of this noise source, according to Barbe (Ref. 3), is

$$N_b = 0.28\sqrt{M} \quad (3)$$

where M is the number of transfers experienced by the charge packet.

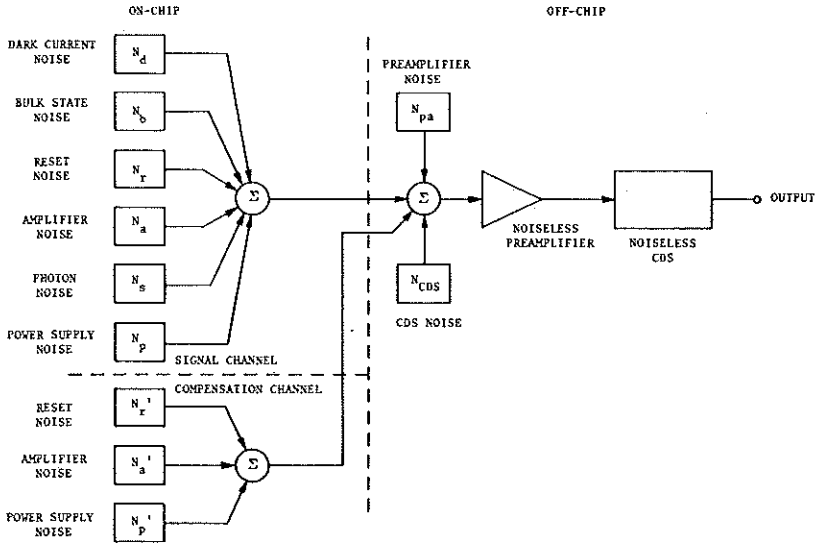


Fig. 4. Noise model block diagram

4. Photon Noise

The emission of photons from any source obey Poisson's statistics. Thus, the noise inherent to the signal to be detected is

$$N_p = \sqrt{N_s} \tag{4}$$

where N_s is the number of signal electrons generated at the pixels.

5. Amplifier Noise

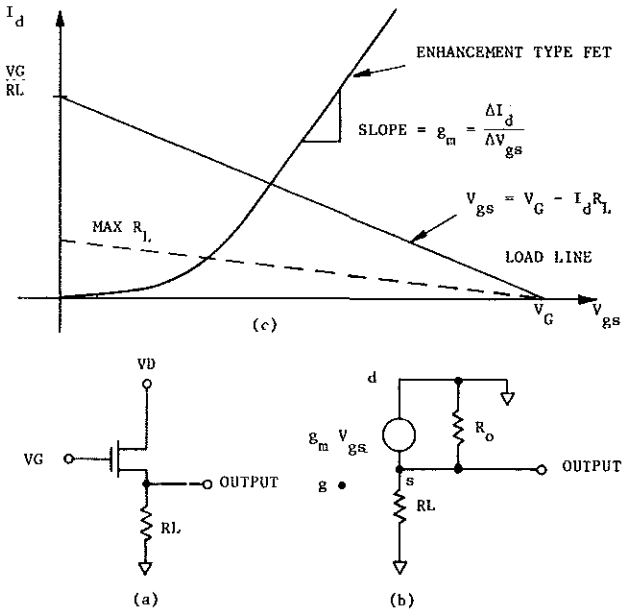
The on-chip amplifier consists of an MOS transistor connected as a source follower. The principal noise source associated with this FET (field-effect transistor) is a noise voltage in series with the gate terminal. The midband value for this voltage (above the 1/f knee) is given by (Ref. 4):

$$e_n^2 = \frac{4kTB}{g_m} K \tag{5}$$

where g_m is the FET's transconductance, B the noise bandwidth and K a factor which depends upon operating conditions and transistor design and processing. The value of K can be as low as 2/3. Thus, the minimum expected noise, in electrons, at the collection capacitor C_o due to the transistor is:

$$N_a = \frac{C_o}{q} \sqrt{\frac{8kTB}{3g_m}} \tag{6}$$

It must be noted that this is the midband value and does not account for any 1/f noise components. Therefore, it is important to know the spectral content of the FET noise and the frequency band of interest in order to include all the noise introduced by the FET. The contribution of input noise current for the FET amplifier is suppressed by the chopping action of the reset switch (Ref. 5) and can, therefore, be neglected.



(a) SCHEMATIC
(b) SMALL SIGNAL EQUIVALENT CIRCUIT
(c) TRANSFER CHARACTERISTIC WITH DC LOAD LINE

Fig. 5. FET source follower

6. Power Supply Noise

Noise present on the drain of the output or reset transistor can perturbate the output signal; noise on the reset drain is directly impressed on the collection capacitor during the reset period. The equivalent noise electrons introduced are

$$N_{RD} = \frac{C_o}{q} e_{RD} \tag{7}$$

where e_{RD} is the rms noise at the reset drain.

The equivalent noise at the collection capacitor C_o due to variations at the output drain terminal is given by:

$$N_{OD} = \frac{C_o}{q} \frac{e_{OD}}{g_m R_o} \tag{8}$$

where e_{OD} is the rms noise present at the output drain and R_o is the output resistance of the FET (Fig. 5b). The total power supply noise component is:

$$N_p = \frac{C_o}{q} \left[\left(\frac{e_{OD}}{g_m R_o} \right)^2 + e_{RD}^2 \right]^{1/2} \tag{9}$$

B. OFF-CHIP ELECTRONICS NOISE SOURCES

1. Preamplifier Noise

The preamplifier is characterized by its own equivalent input noise voltage and current sources, e_{npa} and i_{npa}, respectively. They are a function of the preamplifier's design. The equivalent noise contributed by these sources at C_o is equal to:

$$N_{pa} = \frac{C_o}{q} \left[\frac{1+g_m R_L}{g_m R_L} \right] \left[e_{npa}^2 + (i_{npa} R_s)^2 \right]^{1/2} \tag{10}$$

where R_L is the dynamic load seen by the output source follower and R_S is the equivalent source resistance seen by the amplifier.

2. Correlated Double Sampler (CDS) Noise

Since CDS requires the charging of a capacitor through a switch of finite impedance, the noise produced is identical to the reset noise associated with the GCA. Thus, the noise contributed by the capacitors in the CDS at C_o is given by:

$$N_{CDS} = \frac{C_o}{q A_1} \left[\frac{kT}{C_c} + \frac{kT}{A_2^2 C_H} \right]^{1/2} \tag{11}$$

where

A_1 is the gain of the preamplifier

A_2 is the gain of the buffer within the CDS

C_C is the clamping capacitor

C_H is the holding capacitor.

C. SYSTEM NOISE

Combining each of the component parts described above, two expressions for noise are obtainable. For the system not utilizing the double correlated sampler, the equivalent noise at C_o is given by:

$$N_T^2 = N_d^2 + 2N_r^2 + N_b^2 + N_s^2 + 2N_a^2 + N_{pa}^2 \qquad (12)$$

Using CDS, the equivalent noise at C_o is:

$$N_{T_{CDS}}^2 = N_s^2 + N_b^2 + N_s^2 + 2N_a^2 + N_{pa}^2 + N_{CDS}^2 \qquad (13)$$

In each case, power supply noise N_p was not included since it can be adequately suppressed by proper power supply bypassing.

D. OPERATING CONSIDERATIONS

A review of the on-chip noise source (Equations 1, 2, and 5) indicates that both time and temperature can affect the total noise generated within the CCD detector. Cooling the detector to -10°C will reduce the reset and on-chip amplifier noise components by a small amount. However, dark current noise will be reduced significantly. Assuming that the dark current halves for every 10°C drop in temperature, the dark current noise at -10°C will be 35% of the room temperature value.

Since the detector elements operate independently of the CCD transport registers, it is possible to control the time parameter in the dark current noise expression (Equation 1). Dark current (and the noise associated with it) is generated both in the detector elements and the transport registers. The available intensity level of the object will, in general, set the integration time required for the detector elements to accumulate sufficient signal charge. During the same interval, the detector elements are also accumulating dark current charge. For low light level operation, integration times of 0.1 second are common. Cooling is the only means of reducing dark current under these conditions. However, it is not necessary for the transport registers to also accumulate dark current charge during this time. Depending on the rate at which the register is clocked, it is possible to output all detector element data before the end of an integration period (transfer command). Operation in this mode presents the video information at the output in the form of a burst immediately following a transfer command. The signal present for the remainder of the period is merely the zero signal level of the transport register. This level is a function of clock rate and dark current density. In the case of long integration time systems, the burst readout mode offers three advantages:

- Minimization of noise due to dark current in the transport registers.
- Increased dynamic range since dark signal is less, leaving more well capacity for signal charge.
- Increased suppression of 1/f noise components by CDS due to higher frequency operation.

E. NOISE MEASUREMENTS

To determine the validity of the noise model, we conducted an experiment using a commercially available 1728 element linear array. Since the effect of all external (off-chip) noise sources is divided by the gain of the on-chip source follower, it is important to know this gain. Using the small signal model shown in Fig. 5b, the gain of the on-chip amplifier is:

$$G = \frac{g_m R'}{1+g_m R'} \qquad (14)$$

where R' is the equivalent parallel resistance of R_L and R_o. It is expected that g_m is on the order of 1 mmho. Thus if R' is 1 kΩ , the gain G will be 1/2. This gain, being less than unity, will effectively increase the contribution of all off-chip noise sources. The characteristics of the output FET were measured in order to account for its effect.

1. Measurement of FET Characteristics

The FET characteristics may be measured using the following technique. Bias the output drain (OD) and reset drain (RD) terminals (refer to Fig. 2a) at their normal operating levels as recommended by the manufacturer. Ground all clock inputs except the reset clock (ØR). Apply a bias to the ØR electrode equal to the "high" level recommended by the manufacturer. These bias conditions keep the reset transistor "on", setting the gate potential of the output FET to VRD. By varying R_L, the voltage at the output source (OS) will change according to the FET characteristics. The drain current (I_d) is given by VOS/R_L and VGS is equal to VRD-VOS. This procedure was used to obtain the output FET characteristics of the test detector. The results are plotted in Fig. 6. The measured value of g_m is 0.85 mmho. It is interesting to note that it appears that g_m is relatively constant down to a drain current of 1 ma. This indicates that this device may be operated with a bias resistor of 10 kΩ . This would reduce on-chip power dissipation to under 10 mw.

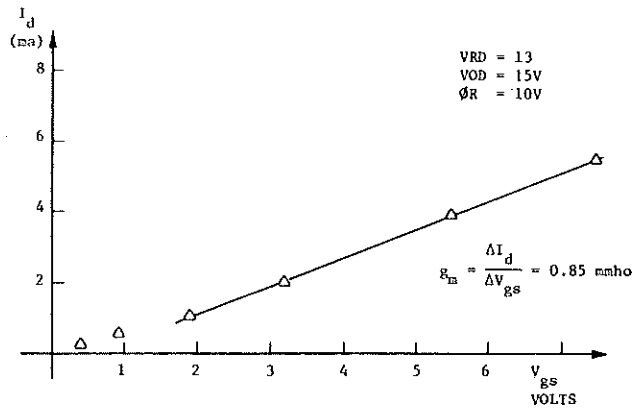


Fig. 6. Output FET characteristics

In a similar fashion, the noise of the on-chip output FET was measured. With the output FET statically biased, the noise in a 5 MHz bandwidth was found to be 38 nV/$\sqrt{Hz}$. Although larger than that predicted by Equation 5 (3.6 nV/$\sqrt{Hz}$), it is not an unusual value. As previously mentioned, Equation 5 predicted only the midband value and did not account for any 1/f contributions. Similar results were reported in Ref. 6.

2. Dynamic Test

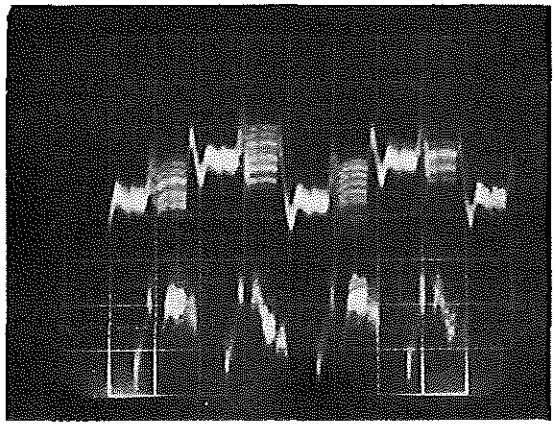
A preamplifier having a total equivalent input noise of 4.8 nV/ Hz was used. The detector was cooled to -10°C. The magnitude of the individual noise components is given in Table 1. The entry for N_d is an estimate; however, its contribution is small and will not effect the results significantly. N_{CDS} and N_p were also small and could be neglected; N_s was omitted since noise was measured under dark conditions.

Table 1. Noise contributors

Source		Magnitude (electrons)
N_r	Reset	188
N_a	On-chip amplifier	132
N_d	Dark current	10
N_b	Bulk state	12
N_{pa}	Preamplifier	56
N_{CDS}	CDS	-
N_p	Power supply	-
N_s	Signal	-

A noise prior to CDS was predicted to be (using Equation 12) 330 electrons and 196 electrons after CDS processing (using Equation 13). Measured results (Fig. 7) indicate 472 and 235 noise electrons before and after CDS, respectively. The large discrepancy between pre-CDS noise is most likely due to the value of the on-chip collection capacitance being larger than expected and significant 1/f noise components of the output amplifier. However, being correlated, this additional noise was rejected by the CDS as demonstrated by the measured noise after CDS.

Since the on-chip amplifier is a dominant contributor to the total noise signal, improved performance could be obtained if the off-chip preamplifier did not use the compensation signal. The compensation source was used only to eliminate front end overload in the preamplifier by canceling the reset clock feedthru. A preamplifier configuration that does not require the compensation signal is presented in section IV. Elimination of this noise source would yield improved performance.



2 μs/DIV

Fig. 7. Measured noise: pre- and post-CDS
(a) Output of CDS - off chip electronics gain of 200
(b) Input to CDS - off chip electronics gain of 100

IV. NEW PREAMPLIFIER CONFIGURATION

The proposed preamplifier configuration (Fig. 8) is a clamped input amplifier. Operation of the circuits is as follows. By selectively closing switch S while the detector's output is at the reference level (Fig. 2), capacitor C will charge towards this level with a time constant equal to

$$\tau_c = (R_S + R_{SW})\, C$$

where R_S is the source impedance and R_{SW} is the "on" switch resistance. With C charged to the reference level, the output of the amplifier will swing negatively for signal levels and positively for reset feedthru's when the switch is opened. The signal level will be amplified by 1+(R2/R1), but the reset feedthru will be limited to one diode drop. The result is that the amplifier's input will not be overdriven and the reset feedthru is limited.

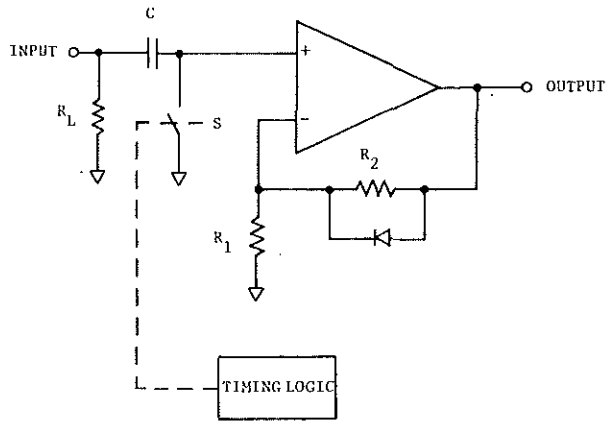


Fig. 8. Clamped input amplifier

The clamping can be done on an element or line basis. However, line clamping is preferable since no extra switching transients are injected into the signal during the video output period. The charging of capacitor C need not be completed in one reference level interval either if line clamping is elected. Several periods may be used. When the switch is opened, an error due to the amplifier's input bias current will be produced, manifesting itself in the form of a ramp. The magnitude of this error at the last pixel is

$$\varepsilon = \frac{I_b\, Ne}{C\, f_d} \qquad (15)$$

where Ne is the number of elements in the array and f_d is the data rate.

The action of charging the coupling capacitor through a finite impedance does introduce another source of reset noise at the preamplifier's input. The amount of noise produced, referred to the collection capacitor within the detector, is

$$N_c = \frac{C_o}{q}\left[\frac{kT}{C}\right]^{1/2}\left[\frac{1+g_m R_L}{g_m R_L}\right] \qquad (16)$$

However, it is correlated noise, that is, on a line-by-line basis. By utilizing the CDS at the preamplifier's output, N_c can be suppressed.

Input clamping provides an additional benefit. By performing a dc restoration immediately at the input, the floating baseline present in a capacitively coupled configuration is eliminated.

V. CONCLUSIONS

During our investigation of a typical imaging CCD video channel, particular attention was paid to the detector's on-chip output amplifier and the off-chip low-noise preamplifier interface compatibility, including the need for the compensation output. A noise model, incorporating the

detector and processing electronics noise sources, was developed for the video channel, and the experimental results demonstrated the validity of the model. The concept of "burst readout" operation to yield improved performance by reducing dark current noise and increasing dynamic range was introduced as a result of the noise analysis. A method to measure the detector's on-chip output FET characteristics also warranted the activity. Data obtained from a 1728 element linear CCD array indicated the following:

- the value of the dc load resistance could be increased to 10 kΩ .
- the noise contributions of the FETs associated with the signal and compensation output amplifiers were significantly higher than predicted by theory.

This being the case, a new preamplifier configuration, allowing the detector to operate with a higher load resistance and not requiring the compensation output from the detector, was our result. Operation with a higher load resistance reduces the effect of all off-chip noise sources by increasing the gain of the on-chip amplifier. Elimination of the need for the compensation output eliminates the noise associated with it, thus increasing the overall signal-to-noise ratio.

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