A CCD - BASED TRANSIENT DATA RECORDER*

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ABSTRACT The recording of analog transient data in a digital form at high bandwidth presents technical challenges in many areas. A variety of techniques lend themselves to the task at hand. Each technique presents unique challenges derived from overall system performance requirements. One particularly attractive technique involves the use of an Analog Shift Register (ASR) for time conversion in order to minimize high-speed components.

After appropriate filtering, transient data is sampled and sorted in the ASR at a high rate as analog samples. After the transient, data is shifted from the ASR at slow rate through an analog to digital converter to a digital memory for temporary storage. Upon remote command, the data is then read nondestructively and transmitted at a convenient rate to a remote location for permanent storage and analysis. The transient data recorder being developed will sample and store 1,000 six-bit words of 100 MHz data with a sampling aperture of +50 picoseconds. Since data is slowed after acquisition in the ASR, the remainder of the recorder is comprised of standard TTL integrated circuit logic.

The ASR consists of eight interleaved CCD's. Each CCD is capable of storing 128 data samples acquired at input rates ranging from 312.5 Ksamples/sec to 62.5 Msamples/sec. Operating eight CCD's in an interleaved fashion provides storage for 1024 samples of analog data acquired at combined rates of 2.5 Msamples/sec to 500 M samples/sec. The necessary CCD was not available initially but was developed under subcontract to GARD, INC. by Rockwell International, Electronics Research Division. Two other papers presented at this conference provide details on the CCD itself[5] and the circuitry required to operate it in the manner required[6]. After acquisition, CCD operation is slowed to a convenient output rate of less than 100 Ksamples/sec per CCD or 800 Ksamples/sec per ASR.

INTRODUCTION

The purpose of a data acquisition system is generally to provide information about a system to the user. The nature of the information required varies widely. Simple yes/no or go/no-go data is often appropriate for operational control. Elaborate tables and graphics resulting from sophisticated data processing procedures are sometimes required for scientific research. While the data requirements for operational control and scientific research may vary by orders of magnitude, there is an important element common to both. The user in both cases wants to see only relevant data.

The control operator may need to know how many times a process exceeds its threshold temperature as well as when each instance occurred. A simple printout stating the number of occurrences followed by a list of the time of day when each instance occurred is appropriate. The operator has little use for a tabulation of temperature data listing entries every minute. Further, he cannot afford the time required to delve through copious data separating meaningful results from meaningless records. Clearly, the

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required sorting of records is better accomplished by the data acquisition system operating in accordance with some rules set down by the operator.

The scientific researcher is often faced with a similar situation. The phenomena under study may be characterized by short bursts of relevant data separated by relatively unimportant background phenomena. While the background phenomena are essential in establishing "steady-state conditions" or "base-line" data immediately before and after the event of interest, their continuous presentation to the user serves no useful purpose. Once again, some sorting of relevant and irrelevant data is required of the data acquisition system.

In general, when the information rate or meaningful, relevant data rate is significantly non-constant, the data acquisition system is required to continuously monitor the phenomena and extract the relevant data for the user. Depending on the application, continuous data may or may not be filed historically by the system. Initially, most users request complete historical records as back-up or reference for the extracted data. This procedure can result in copious data if the phenomenon of interest requires wide-band recording techniques. For example, consider the pulse data presented in Figure 1, which is typical of numerous phenomena. The pulse spans roughly 500 μs. The user has chosen to sample this waveform at 50 Ksamples/second or at 20 μs intervals, producing samples of each point indicated. The pulse is represented with approximately 26 samples. In addition to the pulse itself, the user has requested approximately half a pulse width of baseline before and after the pulse, raising the total data required to approximately 50 points, or 1 ms (1000 μs) of recording. Now consider how much data must be recorded to obtain the 50 samples required if real time processing is not employed. Assume this data represents a shock wave generated by an explosive detonation occurring 1000 feet from the point of measurement. Assume the detonation is used as the time reference for the experiment. The shock wave will travel at the speed of sound traversing the 1000 feet in roughly one second. Barring all other considerations, then, at least one second of data must be recorded to acquire the pulse and its time reference. Given some uncertainty in the speed of sound (which is a function of air temperature, humidity, and barometric pressure), perhaps two seconds of good recording time will be used. Note that in the recording period only 1 ms (50 samples) of data plus the instance of occurrence is truly relevant. That is, 50 out of 100,000 samples recorded are relevant, or 99.95% of the data is irrelevant. To this point other factors which extend the recording period have not been addressed. For example, if the recorder requires some sort of speed stabilization, it may begin as much as one minute before detonation. If some other data occurs five seconds after detonation, then the total period extends another four seconds. If, on the other hand, the data occurrence is largely unpredictable, then the recording must span a large enough period to record the data whenever it occurs. It takes little imagination to envision the percentage of irrelevant data growing from 99.95% to 99.995%, or even greater. Still, in this example, the data is recordable with conventional techniques. General purpose equipment can record an/or sort out the relevant data either in real time or from the tapes after the event.

Generically, data acquisition systems which sample and record the kind of data discussed are called transient data recorders. Transients have been traditionally defined as "fast" events occurring randomly in time. From the examples presented, it is appropriate to regard transient data as data characterized by short periods of highly concentrated information spaced by long periods of low information density. The function of a transient data recorder is to detect and record information concentrated in short periods together with sufficient base-line and time data to provide a reference for the user. Transient recorders are usually characterized by data identification via real time data processing and electronic memory sufficient only for the transient itself and data denoting its time-of-occurrence. Note that a transient recorder is not necessarily a wide-band device.

SYSTEM REQUIREMENTS

Now let us consider the data typical for the system under consideration. The data is generally of the same shape as the

pulse already discussed (see Figure 1). However, it is more than 10,000 times faster. The data contains significant frequency components from DC to 100 MHz. Sampling is required at 500 Msamples/second, or at 2 ns intervals. The trailing edge of the waveform is often more than ten times longer and can contain additional wide band data requiring 500 to 1000 samples. Since the user requires a system accuracy of $\pm 2\%$, $\pm 1/2$ LSB, the data must be resolved to 64-levels and encoded to six-bits. Whereas the previous data was manageable with conventional recording equipment, the required sampling rate and subsequent data rate are so high that unconven tional techniques are required. In addition to these functional requirements, the recorder must remotely operate in a severe environment characterized by temperatures varying from $\pm 10^{o}F$ to + $130^{o}F$, shock up to 30g's (1/2 sinewave, 11 ms), and pressures from sea level to 10,000 feet. It must operate through a combined radiation environment of 10 Rad prompt dose acquired at 10^7 Rads/sec plus 10^7 neutron/cm^2, fission spectrum. EMP is considered best described as up to 2 amperes of sheet current containing significant frequency components up to 100 MHz flowing over the module. The recorder must be small (approximately 400 in^3) and low in power dissipation (less than 40 watts). Since the module may be expended in one out of four uses, it must be low in cost. Sampling rate, signal offset, and pre-history (or time-offset) are all remotely programmable. More details on the specification are presented in Table 1.

APPROACHES

The classical approach to transient data recording centers about an analog-to-digital converter linked to digital memory as shown in Figure 2. Data is first filtered to eliminate aliasing, and then accurately sampled and held in analog form for conversion to digital. The linear phase filter is not an off-the-shelf item, but can be fabricated from standard components to conform to the size and power constraints. The sample and hold must maintain an aperture or time uncertainty of sampling of 50 ps (in order to maintain six-bit accuracy for 100 MHz) while operating at 500 Msamples/second. The requisite sample/hold approaches the state-of-the-art but is not large and does not require excessive power.

The 500 Msample/second, six-bit analog-to-digital converter is currently beyond the known state-of-the-art. The general approach taken to converters approaching this speed and resolution is to simultaneously apply the signal to parallel fast-setting analog comparators as shown in simplified form in Figure 3. Each comparator is biased at one of the 63 resolveable levels. The signal is held until all circuitry is settled and the coded output is stored. Additional speed is obtained using additional interleaved rows of comparators. A recent developmental six-bit converter using two parallel rows of converters was operated at 200 Msample/sec[1]. The converter with Sample/Hold requires 175 watts and is housed in a rack mountable enclosure judged to occupy more than 3000 in^3. While its production cost is not known, the circuitry makes extensive use of both custom and standard ECL logic which does not suggest low cost.

Clearly this converter is too slow (200 Msample/sec vs. 500 Msample/sec), too large (3000 in^3 for converter plus sample/hold vs. 400 in^3 for the total system), dissipates too much power (175 watts vs. 40 watts for system), and is not likely to be low cost.

Following the converter is storage for 1000 words of six-bit data, which must be loaded at 500 Msamples/sec. From manufacturers data sheets it appears that an array of 48 ECL memory chips[2] will meet requirements. However, each chip requires 90 ma, typical, @ -5.2V with inputs and outputs open. This amounts to 0.468 watts per chip or more than 22 watts for the 48 chip array. Note that this power does not include the addressing or control functions.

It is clear that the classical high speed transient data recorder falls far short of the design goals. The overwhelming weak point is the analog to digital converter. Therefore, a method which circumvents the high speed, parallel analog to digital converter must be used.

One unconventional form of analog to digital converter is the scan converter. The scan converter can be thought of as similar to a sophisticated oscilloscope. Wideband data (up to 1 GHZ) is written in x, t form onto a special target which retains the trace. The target is then scanned

at slow speed in such a manner that for each increment of time, the value of the input (X) is encoded. Commercially available equipment[3] offers input bandwidth to 500 MHz at low levels (1 GHz at high levels), with resolution at 400 by 320 lines converted to a 512 by 512 digital array. The conversion results in 512 samples resolved to nine bits which are stored in digital memory. The basic unit dissipates 243 watts and occupies approximately 2500 in^3. From the manufacturers literature, there is no indication that the unit is hardened for shock or radiation. However, it will operate over a temperature range of 0^oC to $+40^oC$ and up to an altitide of 15,000 feet. Although not usually sold as a stripped channel the quoted price is roughly $25,000 in singles. Clearly the scan converter is much more suitable for the application at hand. Still it is approximately six times larger than required and dissipates more than six times the power allocated. While its cost is quite reasonable for the performance offered, it is still more expensive than desired. Table II compares both the scan converter and a transient data recorder utilizing the parallel converter previously discussed. Certainly there is other equipment which could be discussed. The two transient data recorders chosen are considered to be representative.

In general, Table II suggests that even the unconventional techniques available today are too large, consume too much power, and in general fall short of the conversion and/or storage requirements. In both cases considered, most of the power and volume is associated with the converter section as well as the conversion performance.

The principle reason that power is high, volume large, and performance stretched to the limit is that data is being converted at extremely high rates. An approach which minimizes high rate data handling may be expected to minimize size and power.

THE SELECTED APPROACH

With the goal in mind of minimizing size and power, let us review Figure 2. The filter is passive and dissipates little power. The sample/hold circuitry is generally low power and small. The next step (conversion) is the problem. The link between sample/hold and conversion is an obvious place for improvement. Data traversing this link is in sampled analog form as shown in Figure 4. It resembles an irregular staircase comprised of uniform width samples. If a device could be found that would accept data in this form, store it briefly, then play it back at a sufficiently slow rate, the remainder of the circuitry could be dramatically simplified.

Generally, this device is referred to as an analog shift register operated in fast (input)/slow (output) mode. It is located between the sample/hold and the converter as shown in Figure 5. It must be able to accept sampled, analog data at varying rates up to 500 Msamples/sec, store at least 1000 samples and then output the data at a rate $\leq$ 1 Msample/sec with less than 1% total distortion.

ANALOG SHIFT REGISTER ALTERNATIVES

Two candidate analog shift registers were considered: the bucket brigade device (BBD) and the charge coupled device (CCD).

At the time of the selection, a 10-cell BBD with JFET switching between capacitor cells was being operated at 50 Msamples/sec, with a cell transfer efficiency of 97%. A 160 cell device was planned. If the 160-cell BBD was operated in the same manner as the 10-cell BBD, ten parallel channels would yield 1600 sample storage loadable at 500 Msamples/sec. If the cell to cell transfer efficiency remained at 97%, then the 160-cell transfer efficiency would be 0.97^{160} or 0.0076. Then less than 1% of the input signal would reach the output. This situation would put extreme demands on dynamic range and require involved data reduction procedures.

Another device considered was the peristaltic charge coupled device (PCCD)[4]. A 128-cell device had been operated at 100 MHz with transfer efficiency exceeding 0.9999. Eight PCCD's in parallel would provide storage for 1024 samples loadable at ranges up to 800 Msamples/sec. Transfer efficiency for 128 cells would be 0.9999^{128} or .987 nearly full signal.

For these and other performance considerations, the PCCD was chosen over the BBD to implement the scheme shown in Figure 5. Since the PCCD was not commercially available and the developer was not interested in working on the system under consideration, a custom PCCD was developed for this system by Rockwell International under subcontract to GARD, INC. and is the subject of another paper[5].

The remainder of the paper relates how the PCCD was integrated with appropriate support elements to build a system complying with the stated requirements.

SYSTEM CONFIGURATION

The configuration of the system is shown in the block diagram of Figure 6. The major areas of the Transient data recorder are the filter, Sample/Hold, Analog Shift Register, Analog to Digital Converter, memory and the control logic. Special attention is given to the integration of the ASR and its peripheral equipment, timing and operation requirements, and packaging.

A filter is included in this system, as in most data acquisition systems, to limit the bandwidth of the processed signal to less than half the sampling frequency in order to eliminate frequency folding, and to reduce unwanted noise. Since eight sampling frequencies are used eight filters are required. The filters are plugable units with the capability of having any three in the system at one time. Status register control determines which will be selected. Due to the high sampling rates of this system, special filters had to be developed.

The sampling rates required by this system are beyond available state-of-the-art sample/hold and A/D conversion systems. For this reason, a sample and shift method was devised that provides time expansion of the sampling which permits the A/D conversion to be done at a much slower rate. A CCD analog shift register is operated as fast input/slow output temporary storage. The CCD used in this system is a 128 cell, 4-phase peristaltic device. To satisfy both the sampling frequency of 500 MHz and storage capacity of the system, eight sample/hold/CCD combinations were operated in parallel. This provides a 1024 word storage capability and requires that the CCD's need operate only at 62.5 MHz at the fastest sampling rate.

The sample/hold circuitry is a conventional voltage sampling design with a linear switch and a hold capacitor but because of the frequency of operation, special design considerations had to be made. The eight S/H's are operated in sequence. However, to eliminate distortion caused by the operation of other S/H, only one S/H gate is permitted to start sampling at any given time.

After 1024 samples have been taken and temporarily stored in the CCD analog shift registers, the CCD's are then read out at a slower rate, multiplexed, and sent to the A/D in the proper sequence. A slow output rate of 100 KHz is obtainable with the CCD's used. The composite rate out of the multiplexer is 800 KHz requiring an A/D with a conversion time of 1.25 μsec or less. There are a number of A/D converters in the 1 μsec to 800 nsec range that are economically priced and small in size. The particular A/D used in this application is an 800 nsec conversion time device. The relatively slow conversion rates of the A/D also permits use of standard "off-the-shelf" MOS, bipolar or CMOS/SOS (when available) memory IC's to be used for system storage.

The system is remotely operated with all external commands stored in non-volatile internal status registers which in turn control all features of the recorder, including the sampling rate, which varies from 500 MHz to 2.5 MHz, the filter selection, and the offset. The operation sequence from sampling of the incoming signal through A/D conversion and storing of digital information in the memory is all controlled internally. The system can operate either in the normal record mode as described above or in the self-check or function check mode. The function check is an internally generated transient pulse that checks the operation of the system. The trigger commands which start a recording cycle can be generated externally or internally. The trigger commands consist of ARM, which enables all circuits, START, which begins the operation of circuits

that have some finite warm-up time but that require sufficient power to warrant limited use (e.g., the CCD drivers), and TRIGGER, which starts the record cycle.

ASR INTEGRATION

The mode of operation of the shift register in the system (i.e., fast input/slow output) indicates that the most difficult interfacing is involved with the input of the CCD and the peripheral circuitry that must operate at the fast frequency. As was intended, the slow output frequency tends to make the interfacing of the output an easier task. Of special concern here is interfacing of the CCD with the Sample/Hold circuitry, the input structure and the phase drivers.

When the sampling gates are off, they must present a high impedance to the hold capacitor to prevent the stored charge from dissipating. In this case due to the high frequency of operation the hold capacitor must be small requiring a very high hold impedance to prevent any leakage. The hold capacitance for the S/H in this system is the input gate capacitance of the CCD. This requires special care in processing of the CCD to insure that the input capacitance is of a small value and constant from CCD to CCD in order to match all eight CCD's. It further means that the input gate is terminated in a high impedance which makes it susceptable to system noise. Coupling within the CCD must be reduced as low as possible to prevent phase drive signal noise from being coupled to the input.

The input of the CCD is a critical point of this system. There are tight specifications on input linearity, accuracy, thermal stability, and dynamic range. Such things as linearity and accuracy cannot easily be compensated for within the system. The high frequency of operation and the range of frequencies involved put further restrictions on the input. The use of 8 CCD's requires that all parameters be closely matched in performance. The CCD input structures considered for this application were gated charge, gated impulse method, and Tompsett type inputs. The gated charge method controls a barrier under an input gate with the input signal. This allows charge to flow over the barrier in amounts proportional to the input signal. This method was discarded because of its relatively poor linearity and thermal stability characteristics. The gated impulse method allows charge to flow for a specific length of time which is dependent upon a pulse width. This method was not used because of the difficulty in accurately controlling pulse widths at these frequencies. The input selected was a 3 gate Tompsett type input. The primary reasons for selecting this type were its improved linearity and thermal stability over the gated charge method. The timing diagram for the selected input is shown in Figure 7. The input signal is applied to gate 2 which controls the height of a barrier. Gate 3 is biased to a fixed well level. Both gate 1 and gate 3 are heavily bypassed to provide isolation for the high impedance of gate 2 from the possible interference from the diffusion and phase drive signals. The gate 2 barrier provides a wall for the fixed well of gate 3 determining the size of the well. The input gate area is flooded with charge; the input diffusion is then shut off and excess charge backflows out of the gate area. This leaves only the well under gate 3 full of charge. The charge can then be transferred to the first transfer gate of the CCD. Since the barrier under gate 2 must always be low enough to pass sufficient charge, the dynamic range is reduced with this method. This can be compensated for by enlarging the area under gate 3. Care must be taken in the design of the input to insure that the sufficient time is available for charge fill and backflow.

The CCD used in this application is a 128 cell, four phase peristaltic device which as been operated successfully at 80 MHz. The drive gate capacitance is approximately 25 pf and the voltage swing on the drive gates is approximately 15 volts. The ideal wave shape for a drive gate is trapezoidal with some finite rise and fall time, since it functions as a push clock (i.e., pushing charge in front of it). At the fast frequency of operation of 62.5 MHz, the rise and fall times are limited to 5 to 8 nsec. This rise time is held through all operating frequencies. Drivers with these characteristics are not readily available, so they were fabricated from discrete components. Of prime concern was

the power dissipation of the drivers. Both power supply requirements and thermal energy dissipation became a problem if the drivers were allowed to operate for an extended period. For this reason, the START command was incorporated into the system. The CCD does have some warm up time required because thermal filling will saturate the cells when it is not in operation. The START command is programmed to occur 50 to 100 μsec prior to the start of recording which sufficiently clears all charge from the CCD's but does not create a power problem. Sufficient filter capacitance was included in the driver to supply power for the limited operation time. This eliminates restrictions put on the system by power supply response times.

The output of each CCD is fed to an amplifier with offset and gain control. These controls are required to provide adjustments for matching of the eight CCD's. Gain is required to increase the signal level to accommodate A/D input levels. Each CCD amplifier is then fed to a multiplexer which recombines the eight parallel paths back to one sequential data path.

TIMING AND OPERATION

The timing for the CCD phase drivers, the S/H drivers, the CCD input diffusion, the CCD output reset, and the CCD output multiplexer is all controlled by a common eight phase generator. At the highest frequency, a sampling aperture time of ±50 picoseconds must be maintained to meet the system specifications. This made it necessary to use extreme care in the selection of components for and the layout of the timing circuitry. Further timing restraints were placed on the system by the fact that the S/H design, when optimized for the highest frequency, would not operate satisfactorily over the full range of sampling rates. The solution was to maintain the S/H at a higher frequency for the lower operating frequencies of the CCD's (see Figure 8). At the lower sampling rates multiple samples and multiple input cycles are being performed during one CCD phase drive cycle but only one is present when the CCD input transfer gate is ready to accept a sample. This tightens the timing constraints of the slower sampling rates which would normally be much less critical than the upper frequencies.

The operational sequence of the system is controlled by a 1024 counter synchronized with the eight phase generator. When a START command is received from external control, the appropriate sample rate clock is gated to the eight phase generator which provides drive to the CCD's and S/H. Upon receipt of a TRIGGER the 1024 counter is set to zero and enabled. The CCD's are loaded in sequence until the 1024 counter indicates that each has received 128 samples. The clock frequency is then synchronously changed to a slower read out frequency which also controls the multiplexer (thru the eight phase generator), the A/D converter and the memory. The CCD data is read out at the slower rate, multiplexed and sent to the A/D in the proper sequence.

A slow output frequency of 100 KHz is attainable without significant thermal well filling. With eight CCD's in parallel, the composite output frequency from the multiplexer is 800 KHz. At this frequency both the A/D converter and memory are economical, small in size, and easy to control.

PACKAGING

The TDR is packaged in an enclosed module that is 29 in. long x 7 in. high by 1.6 in. wide. The overall layout is shown in Figure 9. The high frequency of operation, the timing constraints and a few special interrelationships between components (such as the CCD input gate acting as the hold capacitance for the S/H) dictated that all components in the sample and shift assembly had to have as little distance between them as possible. The solution found to this was a three layer arrangement. The eight S/H circuits were arranged symmetrically around the incoming data at the center of the top board. The timing circuitry and CCD peripheral circuitry was arranged symmetrically around the eight phase generator on the bottom board. The eight CCD's, their bias networks and output amplifiers were arranged on eight small cards perpendicular to the main cards. The eight cards were so arranged that the CCD input gate was at the top of the CCD card directly below its respective S/H gate. The bottom of the CCD card was then adjacent to its peripheral circuitry. The S/H timing

and drive signals from the lower board were transferred across the CCD board on microstrip. The advantage of modular CCD boards is that since all adjustments for matching of the eight CCD's are on these boards, the CCD's can be matched prior to installation in the system and replacements of CCD's can be accomplished without modification to the larger boards.

Because the module is closed, the thermal load becomes significant. The most heat-sensitive component is the CCD, since at higher temperatures thermal well filling is increased, limiting the slow read out frequency. Most of the heat is generated in the timing and CCD peripheral circuitry. Because of the close proximity of these circuits, special precautions had to be taken. Heat sinks are mounted on the side of the module closest to the heat generating boards. Air at a rate of approximately 50 CFM will be passed over these fins. Thin silicon rubber sheets are placed between the boards and the module walls to increase conduction. Heat reflectors are used between the timing and CCD peripheral board and the CCD's. This reflects the heat back to the heat generating board and out to the heat fins. In a less hostile environment, the module could be opened allowing for convection or air flow thru the module. This would eliminate the need for the heat sinks, silicon rubber, and reflectors described above.

RESULTS AND CONCLUSIONS

A system breadboard has been built and operated. Testing has indicated that the CCD will not operate in the intended transient radiation environment. A redesign is presently being done on the CCD to incorporate radiation hardness. Calculation on the proposed design indicate that the new devices will be able to withstand 50 rads gamma. The proposed design will include a differential channel along with thinning techniques and selection of materials. The differential channel will help compensate for thermal and noise effects in the system as well as well filling due to radiation.

REFERENCES

1. H. J. Pfiffner, "Development of High-Speed Analog-to-Digital Data Converter", June, 1974.

2. Fairchild Semiconductor Preliminary Data Sheet, "ECL Isoplanar Memory F10405".

3. TEKTRONIX Catalog, "R7912 Transient Digitizer".

4. L. J. M. Esser, "The Peristaltic Charge Coupled Device", International Electron Devices Meeting, Washington, D. C., December, 1973.

5. Y. T. Chan, "Extremely High Speed CCD Analog Delay Line", International Conference on the Application of CCD's, October, 1975.

6. D. A. Gradl, "High Speed Operation of CCD's", International Conference on the Application of CCD's, October, 1975.

TABLE 1

TARGET SPECIFICATION

Data Conversion	
Sampling Frequences (MHz)	500, 250, 100, 50, 25, 10, 5, 2.5
Input Filter Freq., 3 db (MHz)	100, 50, 20, 10, 5, 2, 1, .5
Aperature	± 50 ps
Resolution	6 bits
Accuracy	1%; 2% on system
Storage Capacity	1000 samples
Triggers	Internal and external
Size	7" x 2" x 29" (406 in^3)
Power Dissipation	40 watts
Environment (Operational)	
Radiation (gamma)	10^7 rads/sec 10 rad total gamma dose
(neutron)	10^7 neutrons cm^2
Shock	30g, 11 m sec in each direction
Pressure	sea level to 10,000 ft.
Humidity	93 ± 5 per cent
Temperature	+ 10^0F to 130^0F
EMP	2 amps sheet current, to 100 MHz

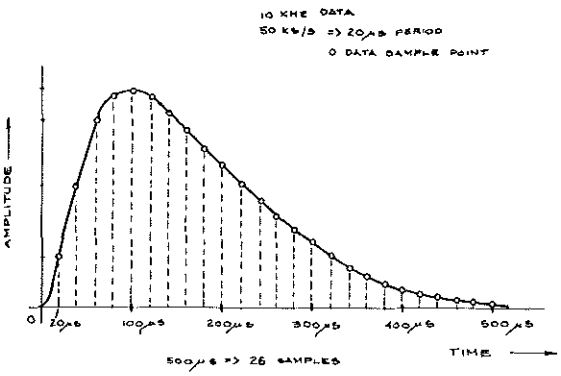

Figure 1. Sampling of Typical Pulse Data

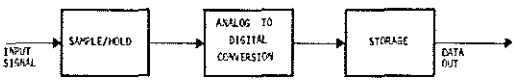

Figure 2. Conventional Transient Data Recorder

Table II

TRANSIENT DATA RECORDER COMPARISON

	Parallel Converter	Scan Converter	Requirement
Maximum signal bandwidth (MHZ) (5:1 quantizing ratio)	40	1000 high level 500 low level	100
Maximum sampling rate (M samples/sec)	200	100,000	500
Resolution (bits)	6	9	6
Storage (samples)	1000 or more	500	1000
Volume ($in.^3$)	4000	2500	400
Power dissipation (watts)	220 est'd	240	40
Cost ($K)			
Singles	80 est'd	25K	14
32	50 est'd	18K	10

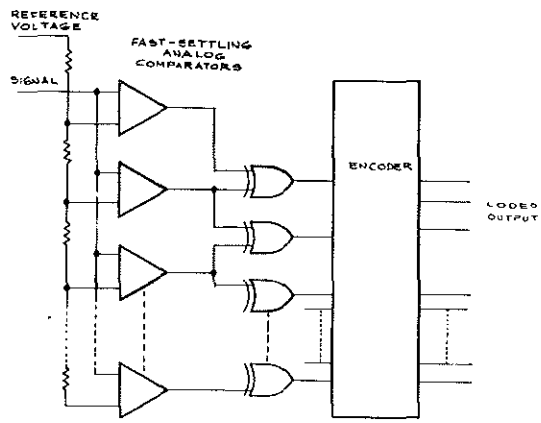

Figure 3. Typical Parallel Converter

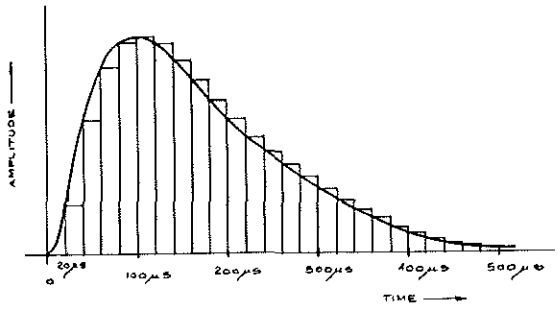

Figure 4. Analog Samples of Pulse Data

Figure 5. ASR Transient Data Recorder

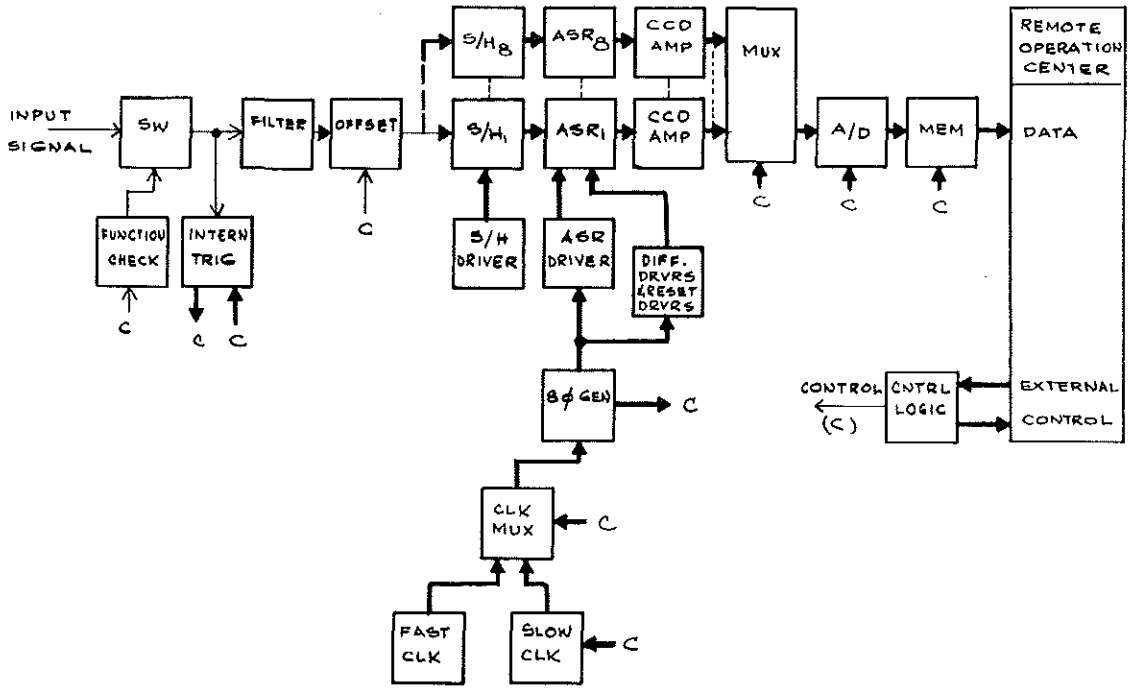

Figure 6. Transient Data Recorder Block Diagram

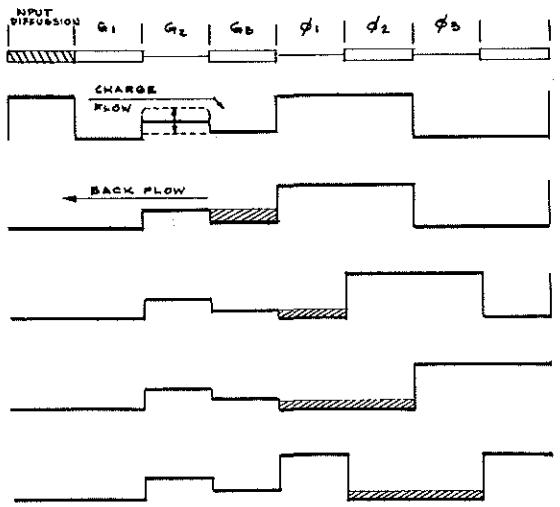

Figure 7. CCD Input Timing

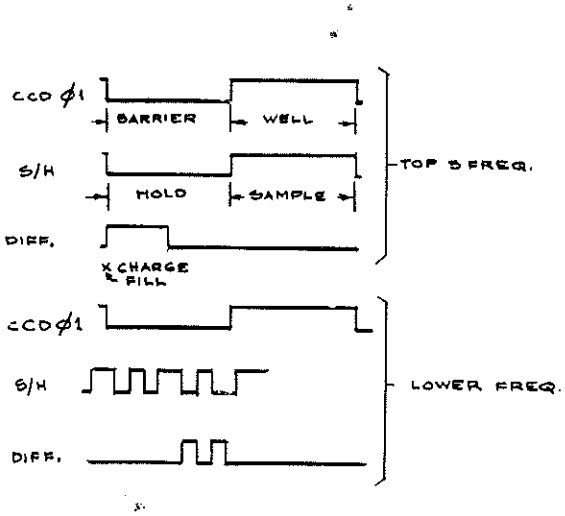

Figure 8. Sample and Shift Timing

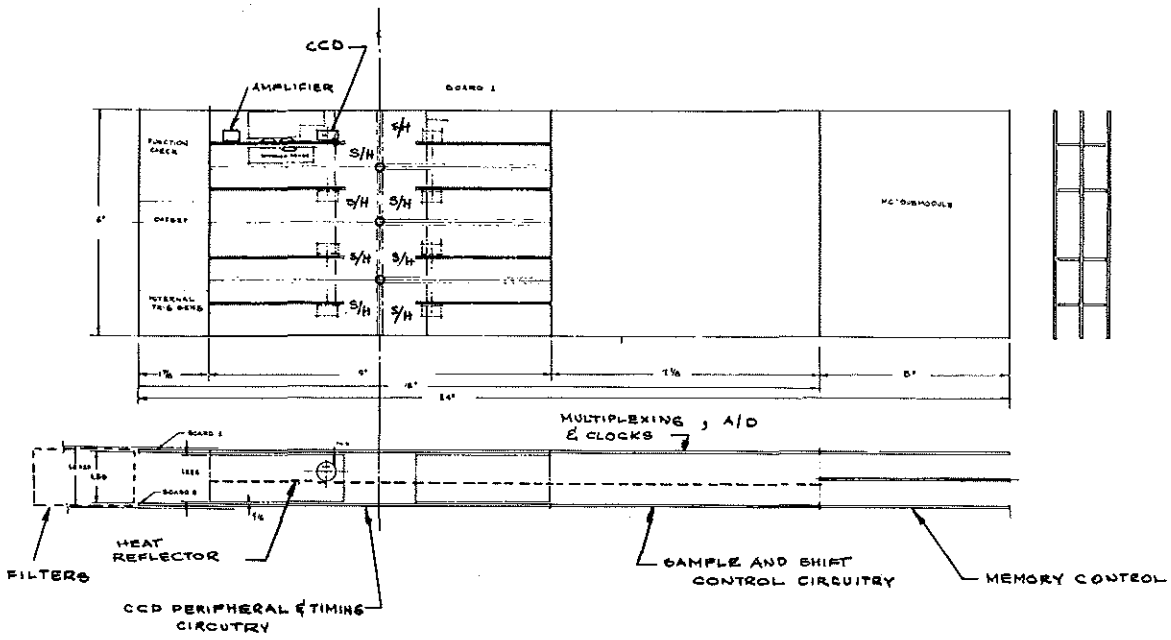

Figure 9. Transient Data Recorder Assembly