EXTREMELY HIGH SPEED CCD ANALOG DELAY LINE*

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ABSTRACT. An N-channel epitaxial ion beam doped buried channel CCD has been fabricated and used to obtain time expansion of sampled analog data. Pulse trains containing up to 130 pulses of analog data were loaded into the device at 105 Mpps. The signal was then transferred out of the CCD for display and examination at 100 kpps. The fast-input/slow-output mode of operation circumvented on-chip high frequency difficulties, reduced the average power requirement of the driving circuitry, and provided a method of observing the effect of high transfer rates on charge transfer efficiency.

The device is a four phase double-overlapping gate structure with an ion implanted/epitaxial deeply buried N-channel. Gate length for this device, in the direction of charge propagation is 0.2 mils (5 μm). Each cell has a 10 mil wide channel which allows a full cell to contain about 0.76 pico coulombs of charge and permits operation over a wide dynamic range. Using push-clock waveforms with voltages switched between +3 to +13 volts, the device exhibited transfer efficiencies in excess of 0.999 per cell. This charge transfer efficiency was observed to be independent of the operating rate. The transfer inefficiency has been attributed to bulk traps with a time constant of 550 μsecs. Output voltages as high as 1.2 volts were observed on the output FET. Trap noise for a full well is characterizable by a sigma of 0.6 mV. No additional noise was observed in the fast/slow mode operation when compared with 500 KHz operation. Linearity of the device and background leakage charge have also been characterized and data is presented herein.

INTRODUCTION

An N-channel epitaxial ion implanted buried channel (peristaltic) CCD has been used to obtain time expansion of data. Input pulses of analog data have been inserted at a rate up to 105 Mpps, up to a maximum of 130 pulses. After acquiring the signal the operating rate of the device was reduced to 10^5 pps and the acquired signal was displayed and examined.

Normally CCD devices transfer the final portion of charge under a given gate from a location which is so near to the transfer gate surface that the effect of the transverse field is negligibly small. This effect limits the operating speed with which good transfer efficiency can be obtained to around 20 MHz. In order to operate at higher frequencies, Esser introduced the peristaltic CCD which transfers charge in a channel several microns below the surface.[1] This configuration was obtained by using epitaxial layers grown on silicon substrates. Because the transverse electric field is very strong at the charge transfer area, the charge can be moved very rapidly out of each cell and, therefore, this type of CCD has been operated at very high frequencies.

DEVICE STRUCTURE

The device discussed here is a 130 cell, four phase CCD. It was fabricated using an N-type epitaxial layer grown on P-type silicon. The dopings of these layers were 1×10^{15} and 5×10^{14} cm, respectively. A cross sectional view of the

design is shown in Figure 1. A four phase overlapped Al propagation gate structure was employed as the driving structure. Silox was used as insulation between the two gate layers. The entire gate structure was formed on a layer of SiO_2 under which was the ion implanted layer. The ion implantation was followed by annealing for 1 hour at 1000°C. This process made the final SiO_2 layer 1500Å thick. Because the device was intended for high speed operation, gate length (in the direction of propagation) was made as small as practicable, i.e., 0.2 mils. This was the spacing for the lower gate electrodes. A 0.225 mil line width for upper gate electrodes was used in order to provide adequate overlap over the lower gates. The total cell length consisting of 4 gates was 0.8 mils. The channel width was 10 mils in order to provide sufficient charge per cell. Referring to the figure, the first gate on the left was used as an input control electrode. A built-in FET amplifier as well as a diode were designed into the structure as outputs. Figure 2 and Figure 3 show photographs of the input and output regions of a finished device. The complete chip consisting of 2 PCCDs, a smaller test CCD and auxiliary test circuitry is shown in the photo of Figure 4. The N+ input and output diffusions shown in Figure 1 and discernible in photos provide good ohmic contact. The P+ diffusion around the CCD channel, also observable in the photos and illustrated in the drawing, acts as a channel stop in order to contain the active charges. Outside the P+ channel stop is an N+ diffusion which functions as a leakage sink. This feature is added in order to remove all leakage currents generated outside the P+ channel stop, a feature which is very important if these devices are to be used on substrates containing other active electronic devices.

HIGH FREQUENCY CCD DRIVER

The drive circuit supplies all gate voltage to operate a CCD with 4 phase drives. The phases are designed to be individually adjustable, although this has not been critical. The charge input was supplied from an external pulse generator which was synchronized with the counter in the driver circuit. For maximum speed, the device operates with 128 fast cell transfers, then 128 slow cell transfers.

The control logic for switching between fast and slow is done by MECL III and MECL 10000 series IC's. The block diagram is shown in Figure 5. Basically, the tester consists of three parts:

1. The logic circuit which controls the start/stop function and the changing of the clock rates;
2. The driving amplifiers which provide the gate voltages required to operate the CCD;
3. The external pulse generator which provides CCD input charge.

The logic circuit in Figure 5 has two clock frequency inputs; one for high and one for low speed operation. Each of the inputs goes through a synchronized switching circuit. When the high rate counter is activated, the high frequency clock is gated on at the beginning of a cycle. When counter sets to the low state, the low frequencies are passed through in the same way. Then the clock frequency is divided by two to obtain 4-phase voltages. Then this 4-phase square wave is amplified to more than 10 volts peak-to-peak and A.C. coupled to the CCD propagating gates. Each gate has its own D.C. bias adjustment.

The amplifier is a differential amplifier using two 2N5583's, followed by an emitter follower to lower the output impedance. The rise and fall time is around 5ns.

FAST/SLOW DEVICE OPERATION

To perform the required task of time expansion, the device was operated in fast/slow mode. First, the circuitry described above was used to operate the CCD in the fast mode. Signal data to be expanded were applied to the inputs and the entire device was filled with packets of analog signal charge. Next, the logic was switched to the slow mode, the input was gated off, and the signal charge packets were propagated to the output transistor for further processing or display. Several devices have been tested under fast input/slow output operation. The devices were operated through 130 cycles of high speed charge transfer followed by 130 cycles of low speed transfer. The timing diagram is shown in the drawing of Figure 7. As the input pulse is moved N cycles, the output is delayed the same number when it is run at low

frequency. Hence, the time expansion is proportional to the ratio of the high speed to low speed operation. The output and the input of the PCCD is shown in the oscilloscope photo of Figure 6. For this test the high speed input was at 62.5 Mpps and the slow speed output was at 100 Kpps.

Two signal pulses are visible both in the input and output traces of the CCD. The lefthand pulse, which emerges first in time, has been transferred through 110 cells at 62.5 MHz and 20 cells at 100 KHz. The right hand pulse has been transferred through 7 cells at 62.5 MHz and 123 cells at 100 KHz.

It was noted that transfer efficiency remains relatively constant over a wide range of operating frequencies. By varying the time of insertion of a single input pulse, the charge packet can be caused to traverse the CCD under any combination of fast/slow transfers totaling 130. In all cases, the transfer efficiency was found to be constant. The values were measured in excess of 0.999 per cell.

The low frequency limitation to slow playback is the thermal generation of carriers which fill the wells. The cumulative effect of thermal generation of charges becomes increasingly apparent at low frequencies and long device lengths. This effect is shown in the oscilloscope photo of Figure 8, as a continuous ramp buildup due to the thermally generated charges when the device is operated in the fast/slow mode.

INPUT LINEARITY

In order to achieve linearity and reduce the effects of input frequency variation upon quantity of input charge, our work utilized the input structure shown in the sketch, Figure 9a. The first gate (nearest the input diffusion) is the control gate G_1. The other gates shown are transfer gates. As schematically shown in Figure 9b, the input N+ diffusion is pulsed more negative than gate G_1 so that electrons are injected through G_1 and ϕ_1. Gate 2 is at a lower potential than the N+ region so that electrons are blocked by this barrier from continuing along the CCD channel. The next step labeled 9c shows the N+ region returned to a voltage higher than G_1. Some of the electrons under gate ϕ_1 now flow back. Hence, the surface potential under ϕ_2 will be level with G_1. The next step, 9d, shows the transfer of this charge into the active CCD channel by increasing the voltage of gate ϕ_2. Figure 9e shows the charge completely transferred to the CCD channel and the ϕ_1 and ϕ_2 gate voltages are returned to their previous values, thus starting the next cycle. The input/output transfer characteristics at 62.5 Mpps were measured and plotted. The results of this are shown in Figure 10. Additional information about the linearity of the device was derived from spectrum analysis of the output when driven with a low harmonic content sine wave input. Photographs of these experimental data are shown in Figures 10a and 10b.

Additional tests using 2-phase instead of 4-phase propagating drives indicate a reduction to 70% of previous output level with a slight degradation in linearity.

TRAPS

The time constant of the bulk traps of this device was measured. Our method of measurement consisted of running the CCD until all cells are empty; then transferring a few full packets of charge into the device so that the traps are filled. The inputting of charge is then stopped. When the input charge has stopped, the traps start to relax and release some of their charges. In order to measure the charge released at a particular time, a nearly full packet of charge is transferred to the CCD. Since part of this charge will now fill the empty traps sequentially, the traps will now take up the amount of charge which they have released during the decay time. Because the test charge will fill the vacated traps, the output level of this test charge will be less than the output if no traps were present. The difference in charge corresponds to the number of traps empty at the time the test charge passes through the device. Figure 11 is the plot of the relative number of traps remaining filled vs. time for two different operating frequencies. The parallel curves show that the trap release time constant (550 μsec) is independent of operating frequency.

Other charge trapping mechanisms have been looked for but not observed. Surface state traps should not be involved since the

active charge carrying area in this device is isolated from the surface by the ion implanted layer.

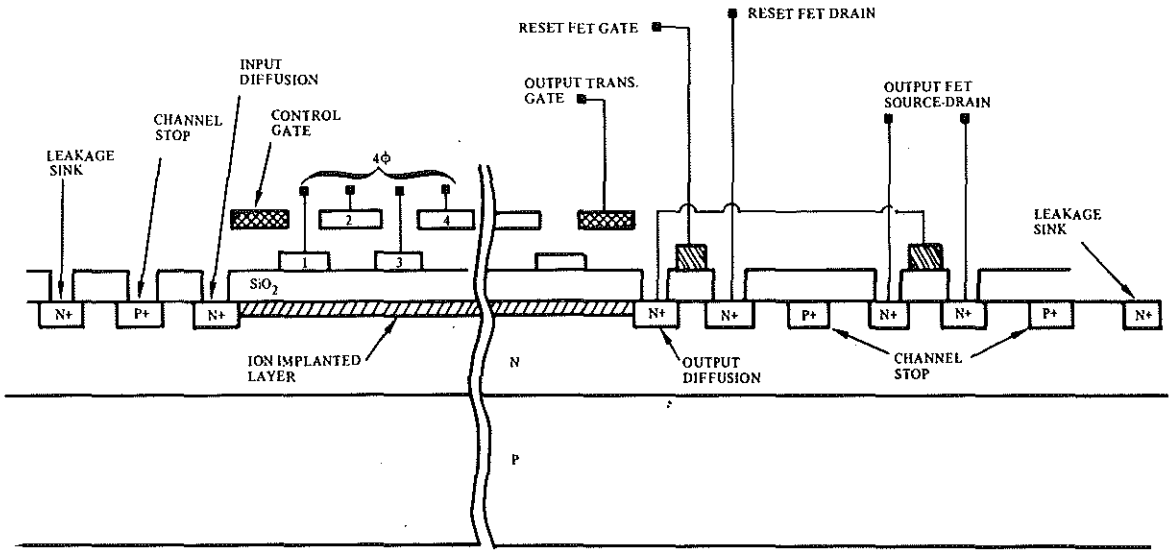
CONCLUSIONS

A CCD has been operated at rates up to 105 MHz. The present upper limit of operation is believed to be a function of the test circuitry and not of the CCD. It has been observed that charge transfer efficiency did not degrade with frequency of operation, and the results were only limited by our test equipment. From observations and experiments performed so far, it is believed the device will be able to be operated to at least 200 MHz. Bulk states which contribute to charge transfer inefficiency appear to be characterizable by a single trap level having a time constant of 550 μsecs.

Noise and dynamic range of the device were found to be in close agreement with the values predicted theoretically for this design.

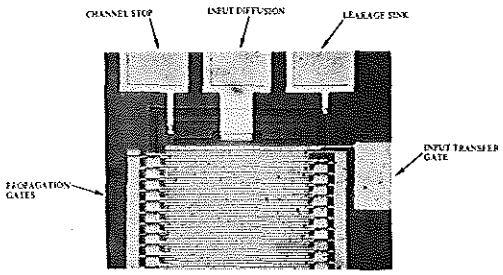
*This work was performed under subcontract by the Electronics Research Division of Rockwell International Corporation for GARD, Inc. performing under contract to Sandia Laboratories, a prime contractor of the U. S. Energy Research Development Administration.

1. Esser, L.J.M., "Peristaltic Charge Coupled Device: A New Type of Charge Transfer Device", Electronic Letters, Vol. 8, P. 620, Dec. 1972.



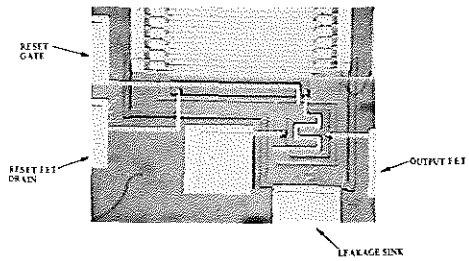
Peristaltic CCD - Cross Section (In Direction of Charge Propagation)

Figure 1.



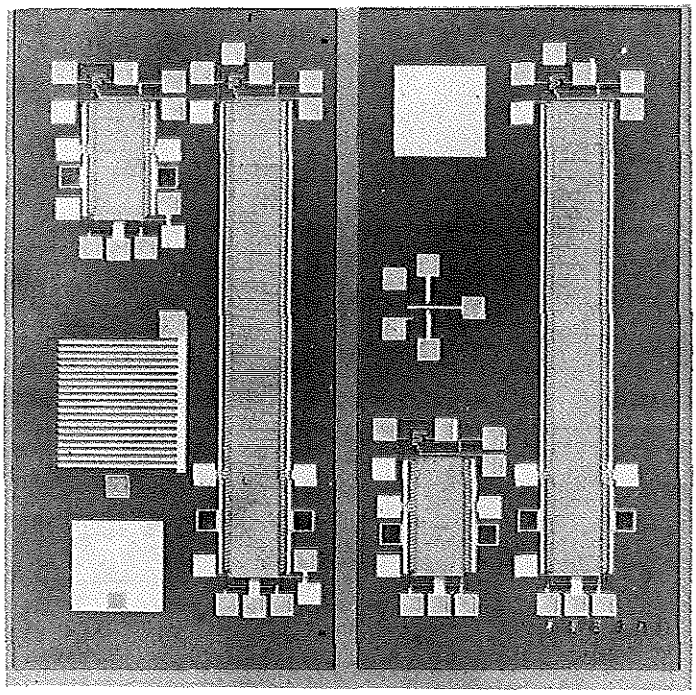
Photograph of Input of PCCD

Figure 2.



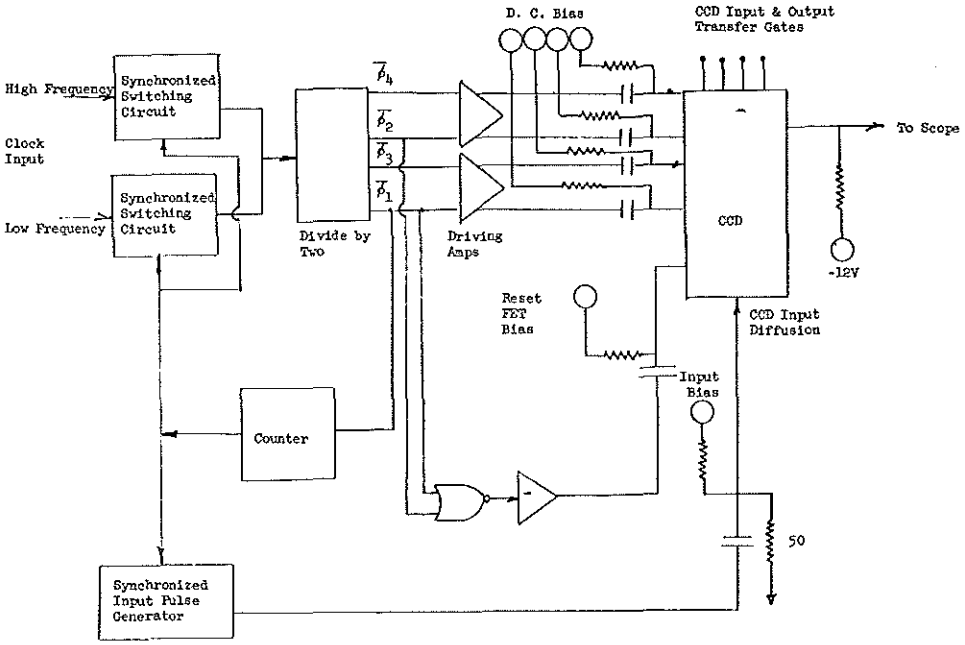
Photograph of Output of PCCD

Figure 3.



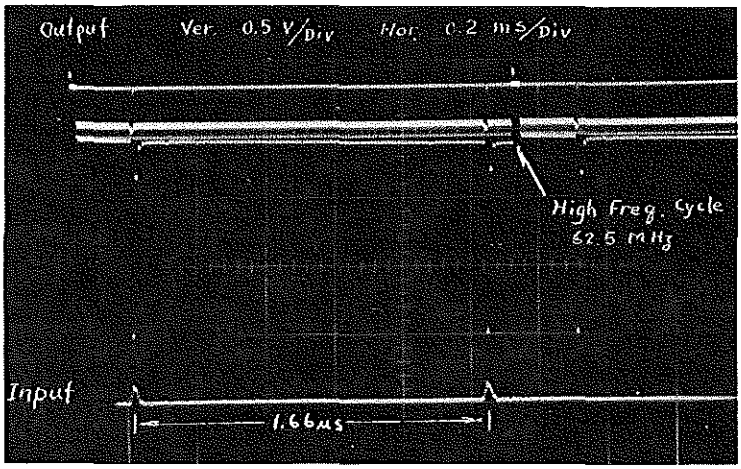
PCCD Chip Design

Figure 4.



Block Diagram of CCD Test Circuitry

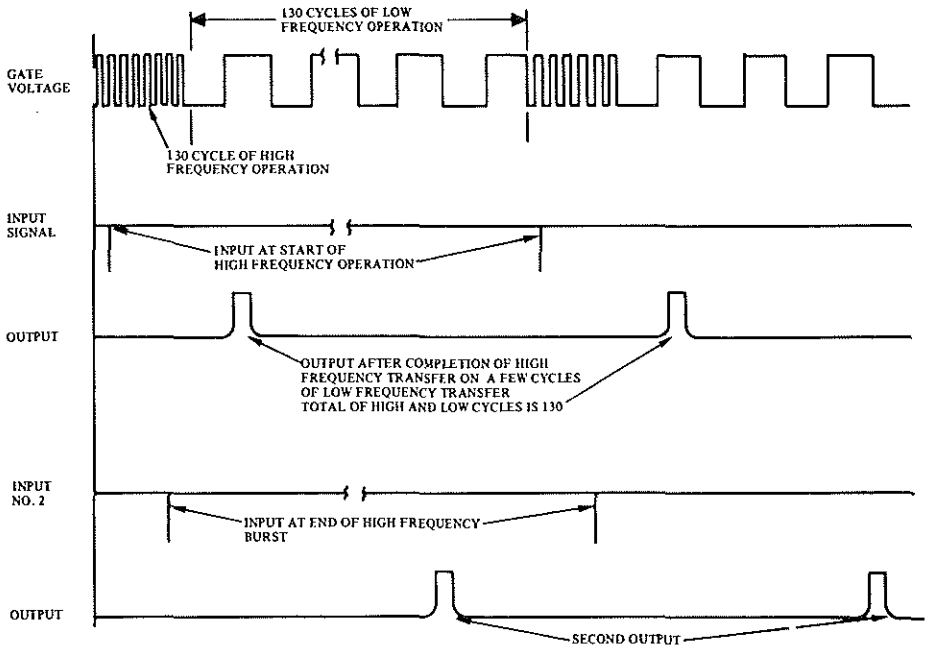
FIGURE 5



Comparison of Small and Large Number of High Speed Transfers in CCD, Output Pulse of Small Number (7) is on Right, Large Number (110) is on Left.

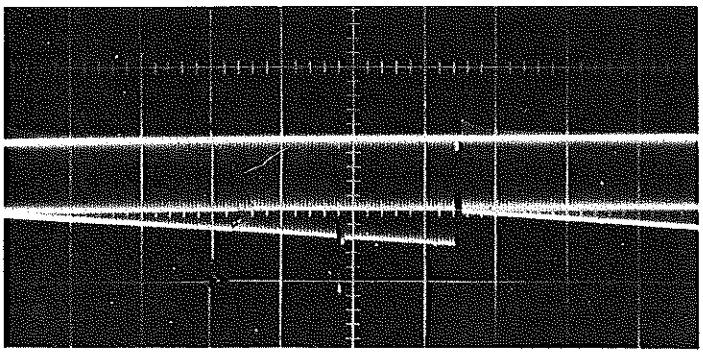
Output of Fast/Slow Operation

Figure 6.



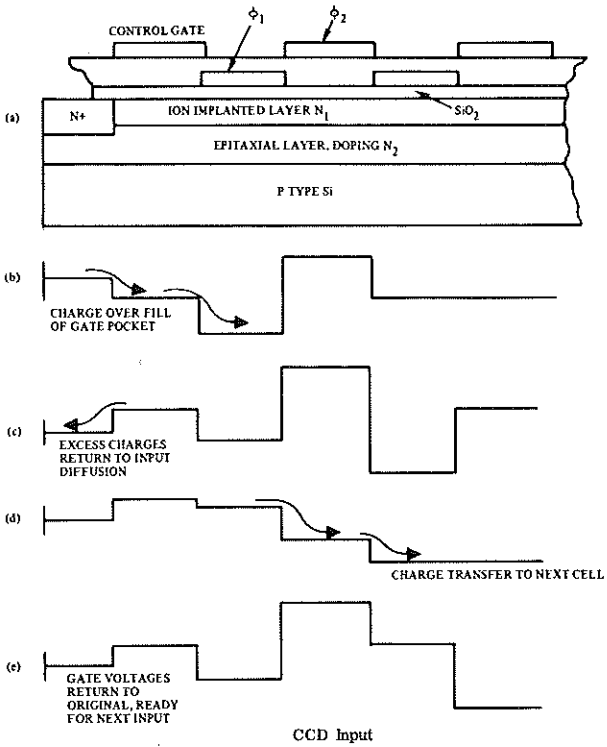
Timing Diagram Fast/Slow Operation

Figure 7.



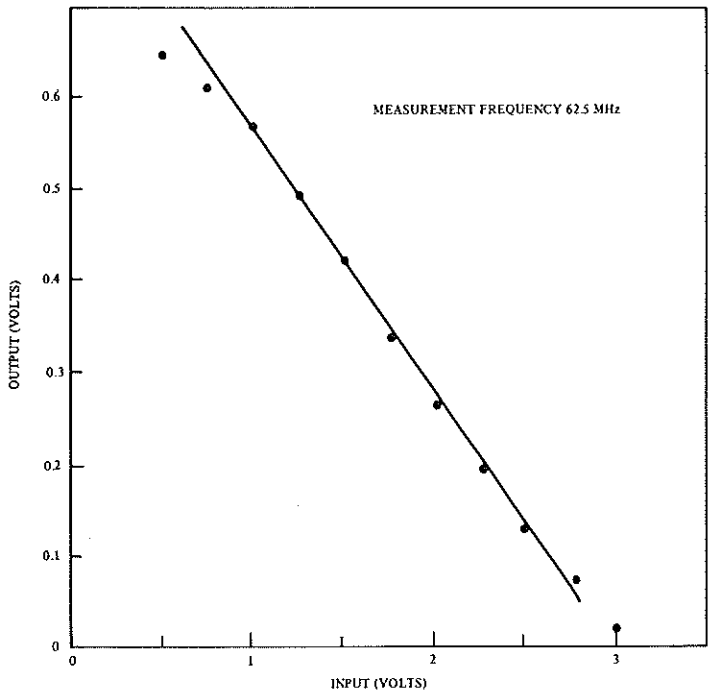
Dark Current Output at 130° F in F/S Mode
(62.5 MHz/100 kHz)

Figure 8.



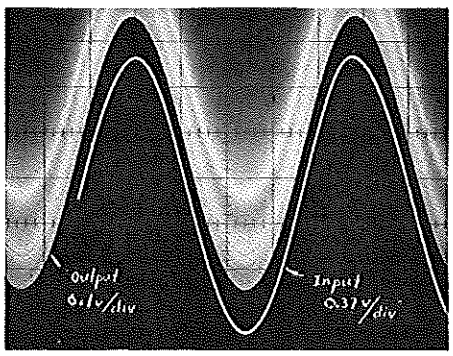
CCD Input

Figure 9.



Peristaltic CCD Linearity

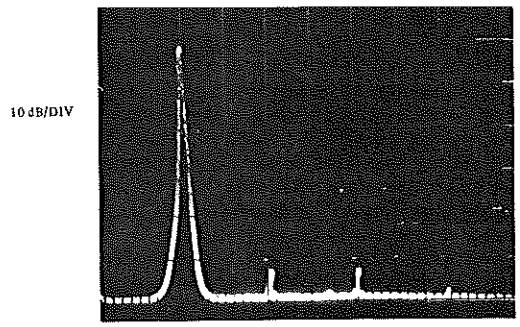
Figure 10.



0.1 μSEC/DIV

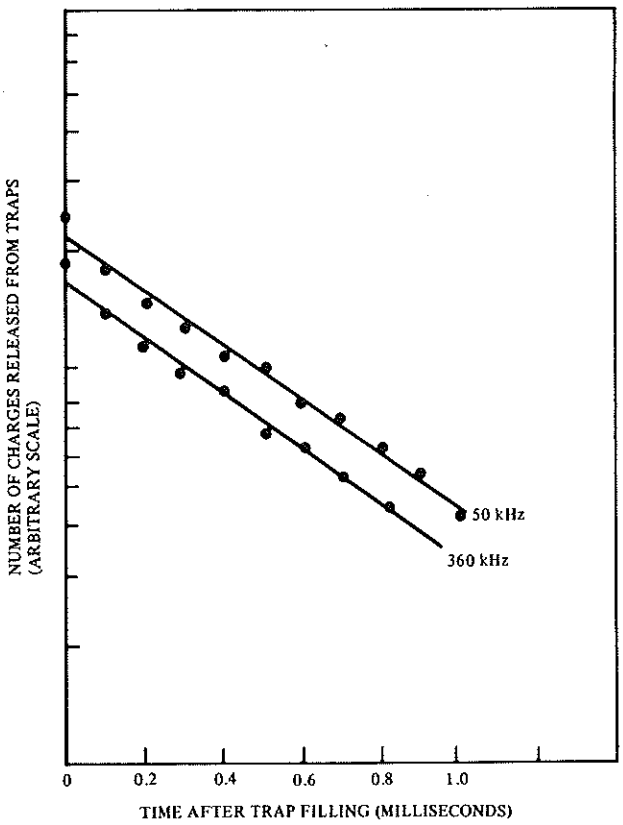
Sinewave Input to PCCD and Its Output

Figure 10a.



Spectrum of CCD Output With 5 kHz Input Frequency

Figure 10b.



Bulk Trap Release Vs Time

Figure 11.