LOW TEMPERATURE SILICON CCD OPERATION

A. J. Steckl
Electronics Research Division
Rockwell International Corp.
Anaheim, California 92803

ABSTRACT. Experimental results are presented on the operation of bulk (peristaltic) and surface channel silicon CCD's at cryogenic temperatures. The transfer inefficiency of both devices exhibited a similar pattern as a function of temperature between 300°K and 30°K, namely a broad curve with a minimum around 77°K. At that temperature the transfer inefficiency per cell of the two devices was measured to be ϵ(PCCD) = 5.5 x 10^{-4} and ϵ(SCCD) = 4 x 10^{-4}. The bulk channel CCD exhibited a sharp transition in transfer inefficiency at the onset of freeze-out, increasing from ϵ = 1 x 10^{-3}/cell at 30°K to ϵ = 1 x 10^{-2} at 18°K and then leveling off to ϵ = 2 x 10^{-2} at 4.8°K. The surface channel CCD did not show a freeze-out transition in transfer inefficiency, rather it increased slowly to a value of ϵ = 1.4 x 10^{-3} at 5°K.

I. INTRODUCTION

The low temperature operation of silicon charge coupled devices, in the range between 5°K and 80°K, is a critical factor in the utilization of CCD's in infrared systems [1]. The temperature of operation of Infrared Charge Coupled Devices (IRCCD) is a function of a number of factors: the type of CCD, the wavelength region of interest, the IR detector material, the sensitivity requirements, etc.

Infrared CCD's (IRCCD's) fall into two categories: monolithic and hybrid. The monolithic IRCCD concept generally uses the standard CCD structure with the substrate consisting of a narrow bandgap or an extrinsic semiconductor sensitive to IR radiation. In the extrinsic semiconductor substrate case the photogeneration is an extrinsic process where only the majority carriers are mobile. The temperature of operation must, therefore, be kept in the neighborhood of freeze-out or below to minimize the dark current. With silicon being used for the substrate, that temperature can vary depending on the wavelength region of interest from 15°K for Si:As with $\lambda_{co} \simeq 24\ \mu$m to 50°K for Si:In with $\lambda_{co} \simeq 8\ \mu$m. The CCD operation in this case can be either in the accumulation mode [2] if the same elements are used for detection and readout or inversion mode if the detection and readout functions are separated but still integrated on the same chip.

The hybrid IRCCD consists of the coupling of any one of various types of IR photodetectors to a silicon CCD shift-register unit. In the hybrid structure, the functions of detection and signal processing are performed in distinct but integrable components. The role of the silicon CCD in this case is that of a signal processor performing appropriate functions, such as multiplexing, amplification, correlation, delay-and-add, etc. The temperature of operation is once again dictated by the detector requirements and could fall anywhere from 5°K to ~ 200°K.

Since on the one hand the great majority of detectors are operated at ~ 80°K or below and on the other hand the most important questions to be resolved lie in the operation in the freeze-out region, we have concentrated our investigation of the low temperature CCD operation to the 5°K to 80°K temperature range.

II. DEVICE STRUCTURE AND OPERATION

Both bulk channel and surface channel CCD's were investigated. The epitaxial bulk (peristaltic) channel CCD (PCCD) [3], [4] with its high frequency of operation is of great interest for large IR focal plane arrays where a high data rate is required for the readout of all detectors in one frame time. The PCCD used is an n-channel epitaxial ion implanted device of 130 cells with an 0.8 x 10 mil^2 cell size (see Fig.1). The p-type substrate has a doping of 5 x $10^{14}/cm^3$ and the 5 μm thick epitaxial layer is doped at 1 x $10^{15}/cm^3$. The driving gate system consists of a two-level overlapped Aℓ structure with a silox intergate isolation layer. A cross-section of the device is shown in Fig. 2. The high frequency room temperature operation of this device is discussed by Y. T. Chan et al [4], who report a present high frequency limit of 105 MHz.

The surface channel CCD (SCCD) is a p-channel device [5] with 100 cells and 8 input taps spaced every 12 cell, as shown in Fig. 3. The taps are designed for the coupling of IR detectors in a hybrid IRCCD structure. The channel width is 2 mils and the cell size 1 x 2 $mils^2$. The gate structure is the same as for the PCCD described above, namely two-layer overlapping Aℓ gates. The substrate doping is~1 x $10^{15}/cm^3$.

III. EXPERIMENTAL RESULTS

For the low temperature operation, the devices were placed inside a dewar and connected via an "umbilical" cord to a rack containing the CCD electronics (see Fig. 4). The operating temperature was varied through the use of refrigerants with different boiling points (helium, neon, and nitrogen) and a heater located on the cold finger. The temperature was monitored with a calibrated temperature sensitive resistor. The operating voltages for either devices did not change greatly with temperature, the only exception being the output reset FET which below freeze-out required considerably greater bias voltages to reset properly. For comparison purposes, both CCD's were operated at the same clock frequency, f_c = 10 KHz.

The transfer inefficiency per cell of the PCCD is plotted as a function of temperature in Fig. 5. At 300°K the transfer inefficiency per cell of this particular PCCD was $\epsilon = 1.2 \times 10^{-3}$. It should be pointed that since our investigation was of a general nature, no effort was made to choose devices with maximum performance [6]. At liquid nitrogen temperature, 77°K, the transfer inefficiency has decreased to $\epsilon = 5.5 \times 10^{-4}$. For temperatures between 77°K and 30°K, the pattern is reversed with the transfer inefficiency now slowly increasing with decreasing temperature. At 30°K the transfer inefficiency is $\epsilon = 1 \times 10^{-3}$, which is approximately the same value as at room temperature. Below 30°K, the transfer inefficiency increases abruptly, an order of magnitude over a range of ten degrees to $\epsilon = 1 \times 10^{-2}$ at 18°K. Finally, below 18°K, ϵ continues to increase but much more gradually and it approaches what appears to be a saturation level of 2×10^{-2} at 4.8°K.

The major factor contributing to the transfer inefficiency of a peristaltic CCD are the bulk traps [7]. To measure the trap emission time constant charge is first introduced into the CCD to fill all the traps. A second charge packet is introduced after a variable time interval, Δt. The output corresponding to the second packet will be a function of the number of traps empty at time Δt and thus capable of capturing charge: $A = A_o\, e^{-\Delta t/\tau_e}$. The output signals for various time intervals are shown in Figure 6 (left hand axis) for the PCCD operated at 80°K and clocked at 10 KHz. The trap emission time constants are obtained by plotting $\ell n(A_o/A)$ vs Δt on the same graph (right hand axis). A value for A_o of 55 mV is obtained by extrapolating the curve to the origin. A time constant with an apparent value of 0.26 mV is calculated from the data. At room temperature, only one time constant was found [4] with a value of 0.55 ms was found for the same device.

The transfer inefficiency of the SCCD is shown as a function of temperature in Fig. 6. Between 300°K and 30°K, the general behaviour is very similar to that of the PCCD with an apparent minimum of $\epsilon = 4^{-5} \times 10^{-4}$ at 77°K. However, below 30°K the SCCD does not exhibit the same transition region shown by the PCCD at the onset of freeze-out. Rather only a gradual increase in transfer efficiency is observed to 5°K where $\epsilon = 1.4 \times 10^{-3}$.

In conclusion, both bulk channel and surface channel CCD's have been shown to operate at temperatures as low as $5^{\circ}K$.

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REFERENCES

1. For a review of IRCCD's see A. J. Steckl, R. D. Nelson, B. T. French, R. A. Gudmundsen and D. Schecter, "Application of Charge Coupled Devices to IR Detection and Imaging", Proc. IEEE, Vol. 63, p. 50, Jan. 75.

2. R. D. Nelson, "Accumulation Mode Charge Coupled Device", Appl. Phys. Lett., Vol. 35, p. 568, Nov. 1974.

3. L. J. M. Esser, "Peristaltic Charge Coupled Device", Electronics Letts., Vol. 8, p. 620, Dec. 1972.

4. Y. T. Chan, B. T. French and P. E. Green, "Extremely High Speed CCD Analog Delay Line", Proc. 1975 CCD Applications Conf., San Diego, CA, Oct. 1975.

5. The surface channel CCD designed by R. D. Nelson.

6. The same device has been operated with $\epsilon\,(T = 300^{\circ}K) = 3 \times 10^{-4}/\text{cell}$.

7. A. M. Mohsen and M. F. Tompsett, "The Effects of Bulk Traps on the Performance of Bulk Channel Charge Coupled Devices", IEEE Trans. Electron Devices, Vol. ED-21, p. 701, Nov. 1974.

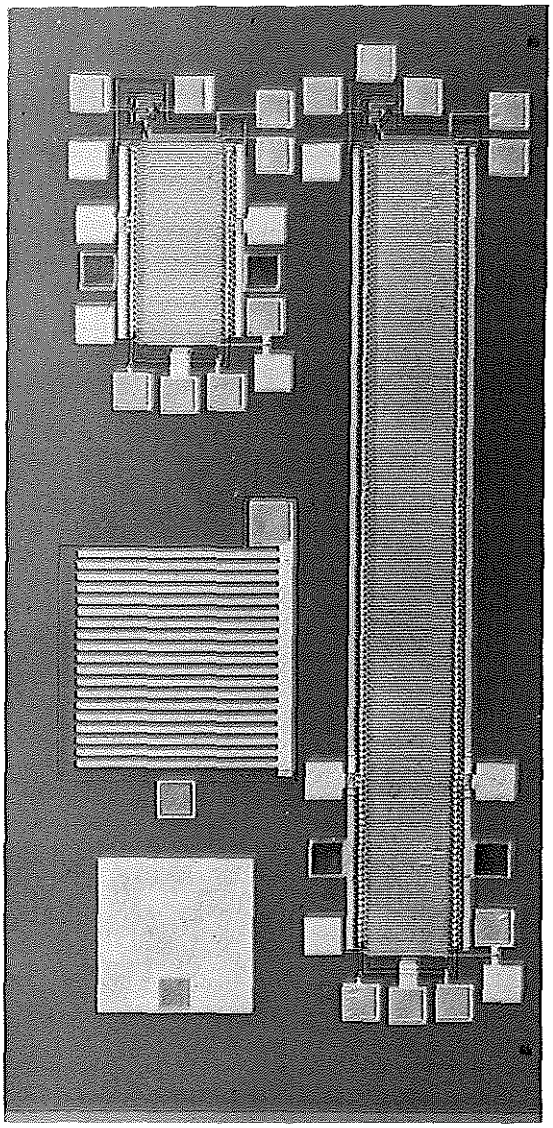

Fig. 1 Photograph of Peristaltic CCD's: 32 cell and 130 cell shift registers.

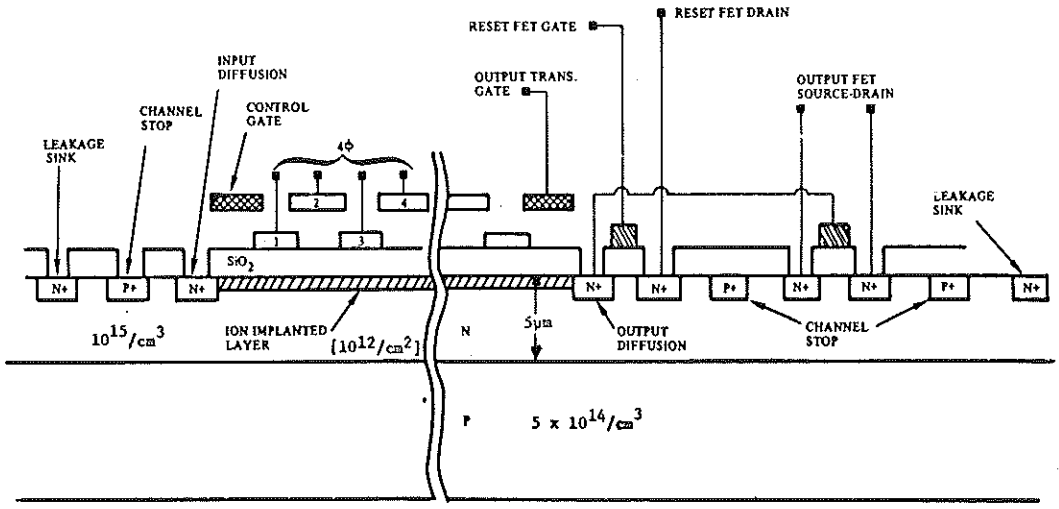

Fig. 2 Cross section of PCCD in direction of charge propagation [4].

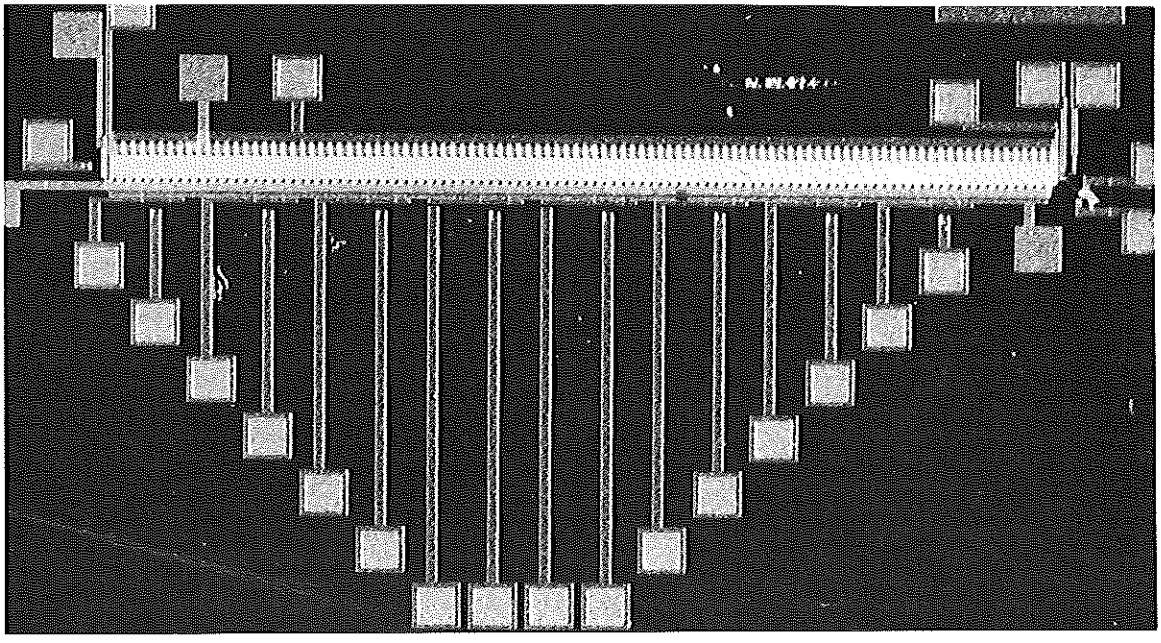

Fig. 3 Surface Channel CCD: 100 cell input-tapped shift register [5].

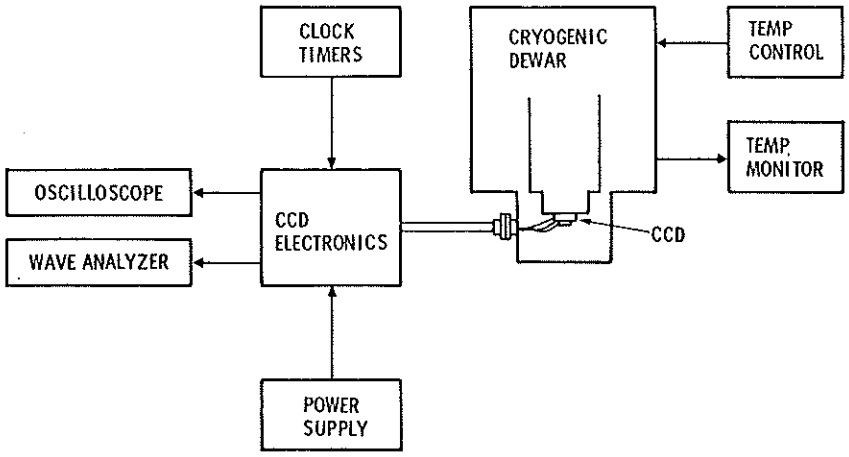

Fig. 4 Low Temperature Experimental Set-up: Block Diagram

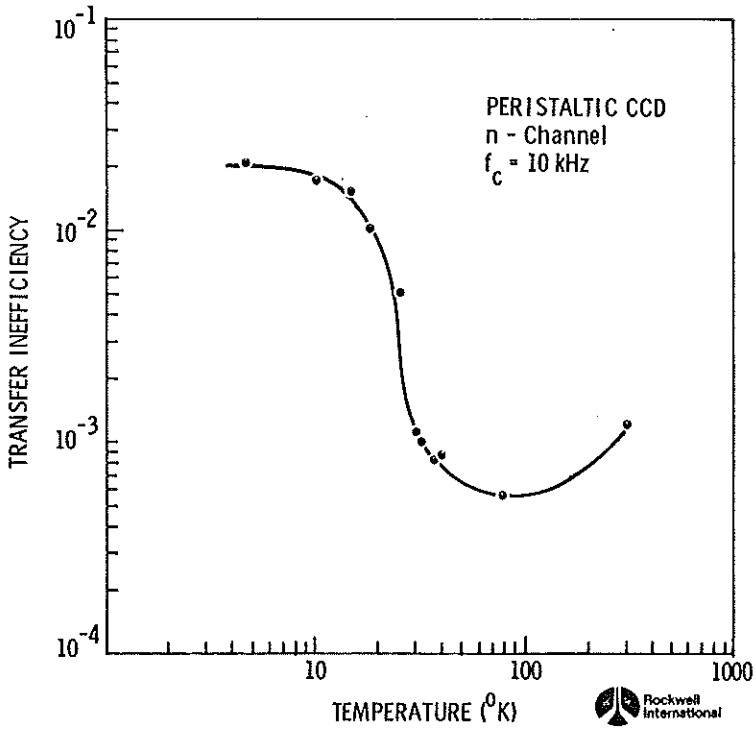

Fig. 5 PCCD transfer inefficiency vs. temperature

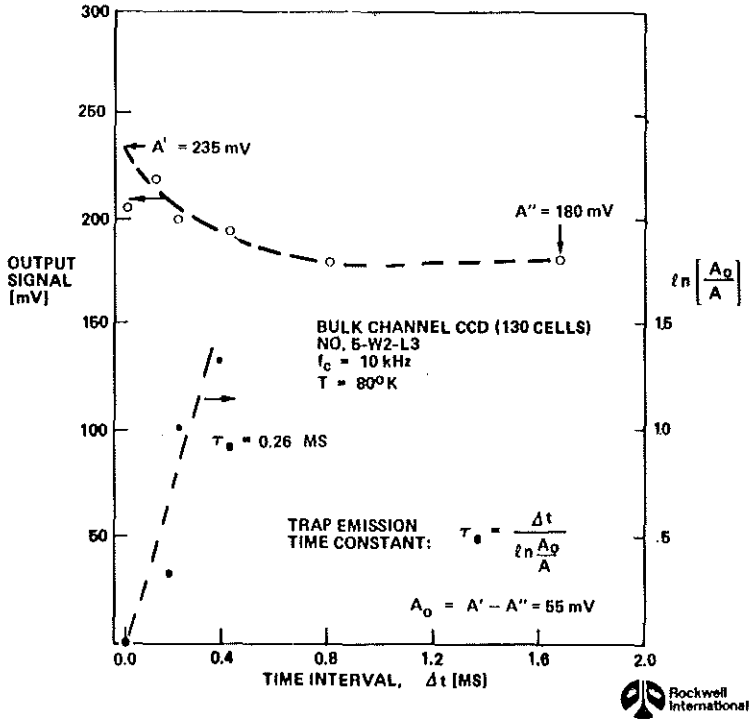

Fig. 6 PCCD trap emission time constants at 80°K

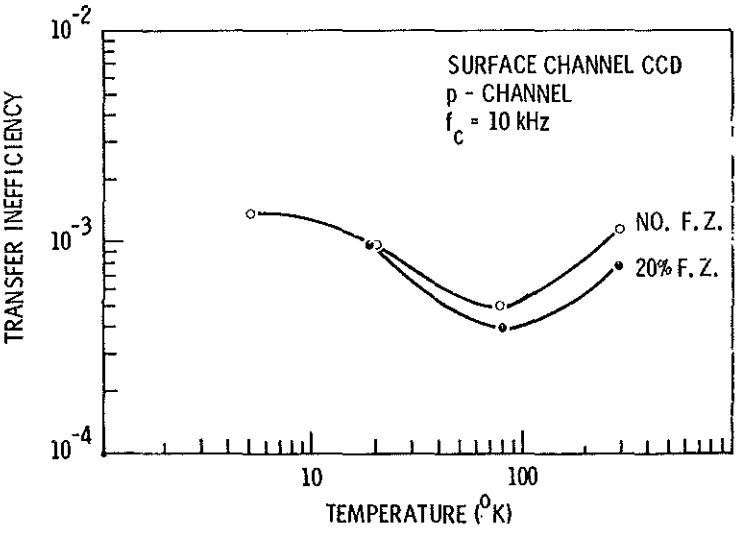

Fig. 7 SCCD transfer inefficiency vs. temperature