LIMITATIONS OF A THRESHOLD-INSENSITIVE CCD INPUT TECHNIQUE IN A TOTAL DOSE RADIATION ENVIRONMENT

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ABSTRACT. The sensitivity of the potential equilibration input method to flat-band voltage shifts has been investigated. The conditions required for proper operation of the technique have been used to predict the magnitude of the flat-band voltage shift that can be accommodated. The effect of gamma irradiation on the device transfer characteristics was determined. The experimental threshold shift tolerance is compared to the predicted behavior. The trade-offs involved in maximizing the threshold shift accommodation are discussed.

INTRODUCTION

Characteristics such as low cost, small size, low power, and high reliability make charge-coupled devices (CCD's) especially attractive for certain space and military applications if the devices can be made sufficiently tolerant of radiation environments. Experiments performed on several types of buried channel devices have shown that the charge transfer process itself is fairly insensitive to irradiation produced interface state trapping and flat-band voltage shifts in devices having the "proper" structure.[1] Buried channel devices have been operated with acceptable transfer efficiencies after exposure to gamma doses greater than 10^6 rads.[2] One of the major obstacles to the use of CCD's in irradiated systems is the sensitivity of the electrical input to flat-band voltage shifts. Even if "hard oxide" techniques can be employed in the fabrication of CCD's, a flat-band voltage shift of about 1v will have to be accommodated at 10^6 rads for the most favorable bias condition.[3]

POTENTIAL EQUILIBRATION INPUT TECHNIQUE

The "potential equilibration input technique", also known as "spill and fill" or "charge extraction", was developed as a low noise CCD input.[4,5,6] This method has the property of being independent of the flat-band voltage if the flat-band voltages of the input gate and the first transfer gate are equal.

The manner in which the potential equilibration input technique was operated on the test devices is shown in Fig. 1. The input diode (ID) is pulsed to a low value, V_{IDL}, when the voltage on the first two transfer gates P1 and P2 is high, injecting charge into the well under P1 and P2. While both transfer gates are still high, the diode voltage is returned to its high level, V_{IDH}, pulling the excess charge from under these electrodes. The amount of charge retained under the first two electrodes is proportional to the difference in the channel potentials under these electrodes and the input gate (IG). It was necessary to use the first two transfer gates since the first P1 gate is much narrower than the remaining transfer gates on this particular device. Hence, very little charge could be held under it. See Fig. 2. A typical transfer curve for the 150 bit buried channel test device is shown in Fig. 3. The threshold insensitive region of operation is indicated.

PREDICTED FLAT-BAND SHIFT EFFECTS

As a first order approximation the amount of signal charge injected into the CCD will

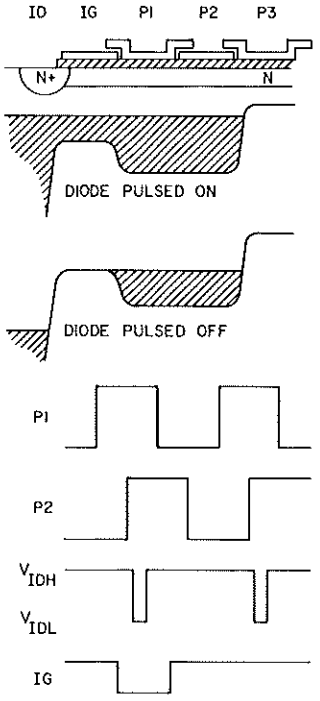

Fig. 1 Schematic cross-section of the buried channel shift register with the buried channel potential profile and the waveforms employed in the potential equilibration method.

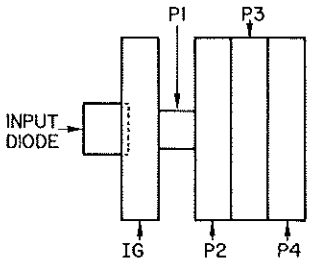

Fig. 2 Schematic top view of the shift register input structure.

be insensitive to flat-band voltage shifts of equal magnitude under the input and first transfer gates, provided that the conditions for proper operation of the potential equilibration input technique remain satisfied.[7] Expressed in the notation of Fig. 1 these

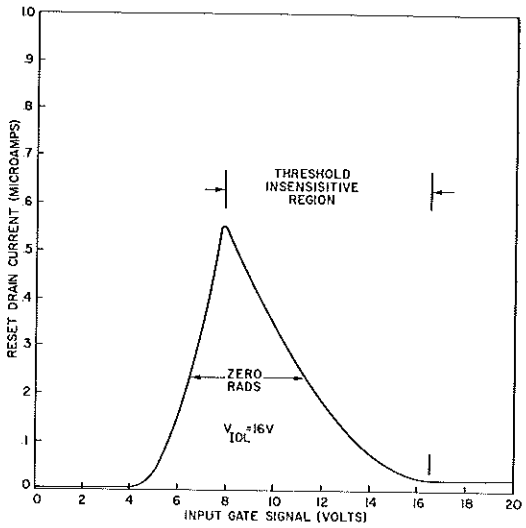

Fig. 3 Transfer curve for the potential equilibration input technique.

conditions for a buried channel device are

$$\phi_{IGL} > V_{IDL}, \quad \phi_{P1H} > \phi_{IGH},$$
$$V_{IDL} > \phi_{P1L}, \quad V_{IDH} > \phi_{IGH}. \tag{1}$$

where ϕ_{nL} and ϕ_{nH} are the maximum potentials in the buried channel when the voltages on the n'th gate are respectively low and high.

These inequalities may not be satisfied after irradiation since the channel potentials, ϕ, are a function of the flat-band voltage while the diode voltages, V, obviously are not. These inequalities can be used to predict the maximum flat-band voltage shift which the potential equilibration input can tolerate for a fixed set of pre-irradiation clock and bias voltages. In the case of the n-channel buried channel test device, only the last two inequalities can be upset by the irradiation produced flat-band voltage shift. The one dimensional solution to Poisson's equation for a buried channel device with a constant channel doping density was used to determine the channel potential maximum.[8] The pre-irradiation value of the terms in these inequalities, listed in (2a) and (2b), were calculated using the operating clock and bias voltages.

$$V_{IDL} = 16v > \phi_{P1L} = 11.6v \qquad (2a)$$

$$V_{IDH} = 40v > \phi_{IGH} = 24.3v \qquad (2b)$$

From (2a) it is seen that when the channel potential under P1 changes by +4.4v, the inequality will no longer be satisfied. A change in channel potential of 4.4v for this device would result from a flat-band voltage shift of -4.7v. In order to increase the magnitude of the flat-band voltage shift for which the inequality will remain satisfied one can either increase V_{IDL} or decrease ϕ_{P1L}. However, the maximum signal charge, Q_{max}, that can be injected is reduced for both options, since

$$Q_{max} \propto \phi_{P1H} - V_{IDL} \qquad (3)$$

and $\phi_{P1H} - \phi_{P1L}$ is fixed for a given clock swing. Of course, increasing the clock swing allows a greater flat-band voltage shift to be accommodated for a given maximum signal capability.

Up to this point it has been assumed that the flat-band voltage shifts under the input and first transfer gates are identical. This assumption is reasonable if the oxide structure and the electric field in the oxide beneath both the input gate and first transfer gate are identical. The voltage drop over the oxide, V_{ox}, in an empty buried channel device is given by[9]

$$V_{ox} = \frac{-qN_D d}{\epsilon_{ox}} \left[t - \phi_c^{\frac{1}{2}} \left(\frac{2N_A \epsilon_s}{qN_D^2} \right)^{\frac{1}{2}} \right] \qquad (4)$$

where $q = 1.6 \times 10^{-19}$C, N_D is the channel doping density, d is the oxide thickness, ϵ_{ox} is the dielectric constant of the oxide, t is thickness of the buried channel, N_A is the substrate doping density, ϵ_s is the dielectric constant of the silicon and ϕ_c is the channel potential at the p-n junction. ϕ_c is related to the maximum channel potential by

$$\phi_{max} = \phi_c \left(1 + \frac{N_A}{N_D}\right) \qquad (5)$$

The greatest difference in the potentials under the input and first transfer gates occurs when the first transfer gate returns to its low value (in this case 1v), while the input gate is biased for zero signal (in this case approximately 16v). The voltage drops across the oxide for this worst case are -5.3v for the +16v gate and -5.8v for the +1v gate. Since the gate is biased negatively with respect to the channel and the difference in the fields under the input and first transfer gates is small, the flat-band voltage shifts for these adjacent gates should be approximately the same. However, even small differences in the flat-band voltage shifts will result in an approximately parallel shift of the post irradiation curve in the operating region.

EXPERIMENTAL DETAILS

The test device was a 150 bit, four phase, n-buried channel shift register with an aluminum-anodized aluminum-aluminum double-level metallization.[10] The gate oxide was 1000 Å and the channel depth was either 1000 Å or 6000 Å. The implanted dose was 1.5×10^{12}cm^{-2} phosphorus. The resistivity of the <100> orientation substrates was 10 to 70 ohm cm. The transfer gates were 30.5 micrometers long and 127 micrometers wide.

The shift registers were operated using the double clocking scheme at 500 kHz.[11] The clock swing was from 1 to 16V with a 50% duty cycle. The buried channel was kept depleted by applying 26.4v to the reset drain. The reset pulse swing was from 0 to 8v. The on-chip output amplifier was operated as a source follower with a drain voltage of 41v. The 10 kilohm source follower resistor was connected to + 11v. The substrate was held at 0v. The output gate voltage was + 4v.

The potential equilibration input was characterized by means of a transfer curve. An electrometer was inserted in the reset drain line and its output was fed into the Y axis of an XY recorder. The input gate voltage was applied to the X axis. The reset drain current was measured to avoid the effects of the radiation on the output amplifier. All transfer curves were taken with V_{IDH} = 40v and V_{IDL} = 16v.

Four devices were irradiated in the NRL Cobalt 60 gamma ray source while being operated as shift registers with normal clock and bias voltages. The input gate was held at + 15v during the irradiation except when a burst of eight full well signals were inserted every 256 clock

periods as a check for proper operation of the device. Transfer curves were taken after each dose increment. The displacement effects due to increased output diode leakage and dark current were subtracted out. The highese dose rate employed was 4.4×10^3 rads (Si) per minute.

EXPERIMENTAL RESULTS AND DISCUSSION

A series of potential equilibration input transfer curves were taken prior to irradiation in which a flat-band voltage shift was simulated by applying positive offset voltages to all the CCD gates. In the operating region the transfer curves were insensitive to offset voltages of up to +4v.

The transfer curves for the potential equilibration input as a function of total dose are shown in Fig. 4.

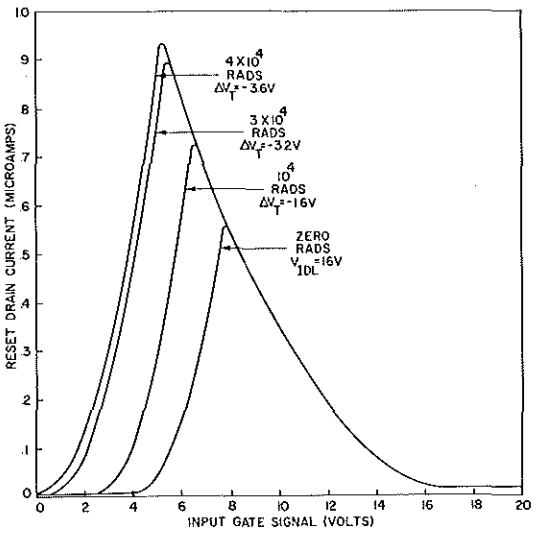

Fig. 4 Potential equilibration input transfer curves as a function of total dose.

The signal charge injected for a given gate voltage was insensitive to threshold voltage shifts up to -3.6v (4×10^4 rads Si). The increase in the maximum charge handling capability of the input as a function of dose can be explained by referring to equation (3). The flat band voltage shift increases the channel potential ϕ_{P1H} and decreases the gate voltage for which $\phi_{IGL} = V_{IDL}$. The threshold voltage shifts were obtained from the dynamic current injection input transfer curves shown in Fig. 5.

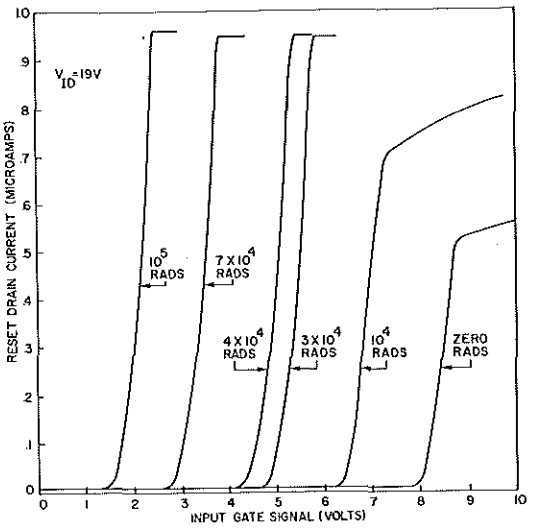

Fig. 5 Dynamic current injection input transfer curves as a function of total dose.

Threshold shifts of less than one volt caused the dynamic current injection transfer curve to be shifted completely out of the pre-irradiation operating range while the potential equilibration input characteristics remained unchanged even after a -3.6v threshold shift. Experimentally it has been observed that the threshold voltage shifts measured by the dynamic injection input are approximately equal to the flat-band voltage shifts measured by the 1MHz CV technique, for a buried channel device.[12] At 7×10^4 rads, the threshold voltage shift was -5.1v, making ϕ_{P1L} equal to 16.6v. As expected, the transfer curve for V_{IDL} = 16v shown in Fig. 6 no longer falls on the pre-irradiation curve for high gate voltages. The predicted threshold shift tolerance (-4.7v), falls within the range of the observed values (-3.6v to -5.1v). If the inequality $V_{IDL} > \phi_{P1L}$ is restored by increasing V_{IDL} to +17v, the post irradiation curve is brought more nearly into coincidence with the zero rad curve. See Fig. 7. The effect of not satisfying the condition $V_{IDL} < \phi_{P1L}$ is further illustrated in Fig. 8.

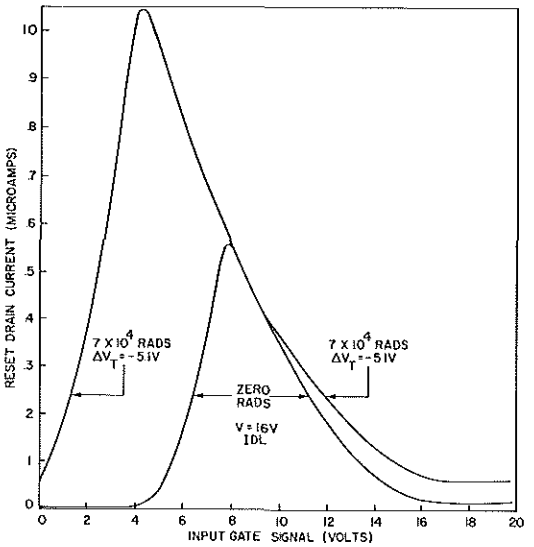

Fig. 6 Comparison of the potential equilibration input transfer curves at zero rads to the curve at $7x10^4$ rads.

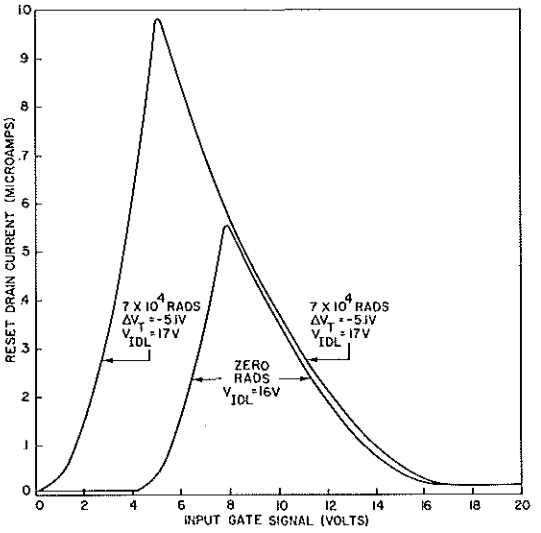

Fig. 7 Comparison of transfer curve at zero rads with V_{IDL} = 16v to the curve at $7x10^4$ rads with V_{IDL} = 17v.

At 10^5 rads Si(ΔV_T = -6.5v), ϕ_{P1L} has a value of 17.4v and the input characteristics are severely distorted for V_{IDL} = 16v.

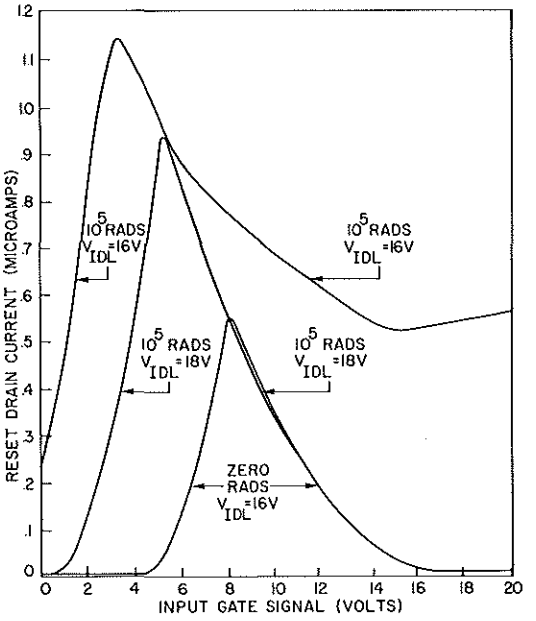

Fig. 8 Comparison of transfer curves at 10^5 rads (Si) as a function of V_{IDL} to the zero rad curve.

Increasing the input diode low voltage to +18v restores the transfer curve to its pre-irradiation value in the operating region. The tradeoff involved in using a larger input diode low voltage to increase the threshold voltage is a reduced signal handling capability. At zero rads the maximum signal for V_{IDL} = 18v was 65% of the $7x10^6$ electron capacity for V_{IDL} = 16v.

CONCLUSIONS

The potential equilibration input has been shown to be insensitive to irradiation produced input threshold voltage shifts of equal magnitude under the input and first transfer gates provided that the conditions for the proper operation of the input remain satisfied. If CCD's can be fabricated with hardened oxides, this input method would be insensitive to the flat-band voltage shift produced by a megarad dose.

BIBLIOGRAPHY

1. J. M. Killiany, W. D. Baker, N. S. Saks, and D. F. Barbe, "Effects of Ionizing Radiation on Charge-Coupled Device Structures," IEEE Trans. Nuc. Sci., NS-21, No. 6, 193 (1974).

2. G. A. Hartsell, D. A. Robinson, and D. R. Collins, "Effects of Ionizing Radiation on CCD's", Proceedings of the Symposium on CCD Technology for Scientific Imaging Applications, Pasadena, California, p. 216, June (1975).

3. K. G. Aubuchon, E. Harari, D. H. Leong, and C. P. Chang, "Effects of HCl Gettering, Cr Doping and AL^{+} Implantation on Hardened SiO_2," IEEE Trans. Nuc. Sci., NS-21, No. 6, 167 (1974).

4. M. F. Tompsett, and E. J. Zimay, "The use of Charge-Coupled Devices for Delaying Analog Signals", IEEE J. Solid-State Circuits, SC-8, 151 (1973).

5. S. P. Emmons and D. D. Buss, "Techniques for Introducing a Low-Noise Fat Zero in CCD's", Device Research Conference, 26-28 June, 1973, Boulder, Colorado.

6. J. E. Carnes, W. F. Kosonocky, and P. A. Levine, "Measurement of Noise in Charge-Coupled Devices", RCA Rev. 34, 553 (1973).

7. C. H. Sequin and A. M. Mohsen, "Linearity of Electrical Charge Injection into Charge Coupled Devices", IEEE J. Solid-State Circuits, SC-10, 81 (1975).

8. C. K. Kim, J. M. Early, and G. F. Amelio, "Buried Channel Charge Coupled Devices" NEREM Boston, Record of Tech. Papers Part I, 161 (1972).

9. D. F. Barbe, "Imaging Devices Using the Charge Coupled Concept," Proc. IEEE 63, 38 (1975).

10. D. R. Collins, S. R. Shortes, W. R. McMahon, R. C. Braken, and T. C. Penn, "Charge Coupled Devices Fabricated Using Aluminum-Anodized Aluminum-Aluminum Double-Level Metallization", J. Electrochem Soc. 120, 521 (1973).

11. D. R. Collins, W. C. Rhines, J. B. Barton, S. R. Shortes, R. W. Brodersen, and A. F. Tasch, Jr., "Electrical Characteristics of a 500-Bit Al-Al_2 O_3-Al CCD Shift Registers", Proc. IEEE 62, 282 (1974).

12. J. M. Killiany, N. S. Saks, and W. D. Baker, "Effects of Ionizing Radiation on a 256-Stage Linear CCD Imager" to be published in IEEE Trans. Nuc. Sci., NS-22, No. 6, (1975).