

Noise Linearity and Trapped Charge Measurements  
with Charge Sensitive Amplifiers

K. Kandiah

U.K. Atomic Energy Authority, Atomic Energy Research  
Establishment, Harwell, Didcot, Oxon, U.K.

ABSTRACT. A measurement technique is described for precise determinations of the magnitudes of the charges flowing in a CCD and their statistical distribution as a function of clock number and related to changes induced on specific clocks. The method involves the use of charge sensitive amplifiers, sample and hold circuits and pulse amplitude analysers commonly used in nuclear measurements. The advantages of off-chip amplification for quantitative determinations and comparisons between devices are demonstrated. Measurements on a few CCDs showing some of the merits of the technique are included. Direct measurements of the charge injected electrically at the input and the noise associated with this are also possible.

1. INTRODUCTION

Determination of the magnitudes and the times of collection of pulses of charge generated in radiation detectors by incident quanta is a common and long established experimental procedure in nuclear measurements. A precision of one part in  $10^3$  in pulse amplitude and a small fraction of  $1\mu\text{s}$  in time is routinely achieved and the stability of the amplitude measurements is generally required to be better than one part in  $10^4$ . The pulses of charge usually contain between  $10^3$  and  $10^7$  carriers and occur randomly in time. The detector is electrically equivalent to a capacitor, and signal amplification and noise in such systems has been extensively studied<sup>(1,2)</sup>. Sophisticated equipment for measuring pulse amplitudes<sup>(3)</sup> and advanced signal processing methods<sup>(4,5)</sup> have also been developed for these applications.

Our interest in charge coupled devices is centred round their application in signal processing and we are using nuclear measurement techniques to study the performance of these new devices. The linearity and noise of CCDs is of the utmost importance in view of the above stringent requirements. Inefficient charge transfer in a CCD introduces a complex time varying characteristic which may make these devices

unsuitable for many nuclear instrumentation applications. It is the purpose of this paper to describe measurement techniques which we believe will lead to a better understanding of the phenomena which limit their performance. The results of measurements on a few CCDs will also be given.

2. THE METHOD

Frequency domain analysis and measurements are unlikely to give a clear indication of the physical processes in a CCD which essentially operates in the time-domain. One of the main features of a CCD is that the clock need not be regular and signal processing applications where the clocks are not repetitive can only be analysed by time-domain methods. If there is adequate knowledge of the devices in the time-domain it is relatively easy to predict their behaviour in the simpler case when the clock is regular and at a fixed frequency.

The present study is therefore aimed at measurements of charge flow using clock pulses occurring in bursts with the period  $T_0$ , total number  $N_0$  in the burst and the repetition rate of the bursts independently variable. Charge is inserted into the input electrically

either as a single charge packet on a specific clock, once in each burst, or combined with a constant level of charge packets of independantly variable magnitude extending over a number of clocks. The average value of the output charge on any specified clock or the integral over a number of adjacent clocks is measured with a digital voltmeter and the statistical distribution of amplitudes of the individual packets over a large number of bursts is measured with a pulse amplitude analyser<sup>(3)</sup>. This latter measurement will give r.m.s. fluctuations of the charges. These measurements are repeated over a range of clock numbers and at different clock frequencies.

The system has been designed to measure the absolute magnitudes of the charges to about 5%. The stability of these measurements is better than 0.2% and the relative measurements of charge are also to this accuracy or to 1 fC whichever is the larger. Such precision is expected to yield useful information on the charge states and transfer properties of the CCD. In order to maintain moderately high accuracy the amplitudes of all drive waveforms including those to the input diode and gate are maintained to an accuracy of about 50 mV. The short term fluctuations and the noise on these waveforms is estimated to be less than 1 mV. The measurements with the present system are not reliable at clock frequencies in excess of 1 MHz owing to the precautions taken to maintain accuracy but faster circuit techniques may make it possible to extend the measurements to 5 MHz.

### 3. EXPERIMENTAL APPARATUS

A block diagram of the major parts of the equipment is given in fig 1. A brief description of the features of each part will now be given.

#### 3.1 CCD AND DRIVE

All the CCD's used in our measurements were three phase n-channel devices with an input diode, one input gate, output diode and one output gate. The output gate and output diode were held at fixed potentials of +3 V and +7 V respectively for most of the measurements. Electrical charge input was achieved by pulsing the input diode and input gate within the duration of the  $\phi_1$

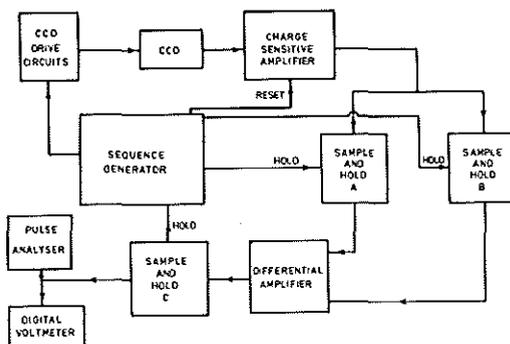


Fig 1

#### Block diagram of equipment

drive waveform as shown in fig 2. This is a surface potential equilibration method as described by Tomsett<sup>(6)</sup> with the difference that the durations of the charge setting time  $T_s$  and equilibration time  $T_E$  are fixed and independant of the clock rate. As shown in fig 2 the input diodes were normally held at  $E_C + 2$  volts, where  $E_C$  is the phase-clock amplitude and pulsed to a low voltage for charge injection.  $E_C$  was +10 V for all the measurements reported here. The total number of input diode pulses is limited to about 20 from the first phase clock.

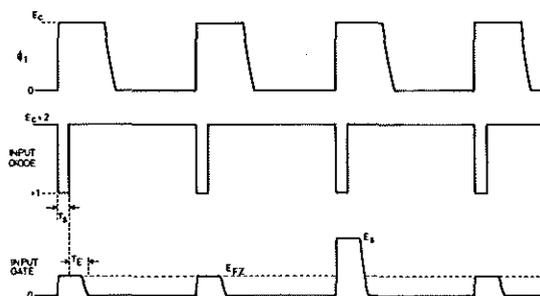


Fig 2

#### CCD drive waveforms for electrical charge input

The input gate is normally held at 0 volts and pulsed to  $E_{FZ}$  or  $E_S$  where  $E_{FZ}$  is the fat zero control level and  $E_S$  is the signal control level. The signal pulse  $E_S$  is applied only on one nominated clock  $N_S$  clocks after the beginning of the phase clocks and  $N_S$  is variable from 0 to 9. The fat zero level of pulses on the input gate were maintained on all clocks except the signal clock for the entire duration of the burst of phase-clocks. However since the total number of the input diode pulses was restricted to about 20 clocks the injection of fat zero signals terminated at that point. This enabled us to study the build-up and decay of fat-zero pulses at the output. The phase-clocks had an overlap of 50 ns and a linear fall time of 150 ns except in the experiment on linearity described later.

### 3.2 THE CHARGE SENSITIVE AMPLIFIER

The measurements reported here depend critically on the performance of this amplifier. There are two parts as shown in the simplified schematic in fig 3. The charge signals are amplified in the low noise amplifier<sup>(2)</sup> which has a JFET input stage and a feedback capacitance  $C_f$  which defines the charge sensitivity. With adequate forward gain A the output voltage is equal to  $Q/C_f$ , where Q is the charge signal at the input.

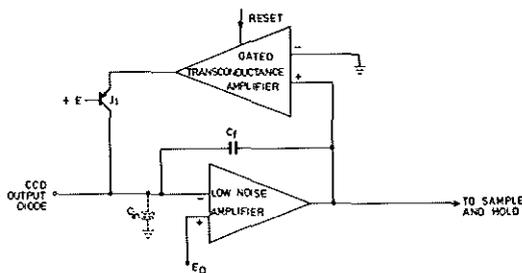


Fig 3

#### Schematic of charge sensitive amplifier and reset system

The gated transconductance amplifier is normally off so that transistor  $J_1$  passes only the small leakage current of

less than 100 pA. When a reset signal is applied this current increases and the output voltage of the low noise amplifier is quickly restored to near 0 volts which is the reference input to the transconductance amplifier. In this reset condition the voltage at the output diode of the CCD will be close to  $E_D$  which is the reference voltage into the low noise amplifier. Reset is not applied during any of the clocks inside the sampling period or during the preceding or following clock i.e. during the period from  $N - 1$  to  $N + n + 1$ .

Because of the large amount of negative feedback over the charge sensitive amplifier its input impedance is low and equivalent to a capacitance of value  $AC_f$ . The feedback capacitance is 0.8 pF so that an output voltage of 1 mV corresponds to an input charge of  $5 \times 10^3$  electrons. Since this is virtually independent of the CCD output capacitance (at the output diode or on a floating gate) the calibration of the system is maintained for any CCD connected to the input. Another important consequence of this arrangement is that any contribution to the non-linearity due to the finite output conductance<sup>(7)</sup> of the CCD, particularly when using floating gate sensing, can be entirely eliminated.

The leakage current of the input JFET is a few pA so that most effects of this can be ignored. The equivalent noise of the amplifier is about 0.11 r.m.s. electrons- $\text{Hz}^{-2}$  referred to its input. Typically therefore the noise contribution of the amplifier will be 78 r.m.s. electrons for a clock frequency of 1 MHz when the output signals are put through a 0.5 MHz low-pass filter. In our measurements however the actual noise due to the amplifier is about 430 r.m.s. electrons owing to the greater bandwidth and the double sampling method as explained in the discussion on the results. With a good on-chip amplifier it may be possible to reduce the amplifier noise to 0.025 r.m.s. electrons- $\text{Hz}^{-2}$  if the noise voltage of the source follower is of the order of  $10\text{nv-}\text{Hz}^{-2}$  and the total sensing capacitance including the gate capacitance of the source follower is 0.4 pF. Our measurements on some polysilicon gate FETs gave an equivalent noise of about 0.1 r.m.s. electrons- $\text{Hz}^{-2}$  which is not very different from the off-chip

amplifier used in these experiments. Furthermore the introduction of a feedback capacitance into the on-chip amplifier is not very convenient. Even if this were possible the value of this feedback capacitance is required to be about 0.2 pF in order to maintain a sufficiently low input impedance at the gate of the on-chip amplifier and this will result in a further degradation of the noise performance.

#### 3.4 SAMPLE AND HOLD CIRCUITS

The output of the charge sensitive amplifier is processed in two stages. The sample and hold A is made to hold the level existing at clock N and sample and hold B holds at clock N + n so that the output of the differential amplifier, after the clock N + n, is proportional to the charge collected in the n clocks starting from N. In our three phase system the "hold" instruction to both the circuits, for most measurements excluding the reverse connected tests on charge injection, is given on the  $\beta_2$  phase when there is no charge output from the CCD. The sample and hold circuit C is made to sample the output of the differential amplifier some time after clock N + n so that the voltmeter and analyser do not see the transients between clocks N and N + n. The accuracy and stability of the sample and hold and difference circuits is better than about 0.5 mV referred to the output of the charge sensitive amplifier i.e. about 2500 electrons. The noise level is negligible in relation to the charge sensitive amplifier.

#### 3.5 DIGITAL VOLTMETER, ANALYSER AND RECORDER

The digital voltmeter is used to measure the mean amplitude of the charge signal in the designated range N to N + n as determined by the sample and hold circuits and the pulse analyser records the amplitude distributions of this signal over a large number of bursts - at least  $10^5$ . From this distribution the r.m.s. noise in units of electrons referred to the CCD output is readily calculated.

The linearity of the CCD is also measured automatically by using a sweep voltage generator which sweeps the voltage  $E_s$  (or  $E_{F2}$ ) applied to the input gate

(see fig 2) linearly. At a fixed repetition frequency the number of counts recorded in each channel of the analyser is then inversely proportional to the slope of the transfer function of the CCD at that signal level. The actual transfer function can also be recorded automatically by using a chart recorder in place of the digital voltmeter.

### 4. RESULTS AND DISCUSSION

Three types of surface channel CCD's were tested. The first, MA302, is a 100 element aluminium gate device with gate length of 8 $\mu$ m, width 100 $\mu$ m and a gap between gates of 2 $\mu$ m. The second, MA315, is a 10 element single level doped-undoped polysilicon gate device with gates of 10 $\mu$ m x 75 $\mu$ m and inter-gate region of 4 $\mu$ m. The third, MA318, is a 100 element device, similar to the MA315, with a gate width of 60 $\mu$ m and with an on-chip amplifier.

#### 4.1 NOISE ON SINGLE INPUT PACKET

The total capacitance, including the CCD, at the input of the charge sensitive amplifier was nearly 20 pF and the equivalent noise voltage of the FET was measured to be 0.9 nV-Hz<sup>-1/2</sup>. This should give an equivalent input noise of 0.11 r.m.s. electrons-Hz<sup>-1/2</sup>. In order to ensure that the waveform was reasonably flat between the 500 kHz clock transients we used a bandwidth of 4 MHz in the charge sensitive amplifier. The noise of the amplifier will then be equivalent to 220 r.m.s. electrons and taking two random samples should give an equivalent noise of 308 r.m.s. electrons at the output of the differential amplifier. The measured noise was about 430 r.m.s. electrons with the CCD taken out and an equivalent capacitance shunting the input of the amplifier. We cannot find a good explanation for this discrepancy except perhaps the effect of the finite rise time of the hold waveform in the sample and hold circuits. We are however confident that the measurements of CCD noise are accurate since these noise components do not change in the  $\beta_2$  clock phase when the sampling occurs.

Measurements of charge output and noise on the MA302 with only one charge packet at maximum level injected into

the input on clock 9 at 500 kHz clock rate are shown in fig 4. The output signals on clocks 109 and beyond was measured with  $n = 1$  so that the magnitudes of individual charge packets are shown here. The back-

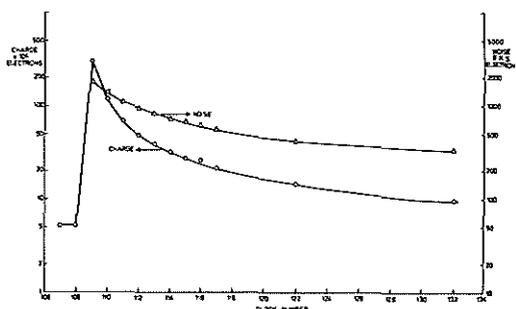


Fig 4

Charge output and noise of MA302 as a function of clock number with single input,  $N_s = 9$ , without fat zero

ground noise as measured on clock 90 was subtracted in quadrature and the noise is therefore that due to the presence of a signal. The fact that the small residual charge and noise 20 clocks or more after the main packet can be reproducibly measured gave us some confidence in the procedures adopted. There was a considerable variation in the magnitude of the charge output when the ambient temperature changed, presumably due to the change in losses due to trapping, and the noise measurements had to be made with automatic stabilisation of the mean signal amplitude in the pulse analyser. The noise measurements were then consistent over many repeated measurements.

The leakage current of the MA302 at the output was typically 5 nA without signal and the measured noise in the absence of signal was 420 r.m.s. electrons which is considerably greater than the noise expected from 5 nA confirming the excess noise reported earlier by Mohsen et al<sup>(8)</sup>. The leakage current fell to about 1 nA when  $\phi_1$  and  $\phi_2$  were kept permanently at 0 volts. One interesting feature was that the leakage current increased to more than 40 nA when  $\phi_2$  was kept at 0 volts. This behaviour is attributed to the buried n+ connection to the  $\phi_2$  gates causing current injection into

the output diode. Another observation was a partial decay of the transient waveform induced by the clock steps into the output diode with a time constant of the order of 5 $\mu$ s. If the coupling is purely due to capacitance the step functions of the clocks should be reproduced exactly at the output. Thorough investigation confirmed that this was not due to instrumental factors. From the above observations it is suggested that the high noise level of the MA302 in the absence of signal could be due to the pumping of charge into and out of the output diode by the various clock waveforms. The resultant current can have a small mean value but cause a high noise level owing to the components being emission or diffusion limited. It is therefore necessary to take great precautions on the details of the layout of all the diffused regions in the silicon as well as the gates and interconnections on top of the thin and thick oxides.

4.2 CLOCK NOISE

Considerable amounts of clock noise have been reported by Mohsen et al<sup>(8)</sup> and Carnes et al<sup>(9)</sup>. Careful measurements of the noise of the MA318 with no signal present are given in table I. Since the normal output from this device was only available through an on-chip amplifier we operated the device reverse connected so that the originally intended input diode,

Table I

Noise of MA318 with no signal

	Total noise r.m.s. electrons
Charge sensitive amplifier without CCD	430
Charge sensitive amplifier and CCD without drives	425
Charge sensitive amplifier and CCD with drives	444

which has a direct connection, was connected to the charge sensitive amplifier as if it was the output diode. Since these measurements are concerned with the noise level in the absence of a signal the details of the

connections to the new input diode and gate are irrelevant so long as they were kept at potentials which prevented charge injection.

The noise measurement without the CCD was taken with a capacitance equal to the measured capacitance\* of the CCD shunting the input of the charge sensitive amplifier. These measurements are reproducible to better than  $\pm 3$  r.m.s. electrons on the totals given above. The noise contribution of the CCD is estimated to be 130 r.m.s. electrons with the clocks present and no more than 50 r.m.s. electrons in the absence of the clocks. The mean leakage current with the clock present was about  $1.1 \times 10^4$  electrons in each  $2\mu\text{s}$  clock period and this could account for about 105 r.m.s. electrons of noise so that the increase of noise due to the clocks not explained by leakage is less than 80 r.m.s. electrons. It is not easy to determine how much of this may still be due to reversible charge pumping which has a small mean current at the output.

#### 4.3 ELECTRICAL INJECTION NOISE

One of the significant causes of noise in a CCD used for signal processing has been ascribed to the electrical charge injection process at the input<sup>(8)</sup>. In normal operation it is not easy to separate this component from those due to charge trapping and free charge transfer inefficiency. The methods which use extrapolations of the noise from light signals injected at varying positions from the end of a long CCD and the net noise from electrical charge injection are not very accurate because they rely on the difference between large numbers. We have devised a method which should give a more direct and accurate figure for the electrical charge injection noise.

Let us consider the details of operation of the output gate and diode. In our case the bias for the output gate and output diode are +3v and +7v respectively

---

\*Capacitance and leakage measurements of the CCD give variable results and these will be reported elsewhere.

in order to perform the normal function of receiving the charge transmitted by the last  $\phi_3$  electrode. In this condition the output charge of the CCD is amplified by the charge sensitive amplifier connected to the output diode. If however the potential of the output gate is at least 1v higher than that of output diode, allowing for threshold potentials, charge will flow out of the output diode to fill the well under the last  $\phi_3$  gate on each  $\phi_3$  clock and be transferred back into the output diode at the end of the  $\phi_3$  clock. These charge flows will be amplified by the charge sensitive amplifier in the normal way. If the output of the charge sensitive amplifier is sampled on sample and hold A on clock  $\phi_2$  and on sample and hold B on clock  $\phi_3$  of the same clock N the difference will be the charge pumped out of the diode to fill the well under  $\phi_3$ . By suitable setting of the potentials at the output gate and diode it is possible to simulate the conditions at an input gate and diode during charge injection and equilibrium. The input diode can be connected to the charge sensitive amplifier and the magnitude of the charge injected into  $\phi_1$  can be obtained directly from these measurements. We studied the fluctuations in these charges and have arrived at the conclusion that the fluctuations are not much greater than the theoretical figure of  $400\sqrt{2Cg}$  where  $Cg$  is the capacitance in pF of each of the two electrodes in the potential equilibration system. Details of this will be reported elsewhere.

An example of high injection noise due to incorrect operation of the fat zero level of the MA302 is shown in fig 5. The level  $E_{FZ}$  (fig 2) was kept at about 0.5v above the threshold in order to obtain a fat zero level of about 50% of the maximum charge. The correct operating voltage to obtain this fat zero level would have been about 6v when normal surface potential equilibration would have taken place. With only 0.5v on  $E_{FZ}$  the filling of the well under  $\phi_1$  would be emission limited and exhibit a large noise level. In order to demonstrate this a signal level  $E_s$  of 2.5v, which gives 75% of maximum charge with equilibration, was also set on clock 9 ( $N_s = 9$ ). The resulting charge output and noise are seen in fig 5. It is seen that the noise on clock 109 was smaller than the

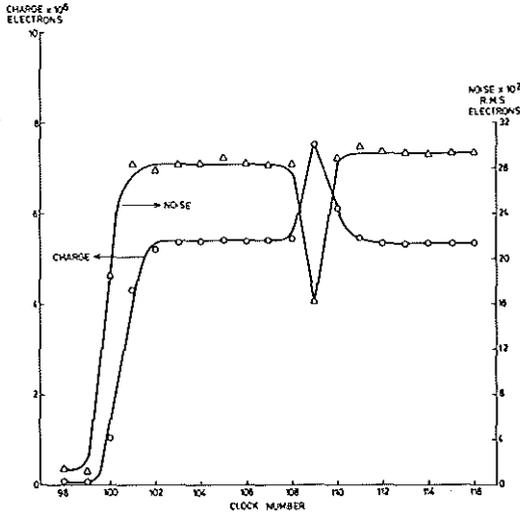


Fig 5

High injection noise in the MA302 when operated with incorrect voltage for obtaining fat zero and lower noise on a larger signal on clock 9 with correct potential equilibration

noise on the other clocks which exhibit the high noise due to incorrect operation of the fat zero.

#### 4.4 CHARGE TRAPPING AND FREE CHARGE TRANSFER EFFICIENCY

A simple example of the effects of charge trapping is seen in fig 6. In this case the fat zero control level  $E_{FZ}$  of the MA302 was set at 1.5v in order to obtain maximum charge with correct potential equilibration. The signal level  $E_s$  on clock 9 was set at 0v so that no charge injection took place on this clock. It is seen that the noise builds up on clock 100 to a larger value than the steady state figure before the fat zero charge amplitude built up to the steady state level. Again when the charge on clock 109 falls to a very low value, owing to the absent signal on clock 9 at the input, the noise on clock 109 shows a slight increase and increases

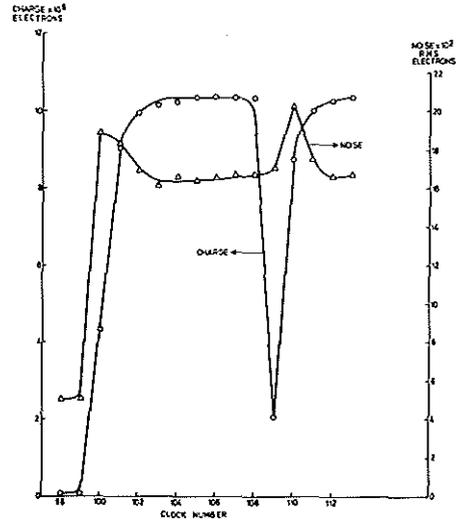


Fig 6

Noise build up in the MA302 on 100% fat zero and excess delayed noise on an absent signal

by a large amount on the trailing clock 110 before returning to the steady state value 2 clocks later. The exact nature of this behaviour will depend on the relationship between the clock period  $T_0$  and the trap emission time constants.

A detailed study of the build up and decay of a string of fat zero pulses will yield information on the relative contribution of losses due to trapping and free charge transfer. Such measurements are in progress and an indication of the accuracy obtainable even with devices with high transfer efficiency is given in fig 7. One interesting aspect is that the figure for transfer inefficiency changes appreciably if many trailing pulses are taken into account rather than only the first one. If the charge recovered on the first trailing pulse only is used the transfer inefficiency of this device is calculated to be  $4.9 \times 10^{-4}$  without fat zero and  $3.3 \times 10^{-4}$  with fat zero. If however the total charge

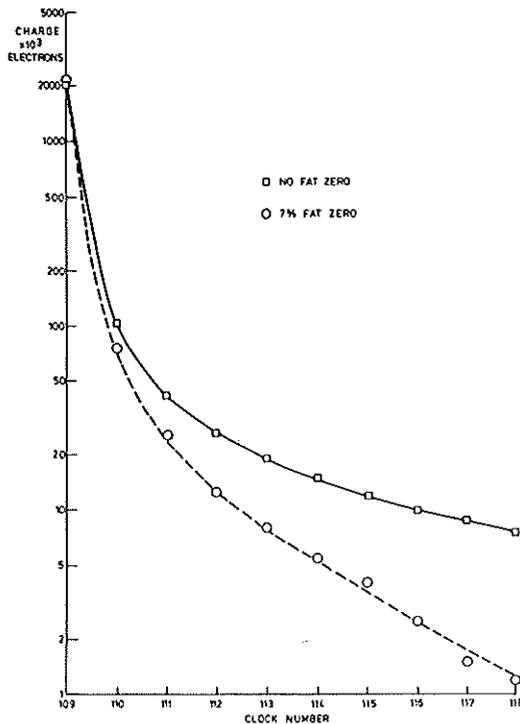


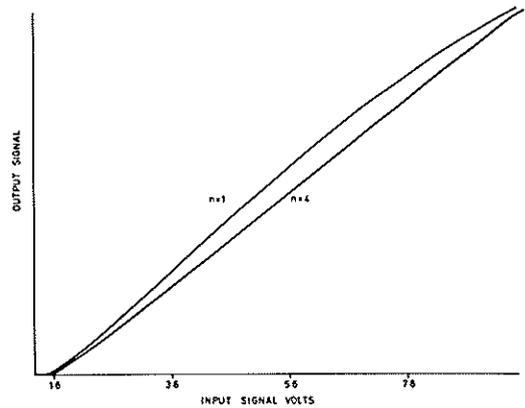
Fig 7

Charge output of MA318 as a function of clock number with and without fat zero.  
The fat zero level was deducted in these plots ( $N_s = 9, n = 1$ )

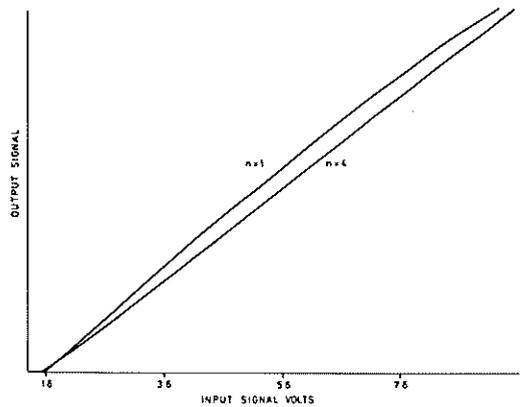
recovered in 10 trailing pulses is used in the calculation the figures are  $1.2 \times 10^{-3}$  without fat zero and  $5.3 \times 10^{-4}$  with fat zero.

#### 4.5 LINEARITY

It has been shown above that the study of charge packet size and the associated noise as a function of clock number following a change in the input can give useful information on device behaviour. The study of linearity of the transfer function can be equally useful if it is suitably oriented. The normal transfer function measurement consists of recording the actual magnitude of the output charge as a function of the input and two examples of such a record are given in fig 8. All these measurements were made at a clock frequency of 500 kHz. In figure 8(a) the



(a) clock trailing edges 70 ns



(b) clock trailing edges 170 ns

Fig 8

Transfer function of MA315  
measuring charge output in  
the first clock ( $n = 1$ )  
and on the total charge in  
the first four clocks ( $n = 4$ )

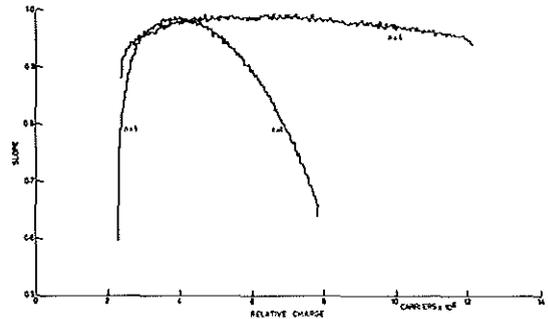
transfer function is plotted for the case where the trailing edge of the phase driving clocks had a linear fall time of 70 ns and the two curves correspond to the charge collected on the first pulse and the integral of the charge on the first four pulses. Fig 8(b) shows the measurements

with a clock fall time of 170ns. It is seen that there is some difference between these measurements but it is difficult to abstract quantitative information from these results. The output signal scales in fig 8 are only relative and have been adjusted in each case to make the maximum signal levels correspond to make comparisons easier.

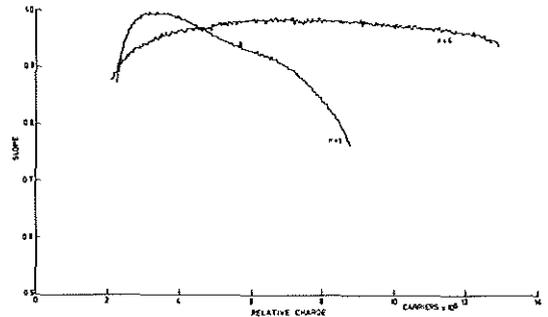
A much more reliable and accurate technique is one in which the differential coefficient of the transfer functions shown in fig 8 is plotted as a function of output charge. This is readily obtained automatically by sweeping the input voltage  $E_{FZ}$  or  $E_g$  (fig 2) linearly over some predetermined range, maintaining a constant pulse burst repetition frequency and plotting the number of counts recorded in each bit interval (channel) of the pulse analyser in fig 1. This is standard procedure for measuring linearity with pulse analysers and the results for the same cases as in fig 8 are shown in fig 9. The gross nonlinearity with  $n = 1$  for the faster trailing edge of the clock due to variation in free charge transfer efficiency is reduced by integrating the output charge over four clocks ( $n = 4$ ). However it is also noticed that the non-linearity when  $n = 4$  is slightly worse for the longer trailing edge and for the smaller charge packets owing to charge trapped in the interelectrode gaps during transfer. It is seen that the differential linearity for  $n = 4$  of this 10-element device with 10v clocks is better than 5% for a total charge output range of about  $10^7$  electrons (from  $2 \times 10^6$  to  $12 \times 10^6$ ). We have not attempted to interpret these in terms of harmonic distortion since the differential linearity gives a better and more direct indication of the expected performance of the device in our signal processing applications.

## 5. CONCLUSIONS

The measurement techniques reported here give accurate numerical figures which are a direct indication of the mechanisms governing CCD operation. Direct measurements of the charge injected and the noise associated with this process can be obtained so long as the connections to the appropriate electrodes are available. It has been shown that the noise performance of the off-chip amplifier is more than



(a) Trailing edges 70 ns



(b) Trailing edges 170 ns

Fig 9

### Differential linearity measurements for the conditions identical to those in fig 8

adequate for most measurements. The linearity, constancy of calibration and low input impedance of the charge sensitive amplifier make it possible to make direct quantitative comparisons between a range of devices.

From the measurements reported it is evident that the background noise both intrinsic and extrinsic are quite small even with off-chip amplification. The

techniques used for the control of drive waveforms have resulted in clock noise figures much smaller than reported elsewhere. Even the small remaining excess background noise can be attributed to spurious charge flow induced into the CCD by the clock waveforms. The difficulty of calibration of on-chip amplifiers and their dubious linearity and noise performance make them unsuitable for serious investigations of device behaviour.

#### ACKNOWLEDGEMENTS

The author is deeply indebted to T.G. Groves, G. Haywood and P. Townsend for the construction of the special equipment and assistance in the measurements and to R.A. Harris of the Hirst Research Centre of G.E.C. for the supply of the CCDs and many useful discussions.

#### BIBLIOGRAPHY

- (1) A.B. Gillespie, "Signal, noise and resolution in nuclear counter amplifiers". McGraw-Hill Book Company, New York, 1953
- (2) V. Radeka, "State of the art of low noise amplifiers for semiconductor radiation detectors". Proc. International Symposium on Nuclear Electronics, Versailles, 1968
- (3) R.L. Chase, "Nuclear Pulse Spectrometry". McGraw-Hill Book Company, New York, 1961
- (4) K. Kandiah and A. Stirling, "A direct coupled pulse amplifying and analysing system for nuclear particle spectrometry". National Academy of Sciences, Publication 1593, pp 495-505, Washington, 1969
- (5) V. Radeka, "Signal processing for high resolution pulse amplitude spectrometry". *ibid* pp 511-522
- (6) M.F. Tompsett, "Surface potential equilibration method of setting charge in charge-coupled devices". IEEE Trans. Electron Devices, Vol ED22, pp 305-309, June 1975
- (7) C.N. Bergland and K.K. Thornber, "Incomplete transfer in charge-transfer devices". IEEE J. Solid-State Circuits, Vol S.C.8, pp 108-116, Apr. 1973
- (8) A.M. Mohsen, M.F. Tompsett and C.H. Sequin, "Noise measurements in charge-coupled devices". IEEE Trans. Electron Devices, Vol E.D.22, pp 209-218, May 1975
- (9) J.E. Carnes, W.F. Kosonocky and P.A. Levine, "Measurements of noise in charge-coupled devices". RCA Review Vol 34, pp 553-565, Dec. 1973