THE MEASUREMENT OF NOISE IN BURIED CHANNEL CHARGE COUPLED DEVICES*

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ABSTRACT. The noise in buried channel charge coupled devices was measured and was found to be composed of noise from four sources, output amplifier noise, dark current noise, electrical input noise and bulk state trapping noise. Because of the low levels of noise achieved in the output amplifier and in the electrical input of signal it was possible to make direct measurements of the dependence of bulk state trapping noise on input signal, clock rate and spectral frequency. The measured results for all the noise sources were found to be in satisfactory agreement with theoretical expectations.

I. INTRODUCTION

In this paper an investigation is made of the noise sources which limit the dynamic range of a buried channel charge coupled device (CCD) linear shift register. There were four sources of noise which were observed; output amplifier noise, dark current noise, electrical input noise and bulk state trapping noise. The noise level of each of these sources was found to be in reasonable agreement with the theoretical expectations.

A procedure was developed and will be presented in Section V which made it possible to separate the relative contributions of each of the above four components of noise. However, in order to perform this separation, an output amplifier was needed which had a very low noise level. It was found that satisfactory noise levels could be obtained by the use of correlated double sampling[1] (CDS) if very careful optimization of band limiting and pulse timing was employed. A noise analysis will be given in Section VI which identifies the tradeoffs involved in this optimization. Using the results of this analysis it was possible to obtain noise levels of less than 30 e^- (rms noise electrons).

In Section VII the dark current noise as expected was found to be well characterized by shot noise and for our devices at a 500 kHz clock rate, a typical value of noise due to dark current was 20 e^-.

A low noise design of the "fill and spill" type input was used which will be described in Section VIII.[2,3,4] This input structure made it possible to electrically inject very low noise signals. The dependence of this noise on signal size was found to be in satisfactory agreement with a simple phenomenological theory.

Because of the low noise levels which were obtained for the previous three noise sources, it was possible to make extensive direct measurements of the noise due to bulk state trapping, the level of which ranged from less than 10 to greater than 100 noise electrons. In Section IX measurements of the spectral density of bulk state trapping noise will be presented as well as its dependence on input signal and clock rate.[5] The most abundant bulk trap was identified as being introduced by gold impurities which had a density on the order of $10^{11} cm^{-3}$.

In Sections II-V general information is given about the test device, measurement procedures and data presentation. In particular, in Section II a description of the device will be given as well as some of its performance characteristics. In Section III a few definitions will be

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presented and in Section IV the test instrumentation will be described.

In Section V a summary is given of the characteristics of the four observed noise sources, which are described in detail in Sections VI-IX.

II. TEST DEVICE CHARACTERISTICS

A portion of the 150 stage linear shift register which was used exclusively in these noise measurements is shown in Figure 1. It makes use of overlapping gate, four phase clocks (600 charge transfers) with an electrode size of 7.5 μm x 125 μm. The metallization masks were compatible with both $A\ell$-$A\ell_2O_3$-$A\ell$[6] and poly-silicon-aluminum double level metal systems.[7] Both of these metallization methods were used in fabrication without noticeable effect on device operation. The thermally grown oxide under the metal gates was typically 1300 Å thick and it was grown on ⟨100⟩ oriented, p-type substrates with a typical resistivity of about 30 Ω-cm. The n-type layer in the active CCD area which when depleted forms the buried channel[8] was introduced by ion implantation followed by a short drive-in diffusion. The ion implantation dose was typically $1.5 \times 10^{12} cm^{-2}$ of phosphorus ions and the resulting depth after diffusion of the buried channel ranged in depth from 2000-3000 Å from the SiO_2-Si interface.

The CCDs were selected so that only those devices which exhibited low transfer inefficiency and dark current were used in the measurements. The transfer inefficiency was less than 1×10^{-5} (fraction of the signal packet lost each transfer) in the best devices but was more typically on the order of 2×10^{-5}. The dark current ranged from 3-8 na/cm^2 and the devices were also checked to eliminate those which exhibited points of localized avalanching (spikes). Measurements were made using gate controlled diodes on the same I.C., to separate the bulk and surface contributions to the dark current and in this way bulk lifetimes of 200 μs were determined with surface recombination velocities of less than 5 cm/sec.

An important characteristic in determining the performance of a buried channel device is the distribution of the signal charge in the buried channel.[9] This distribution is controlled by the profile of the n-type buried channel layer and for use in later sections the calculated distribution of signal charge is shown in Figure 2 for the impurity profile, $N_{IM}(X)$, (shown as the dashed line in Figure 2) given by

$$N_{IM}(X) = \frac{2 N_{DOSE}}{\sqrt{\pi}\, X_g} e^{-\left(\frac{X}{X_g}\right)^2} - N_A \qquad (1)$$

where $X_G = .2\mu$, $N_A = 5 \times 10^{14} cm^{-3}$ and $N_{DOSE} = 1.0 \times 10^{12} cm^{-2}$. In this figure a one dimensional plot of the charge distribution is shown in the direction from the $Si\text{-}SiO_2$ interface (X = 0) into the silicon. The charge is shown in Figure 2 to be located in a layer which extends from .11 μm to .16 μm for a signal charge of 7.3×10^9 e^-/cm^{-2}. This layer is observed to increase in width and move closer to the surface as the quantity of signal charge is increased. This property of the signal charge in buried channel devices will be found to significantly affect their noise characteristics.

III. DEFINITIONS AND NOTATION

Throughout this paper the measured rms noise voltage levels will always be presented as the number of rms noise electrons referred to the charge packet in the CCD channel.

In order to simplify comparisons between the spectral density and rms voltage measurements and to facilitate comparison of measurements at different clock rates, the units which will be used in the spectral density measurements will be the "equivalent" number of rms noise electrons, n(f), which is defined by

$$n^2(f) = \frac{1}{R^2} \frac{V_{WA}^2}{B} \frac{1}{G^2(f)} \left(\frac{f_c}{2}\right) \qquad (2)$$

in which R (volts/electron) is the responsivity of the entire output circuit which includes source follower, CDS circuit and high gain amplifier, $V_{WA}(f)$ is the wave analyzer reading over a bandwidth, B, which is centered at a frequency f. The function G(f) characterizes the sample and hold output waveform and for a sample pulse which is much shorter than the clock period, G(f) is given by

$$G(f) = \frac{\sin(\pi f T_c)}{\pi f T_c} \qquad (3)$$

To calculate the actual number of rms noise electrons, n, from the wave analyzer reading the following expression should be used.[10]

$$n^2 = \frac{1}{R^2} \int_0^{f_{c/2}} \frac{V_{WA}^2(f)}{B} \frac{1}{G^2(f)} \, df \qquad (4)$$

Therefore, n(f) is equal to n when the spectrum is white (independent of frequency) but for a general non-white spectrums (e.g., the noise from bulk state trapping), n and n(f) are related by

$$n^2 = \frac{2}{f_c} \int_0^{f_{c/2}} n^2(f) \, df \qquad (5)$$

The notation which will be used is that actual rms noise electron values (Eq. 4) will be denoted by n_i in which the subscript, i, will denote the particular noise source. To denote the spectral density as the equivalent number of rms noise electrons (Eq. 2) the argument, f, is added, $n_i(f)$, which identifies the frequency at which the spectral density is being evaluated.

In order to provide a noise source "standard" to check the accuracy of the overall measurement setup an optical input was introduced by a simple light bulb placed in a light tight box over the CCD (as shown in Figure 3). By monitoring the average current out of the device using the ammeter in the drain of T_1, it is possible to calculate the number of optically introduced electrons, N_{opt} from which can be calculated the expected shot noise level of $(N_{opt})^{\frac{1}{2}}$. This calibration procedure gave confidence that the noise measurement accuracy was within ± 10%.

IV. TEST INSTRUMENTATION

The test setup used for the noise measurements is shown in Figure 3. A standard floating diffusion output was used (which will be discussed later) which is composed of the on-chip MOSFETS T1 and T2. In the drain of the reset transistor T1 an ammeter is shown which is used to determine the responsivity, R(volts/electron), of the CCD output by measuring the change in current corresponding to a change in the output voltage. The output of the CCD I.C. at point B is then processed using a circuit which implements correlated double sampling (CDS).[1] The CDS circuit performs two functions; first, it removes the noise introduced by the preset of node A by T1, and it also converts the output into a sample and hold format which can be amplified without saturating a high gain amplifier. The amplifier which was used had a gain of 200, and an equivalent input spot noise level of 3 nv/Hz$^{1/2}$. The output of this amplifier was then fed into either a wave analyzer (HP 310A) which has a 3000 Hz bandwidth for spectral density measurements or into a multi-channel analyzer (MCA) for rms voltage measurements. The MCA was operated in the mode which provides a visual display and storage of the amplitude distribution of the noise which is Gaussian for all the CCD noise sources (as expected for most physical noise sources). An advantage of this approach for rms voltage measurements is that spurious non-Gaussian signals (e.g., 60 Hz) can be easily identified and then eliminated.

V. NOISE SOURCES

As discussed in the introduction, an important purpose of this investigation was to determine whether the theoretical understanding of the CCD noise sources is consistent with experimental evidence. The four types of noise which were observed were due to; 1) Output amplifier, 2) Dark current, 3) Electrical input and 4) Bulk state trapping.

A brief description will now be given of each of the above contributions along with a procedure which makes it possible to investigate individually the noise from each of the four sources.

1) OUTPUT AMPLIFIER

Output amplifier noise will be described in Section V and will be defined as the noise generated after the last CCD transfer has taken place. In the experimental setup shown in Figure 3 the largest contribution to the noise of the output amplifier was generated by the thermal or Johnson-Nyquist noise in the source follower, T_2. A small amount of additional noise was generated in the CDS circuit following T_2. The output amplifier noise could be separated from the other three noise sources by simply reversing the direction of the CCD clocks. All dark current (thermally generated minority carriers) will then be clocked out the input diode (which is biased with a high D.C. voltage) so that any noise measured at the wave analyzer (or MCA) is due only to the output circuits.

2) DARK CURRENT

Dark current noise will be briefly discussed in Section VII and is due to the thermal generation of electrons at the SiO_2-Si interface and in the bulk material.[15] Since this generation is totally random, the collection of these carriers into the buried channel results in full shot noise on the number of generated electrons.[11] This is a white noise source, the amplitude of which can be determined by measuring the noise while the device is being clocked forward without electrical input of charge and then subtracting the output amplifier noise which was measured when the device was being clocked in reverse. As usual in subtracting (or adding) noise voltage, the subtraction (or addition) is in quadrature, i.e., the measured noise voltages must be converted to power (voltage squared) before the two noise levels are subtracted (or added).

3) THE ELECTRICAL INPUT NOISE

The electrical input noise was measured on a "fill and spill" type input (see Section VIII) which was especially designed for low noise operation. The separation of this noise from the output amplifier and dark current contributions can be performed by simply subtracting out in quadrature the noise measured without any introduced signal. The separation of input noise from the bulk state trapping contribution is somewhat more difficult in that it is necessary to make use of their characteristic spectral distributions. This is possible because the correlated nature of bulk state trapping noise[12] results in a suppression of the noise at low spectral frequencies so that the noise measured at these frequencies is due only to the spectrally flat input noise.

4) BULK STATE TRAPPING NOISE

Bulk state trapping noise was found to account for all the remaining noise after the noise due to the above three sources were subtracted out in quadrature from the measured readings. It is easily identifiable because of the above mentioned spectral density frequency distribution resulting from the correlated aspect of this noise.[12] This noise source also has a relatively strong dependence on clock rate and input signal[5] and in Section IX measurements will be presented which will explore these dependences.

VI. OUTPUT AMPLIFIER NOISE

A critical aspect of noise measurements (and operation in general) of CCDs is the performance of the charge detection circuitry. The method used in these measurements was correlated double sampling (CDS) which was developed by M. White, et. al,[1] for low light level image arrays. This technique not only has the capability if properly implemented to achieve very low noise levels but has the additional advantages of being linear, stable and that implementation can be easily performed off chip (or on-chip) with only a few MOSFETS. Also, the final output is in a sample and hold format which is important for noise measurements because it minimizes signal power at the clock rate and therefore allows high gain amplification.

In spite of the apparent simplicity of this technique it was found that only by careful optimization of the timing of the sampling pulses as well as introduction of appropriate filtering was it possible to achieve noise levels below 30 noise electrons. In order to understand the tradeoffs involved in this optimization a large part of this section will be devoted to a noise analysis of this output. Also the contributions of the various noise sources in the circuit which was implemented will be discussed. First, however, a brief review will be given of the operation of CDS, as well as discussion of the circuits used for the implementation.

IMPLEMENTATION OF CORRELATED DOUBLE SAMPLING

Figure 4 is a schematic representation of the circuit which was used to implement CDS. The portion of this circuitry which wason the CCD I.C. (on chip) is composed of two MOSFETS, T_1 and T_2. The purpose of transistor T_1 (shown as a switch) is to preset the output capacitance, C_o, (the capacitance of node A) to a voltage sufficiently high to deplete the buried channel. The signal packet is then transferred onto this capacitance and discharges it towards ground. The resultant change in voltage is sensed by the source follower amplifier T_2 and is brought off the chip at point B. The voltage waveform which is observed at point B is shown in Figure 5. The preset takes place in the time interval from t_o to t_1 and the signal transfers onto node A at time t_3. It is well known that because of the thermal noise in the channel of T_1

there is a noise due to the preset operation given by [1,11]

$$n_1 = \frac{1}{q}(kTC_o)^{\frac{1}{2}} = 400e^- C_o(pf)^{\frac{1}{2}} \quad (6)$$

The output capacitance of the device used in these measurements was $C_o = .25$ pf which would yield the unacceptably high noise level of 200 e^- if the output were taken at this point without further processing.

The CDS technique provides an approach for removal of this preset noise.[1] As discussed by White, et. al.,[1] when the preset switch is opened node A has a time constant given by $R_{off}\ C_o$ where R_{off} is the resistance to A.C. ground of node A when transistor T_1 is off and is typically $> 10^{10}\,\Omega$. The preset noise, n_1 will therefore be correlated between any two samples which are taken after the preset at t_1. A discussion of this correlation is given in Appendix A. Therefore if the output is taken to be the difference in voltage of the samples at times t_2 and t_4 (shown in Figure 5) subject to the constraints $t_1 < t_2 < t_3 < t_4 < t_5$. The preset noise will approximately cancel and only the change in voltage due to the transfer of the signal charge will be observed. If the time between the two samples (t_4-t_2) is too long compared to the time constant $R_{off}\ C_o$ then the correlation of the noise is decreased and the noise level, n_A, will be measured[13] (see Appendix A)

$$n_A = n_1\left[2\left(1 - e^{\frac{-(t_4 - t_2)}{R_{OFF}\ C_o}}\right)\right]^{\frac{1}{2}} \quad (7)$$

where n_1 which is given by Equation 6 is the preset noise without CDS. The effective value of R_{off} which was observed was on the order of $10^8\,\Omega$ which required the interval t_4-t_2 to be less than 5 μsec for suppression of the preset noise. The reason for this low value of R_{off} is thought to be due to surface leakage. Therefore, if very low frequency operation is desired then care should be taken to reduce this leakage.

If the interval t_4-t_2 is much greater than $R_{off}\ C_o$ the preset noise will actually be increased by the use of CDS.[13] This increase occurs because the noise voltage sampled at the times t_2 and t_4 are then totally uncorrelated and when the difference in voltage is taken between these two samples the noise, n_1, from each sample adds in quadrature and yields a resultant noise level of $\sqrt{2}\,n_1$ which can be seen from Eq. 7.

The circuit which was used to take the difference in the two samples is shown in Figure 4. The signal was capacitively coupled at point B by capacitor C_c and the clamped to a D.C. voltage at time t_2. The voltage difference was sampled and held on capacitor C_{SH} by briefly closing MOSFET switch T_5 at time t_4. The buffer amplifiers T_4 and T_6 were both MOSFET source follower circuits.

NOISE OF CLAMP AND SAMPLE CIRCUITS

In this and the following sections expressions will be obtained and evaluated for the various noise sources which contribute to the total output noise and they will be evaluated and compared with the measured results.

The clamping of capacitor C_c and the sampling by T_5 which sets C_{SH} are subject to the same considerations applied to the preset of node A (Eq. 6) with respect to the uncertainty of voltage on capacitors C_c and C_{SH} except there is no suppression by the double sampling. Therefore, the equivalent number of rms noise electrons referred to the CCD channel, n_D, resulting from the clamping operation at time t_2 is given by,

$$n_D = \frac{1}{q}\frac{C_o}{A_2}\left(\frac{kT}{C_c}\right) \approx \frac{400\ e^-}{A_2} C_o(Pf)C_c\ (pf)^{-\frac{1}{2}} \quad (8)$$

in which A_2 is the gain of MOSFET amplifier T_2. A similar expression can be obtained for noise due to the sample and hold,

$$n_E = \frac{1}{q}\frac{C_o}{A_2A_4}\left(\frac{kT}{C_{SH}}\right)^{\frac{1}{2}} \approx \frac{400\ e^-}{A_2A_4} C_o(Pf)C_{SH}\ (pf)^{-\frac{1}{2}} \quad (9)$$

in which A_4 is the gain of amplifier T_4.

Choosing suitably large values of C_c and C_{SH} will result in a negligible contribution of noise from the clamp and sample operations. For the circuit which was actually implemented the calculated noise levels from these sources are $n_D = 7\ e^-$ and $n_E = 9\ e^-$.

The noise contributed by the buffer source follower amplifiers T_4 and T_6 can also be made acceptably small by proper choice of components. In the realization used in these measurements standard n-channel MOSFETS were used which had a low white noise (thermal noise) component but unfortunately had a rather high 1/f noise which was characterized by a corner frequency near 100 kHz. An increase in the output noise at low frequencies was observed due to this excess noise but it was not sufficiently large to significantly degrade the subsequent measurements of other noise sources.

1/f NOISE OF SOURCE FOLLOWER, T_2

The rms noise contributed by the amplifiers T_4 and T_6 is unaffected by the CDS operation, however, the noise generated by amplifier T_2 is substantially modified because the noise is generated before the CDS circuit. One effect on the noise of T_2 which was pointed out by White, et.al.[1] is that noise at frequencies that are much less than $(t_4-t_2)^{-1}$ is substantially suppressed. This characteristic of CDS is especially effective in suppressing the 1/f noise of T_2 as long as the 1/f corner frequency of T_2 is sufficiently low. If on the other hand the 1/f noise corner is significantly greater than $(t_4-t_2)^{-1}$ then excess noise will be measured at the output. Since 1/f noise in MOSFETS is believed to be due to trapping in surface states, substantial reduction in 1/f noise can be obtained if these transistors are operated in a buried channel mode (i.e., the signal is away from the Si-SiO_2 interface). In Figure 6 the spectral density of the noise for several surface and buried channel transistors shows the improvement obtained with the buried channel devices. To fabricate a buried channel transistor it is only necessary to implant the MOSFET with the same dose which was used to make the buried channel CCDs and to then operate at sufficiently low current levels to keep the channel buried. These devices have a 1/f corner around 50 kHz which is seen to be well over an order of magnitude lower than the surface channel device which are identical to the buried channel devices in all respects except they did not receive the implant.

For reasons which will be discussed below, the time interval $(t_4-t_2)^{-1}$ should be set to 2 f_c, so that for clock rates greater than 25 kHz substantial suppression of the 1/f noise will occur for a buried channel MOSFET, while a large amount of excess noise will be introduced at the lower clock rates if a surface channel MOSFET were used.

THERMAL NOISE OF SOURCE FOLLOWER, T_2

Besides suppressing the 1/f noise of transistor T_2, the CDS circuit also affects the white (thermal) noise component generated by this device. In Figure 7 the level of this noise is typically seen to be approximately 9 nv/$Hz^{\frac{1}{2}}$. Unfortunately the effect of CDS is to increase the contribution from this source instead of suppressing it. In fact it will be shown that this noise component is the dominant source of noise in the entire output amplifier. The optimization of timing and band limiting which was referred to in the Introduction, which will now be discussed, is an attempt to decrease the contribution of noise from this one source.

The purpose of the single pole low pass filter with time constant R_1C_1 which follows T_2 in Figure 4 is to band limit the thermal noise of transistor T_2 and thus to reduce its contribution to the rms noise. The effect of this bandlimiting is to introduce correlation of this noise between the two samples at t_2 and t_4. Taking this correlation into account the resultant rms noise after band limiting and double sampling is given by (see Appendix A),

$$n_B = \frac{C_o \sqrt{V_{T_2}}}{qA_2} \left(\frac{1}{4\ R_1C_1}\right)^{\frac{1}{2}} \left[2\left(1 - e^{\frac{-(t_4-t_2)}{R_1C_1}}\right)\right]^{\frac{1}{2}} \quad (10)$$

in which V_{T_2} is given by[16]

$$\sqrt{V_{T_2}} = A_2 \left[4kT\left(\frac{3}{2}\, g_m + \frac{1}{R_L}\right)^{-1}\right]^{\frac{1}{2}} \quad (11)$$

where $A_2 = g_mR_L/(1 + g_mR_L)$, R_L is the load resistor of the source follower and g_m is the transconductance of the MOSFET T_2. From Eq. 10 it can be seen that either decreasing the bandwidth of the R_1C_1 filter (increasing the band limiting of the wide band noise $\sqrt{V_{T_2}}$) or decreasing the ratio (t_4-t_2/R_1C_1), (increasing the correlation between the two samples), will result in a decreased noise level. Therefore, it would appear desirable to increase R_1C_1 while

decreasing the time between the clamp and sample pulses. However, as the time constant R_1C_1 of the filter is increased the voltage swing which represents the signal is attenuated by the factor, $[1-e^{-(t_4-t_3)}/R_1C_1]$. To maximize this factor the largest possible amount of time should be given for the signal transient to occur. Therefore, the sample at t_4 should occur just before the following preset occurs at t_5(see Figure 5).

Another consideration which also limits the maximum size of R_1C_1 is that a fraction $e^{-(t_2-t_1)/RC}$ of the preset noise, n_A, will remain after the clamp has occurred because of the correlation effects introduced by the bandlimiting.[14] This fraction can be decreased by minimizing the width of the preset pulse ($t_1 \approx t_o$) and by clamping (i.e., the sample at t_2) just before the signal is transfered at t_3. Therefore, the tradeoff involved in choosing the bandwidth of the low pass filter; R_1C_1, is that the wide band noise of T_2 should be bandlimited to as low a frequency as possible which implies a long time constant; however, this long time constant attenuates the signal swing as well as decreases the preset noise suppression.

A suitable compromise of the above considerations is to allow three to four time constants (R_1C_1) between the preset and clamp pulses as well as between signal transfer and the sample pulse. The optimum timing subject to this constraint is given by

$$t_1 - t_0 \ll T_c \qquad (12)$$

$$t_2 - t_0 \approx t_3 - t_o \approx \frac{t_c}{2} \qquad (13)$$

$$t_4 - t_0 \approx T_c \qquad (14)$$

and to obtain four time constants for the above mentioned intervals the low pass filter should have a bandwidth, $f_{3dB} = 1/2\pi R_1C_1$, given by

$$f_{3dB} \approx \frac{4}{3} f_c \, . \qquad (15)$$

From Equation 14 it is found that with this band limiting and timing sequence that the effect of CDS on the noise, V_{T_2}, (Eq. 11) generated in T_2 is to increase the rms level by a factor of $\sqrt{2}$ over the noise level which would be obtained without CDS. This increase in noise is due to the lack of correlation which exists between the clamp and sample pulse because the band limiting (which has been optimized taking this effect into account) is too wide to provide correlation between the two samples. The effect is similar to that discussed in Section VI in which the preset noise could also be increased by a factor of $\sqrt{2}$.

Evaluating Eq. 10 for the rms noise due to the thermal noise of T_2 at a clock rate of 500 kHz, including processing by the CDS circuit (with timing and bandlimiting given in Eqs. 11-14) yields a rms noise level of n_B = 21 e^-, which as pointed out previously is the largest noise source in the output amplifier.

OUTPUT AMPLIFIER NOISE MEASUREMENTS

Evaluating Eqs. 8, 9 and 10 and summing the results (in quadrature) results in a total expected output amplifier noise level of 25 e^-. In the lower curve in Figure 7 the measured output amplifier noise is shown for a CCD which is being clocked in reverse so that all dark current will be clocked out the input which isolates the noise due to the output circuit. The measured value of 27 e^- agrees very well with the expected value. At low frequencies the noise is seen to increase and this is due to 1/f noise of the off chip MOSFETS T_4 and T_6 as discussed earlier in this section. The simplest method to decrease the noise level of the output amplifier is to decrease the capacitance, C_o, of the output node. This procedure linearly increases the responsivity of the output without increasing the noise voltage of any of the sources which have been considered. Since the noise is referred to the CCD channel the equivalent number of noise electrons, therefore, decreases linearly with this capacitance. It is expected an overall noise level of 10 e^- could be achieved with a design of the output node which minimizes C_o.

VII. DARK CURRENT NOISE

In the last section the noise which was analyzed was the observed noise when the device was clocked in reverse. In this section will be discussed the origin of the additional noise which is measured when the device is clocked normally. There is, however, not yet any intentionally introduced signal charge.

Since a CCD (buried or surface channel) is operated in deep depletion there exists a thermal generation of carriers which is attempting to re-establish an equilibrium condition.[15] The electrons generated in this way are collected in the buried channel along with the signal charge. The variation in the amount of electrons generated and subsequently collected is characterized by shot noise, i.e., the number of rms noise electrons is the square root of the mean value of the collected electrons. For a dark current level of J_D(amp/cm^2) the number of rms noise electrons, n_{J_D} is given by

$$n_{J_D} = \left(\frac{J_D A_S M}{q f_c}\right)^{\frac{1}{2}} \qquad (16)$$

where A_S is the area of single stage (four gates for a four phase device) and M is the number of stages.

In the upper curve of Figure 7 the measured noise is shown for a device which is clocked normally but the input is biased so that there is no electrical introduction of signal charge. The increase in noise from the lower curve which is being clocked in reverse is due to dark current. If these two curves are subtracted in quadrature a noise level of 21 e$^-$ is determined which is due to dark current and is in good agreement with the value obtained from Eq. 16.

In general the dark current was found to be characterized by shot noise as was the case for the device in Figure 7, however, for devices in which localized avalanching was occuring (spikes) the noise was sometimes in excess of shot noise.

VIII. INPUT NOISE

In sections VI and VII the noise was determined for a CCD which is operated without intentionally introduced signal charge. This section and the next on bulk trapping noise will investigate those noise sources which are only present when there is signal charge being introduced. In order to separate the two components of this noise it is necessary to make use of their characteristic spectral distributions. In Figure 8 the measured spectral density for device A in units of equivalent rms electrons squared (noise power) is plotted for the signal dependent noise.

This noise can be separated into a white noise component which is due to the electrical input of the signal charge and a part which has a $(1 - \cos 2\pi f/f_c)$ frequency dependence. This is the dependence to be expected for bulk state trapping[12] and will be investigated further in Section IX. From Figure 7 it is obvious that in order to separate out the input noise contribution it is only necessary to measure the spectral density at low frequency, where the trapping noise is suppressed. All the measurements presented in this section were made using this technique.

The method of introducing the input signal which was used was based on a low noise scheme which was developed independently at Bell Labs,[3] Texas Instruments,[3] and RCA.[4] This approach which will be called the "fill and spill" method involves application of the signal to an input gate (see Figure 9). The diode voltage is initially set so that there is no charge introduction into the channel. The input diode is then pulsed so that a full well of charge is introduced into the first CCD well. The diode voltage is then restored to its initial level and the capacitance associated with the receiving well is then discharged to a voltage level set by the signal on the input gate. At the termination of this process, charge stored in the pinched-off transfer channel, under the input gate is minimal, and uncertainties associated with its removal path are small. The amount of charge introduced is the difference between the input and the clock voltages times the capacitance of the receiving well, C_{in}. Analyses predict that the number of rms noise electrons, n_{in} which are introduced into the signal packet using this input technique is given by

$$n_{in} = \frac{1}{q} (\alpha\, kTC_{in})^{\frac{1}{2}}, \qquad (17)$$

In which α is on the order of one[18] In order to reduce the input noise it is only necessary to reduce the size of the input capacitance, C_{in}. This was done by constricting the channel stop under the first ϕ_1 well so that the channel width was only 12 μm wide as shown in Figure 10. Since the operation of a buried channel

transistor in the regime near cutoff not well understood, α will be treated as a parameter and its value will be determined by fitting the data.

In the usual analysis the capacitance, C_{in}, is assumed to be a constant value, independent of signal size. For a buried channel input, however, as the signal size decreases the input capacitance decreases. There are two effects which cause this decrease. In Figure 2 the distribution of the signal charge is shown into the silicon and as discussed in section II, the distance from the gate to the signal packet increases with decreasing signal, thus decreasing the capacitance. The second effect which decreases the effective capacitance for small signals is that the area that the signal charge occupies decreases since a small value of signal charge will not cover the entire region under the gate. The signal packet contracts toward the potential minimum which lies at the center of the gate.[14]

To experimentally determine the actual capacitance of the input node, a small change in voltage, ΔV, was made on the input gate, which was biased at a voltage corresponding to an input of N_{SIG} electrons, and the corresponding change in charge level, ΔQ, was monitored at the output. The capacitance, $C_{in}(N_{SIG})$, was then calculated from the expression

$$C_{in}(N_{SIG}) = \frac{\Delta Q}{\beta \Delta V} \quad . \qquad (18)$$

The factor β takes into account the imperfect modulation of the buried channel potential by the gate above it. For the devices tested the measured value of β was experimentally determined to range from 0.8 to 0.9. A typical result of this measurement is that the input capacitance varies from 0.004 pF for an input signal level of 2.5×10^4 e^- to 0.013 pF at 6×10^5 e^-. The input noise would, therefore, be expected to increase by a factor of 1.8 over this signal range.

In Figure 11 the measured value of input noise for device B is compared to the calculated value obtained using the capacitance values determined using Eq. 18 and an excellent fit to the data results for $\alpha = 1.1$ in Eq. 17.

A very important point to note in this figure is the extremely low noise levels that were obtained for very small signals. For example only 10 noise electrons were introduced for the signal level of 6.2×10^3 e^-. The rapid decrease in noise for very small signals ($< 10^4$ e) is due to the decrease in area occupied by the signal charge. It is therefore, possible to inject very low noise bias charge levels (slim zeros). These bias charge levels are necessary to obtain optimum performance with buried channel devices.

At higher signal levels the noise increases to approximately 50 noise electrons, this is still a very low level (about 5 times lower than any previous reported results) and verifies the expected low noise characteristics of the input structure shown in Figure 10.

There are some special characteristics of this structure, however, which may limit its usefulness in certain applications that are more demanding than noise measurements. Due to the dependence of the input capacitance on signal level, the input has a rather non-linear relationship between charge and voltage. A second difficulty is that because of the restricted size of the first CCD well it would require large voltages on the input and the first CCD gate in order to introduce a full well of signal charge.

VI. BULK STATE TRAPPING

The extremely low noise levels which were obtained for the other three CCD noise sources has made possible extensive characterization of noise due to bulk state trapping. The spectral density of the trapping noise was measured, as was its dependence on clock frequency and signal level.

The trapping of signal charge in bulk states affects the transfer efficiency and noise of buried channel devices in a manner similar to the way surface states determine the noise and transfer efficiency of surface channel devices. A thorough discussion of these effects has been presented,[6,9,16] and only the points relating to the measurements to be presented will be reviewed in the next section. Following this review the results of spectral density measurements will be presented as a function of signal size and clock rate. In order to obtain the density and emission times of the bulk traps which are contributing to the noise the double pulse measurements of the loss will be presented. The double pulse technique

will then be extended to noise measurements and the emission times and densities obtained from these measurements will be compared with the results of the loss measurements.

REVIEW OF EFFECTS OF BULK STATE TRAPPING

The effect of impurities in the bulk silicon is to introduce trapping levels, which can be characterized by a single emission time. When a sufficiently large charge packet comes into contact with these traps they are rapidly filled. This fill time is strongly dependent on signal size, but except for very small signals it is extremely fast compared to standard clock rates (< 10 MHz). As the charge packet is transferred to the next electrode, these traps will emit a portion of the trapped signal charge and this reemitted charge will transfer along with the signal packet. However, after a transfer time T_t, additional emitted charge will reside in trailing charge packets, which results in charge loss from the initial packet. To determine the net amount of charge that is lost from a signal packet, it is necessary to know the initial occupancy of the traps.

A simple case in which this occupancy can easily be determined is the case of a train of signal packets ("ones") which are followed by a series of N_z empty packets ("zeros"). The loss per transfer due to bulk trapping in the first "one" after N_z zeros is[6]

$$N_{loss}^{N_z} = M\, V_{SIG} \sum_i N_i\, e^{\frac{-T_t}{\tau_i}} \left[1 - e^{-N_z T_c/\tau_i}\right] \tag{19}$$

where V_{SIG} is the volume that the signal charge (the ones) occupy, N_i is the density of the i^{th} bulk trap which is characterized by an emission time τ_i, T_c is the clock period and M is the number of transfers.

The rms noise, $n_{B.T.}^{N_z}$, introduced into the first one after N_z zeros is[6]

$$(n_{B.T.}^{N_z})^2 = M\, V_{SIG} \sum_i N_i \Big[e^{-T_t/\tau_i}\left(1 - e^{-T_t/\tau_i}\right) + e^{-(N_z T_c + T_c)/\tau_i}\left(1 - e^{-(N_z T_c + T_c)/\tau_i}\right)\Big] \tag{20}$$

In the latter part of this section both the loss, $N_{loss}^{N_z}$ and the noise $n_{B.T.}^{N_z}$ will be measured as a function of N_z. From these measurements the density and emission times of the bulk states which are present in the buried channel will be determined by fitting the data to Eqs. 19 and 20.

Inspection of Eq. 19 and 20 indicates that knowing the transfer time T_t is very critical to interpretation of any data which is fit to these equations. However, the transfer time, T_t, is a somewhat difficult parameter to determine, since it depends strongly on the clock waveform used to drive the device and the dynamics of charge transfer. A simplified model to determine the dependence of the transfer time on clock waveform is outlined in Figure 12. In curve A of this figure the channel potential is shown with signal charge being stored under the ϕ_1 well. The bulk states will therefore be completely filled under this electrode. In curve B the signal packet has transferred to ϕ_2 and the charge emitted from the bulk states under ϕ_1 are swept into the adjacent ϕ_2 well. This is the beginning of the transfer time interval. In curve C the signal packet has transferred to ϕ_3, and the emitted charge is now sufficiently removed from the initial charge packet so that there is an equal probability for the signal charge to transfer along with the signal packet or to transfer into the following packet and this will be considered the end of the transfer time interval. Using this model the transfer time, T_t, for a four-phase device as a function of fractional overlap of adjacent clock phases is found to be

$$T_t = (.375 - Y/2)\, T_c \tag{21}$$

Since the overlap can vary from almost 0 to 3/4 a wide range of transfer times are possible for a single clock rate. This is in contrast to the usual assumption for T_t which is that $T_t = T_c/p$ where p is the number of clock phases.[6,11] From Eq. 16 and 23 it can be seen that the noise which is contributed by a given species of bulk trap can be varied substantially by simply varying the clock overlap, therefore care must be taken to keep the overlap constant in order to obtain consistent data especially in comparing data at different clock rates.

The noise due to bulk trapping has several distinctive characteristics which

make it simple to separate from the other CCD noise sources. Besides the dependence on the occurrence of signal charge (given by Eq. 20 for a simplified case) it also depends on the signal size. As the signal charge increases in size, the volume it occupies, and thus the number of bulk states it interacts with also increase. This is shown in Figure 2 in which the volume is seen to increase from a 500 Å wide layer for a small signal to a 1500 Å wide layer for a large signal. Figure 2 is a one-dimensional plot and therefore does not include the contraction of the signal packet to an area that is less than the size of the gate. These edge effects will be found to be important for very small signals and thus the volume (and therefore the noise) is found to decrease substantially at low signal levels.

The most unambiguous characteristic of bulk state trapping is the dependence of the spectral density on frequency and for the case of a continuous input signal the spectral density has been calculated by Thornber and Thompsett.[13] Their calculation has shown that because of the correlation which exists between noise in adjacent charge packets (a deficit in one packet results in excess in the adjacent packet) the spectral density has a distribution $n_{B.T.}(f)$, in units of equivalent rms noise electrons (see Section III), given by

$$\left(n^2_{B.T.}(f) \right)^2 = (n^0_{B.T.})^2 \left(1 - \cos\frac{2\pi f}{f_c}\right) \qquad (22)$$

where $n^0_{B.T.}$ is calculated by setting $N_z = 0$ in Eq. 20. This dependence was already exploited in the measurement of the input noise (see Section VIII) and will be used in the next part to provide unambiguous identification of the bulk state trapping noise. Therefore, it will be possible to obtain experimental verification of the above theoretical expressions and it will be found that satisfactory agreement was obtained in all cases. The first set of measurements to be described will be spectral measurements for varying signal levels and these will be followed by a series of rms voltage measurements in which the dominant bulk traps are identified.

SPECTRAL DENSITY MEASUREMENTS

The purpose of these measurements was to verify the spectral dependence predicted by Eqn. 22. In Figure 8 the noise power has been separated into two components. The dashed line represents the contribution of the input noise which was discussed in Section VIII, and added to this (since noise power is being summed it is a linear addition) is the noise due to bulk state trapping. The solid line is a fit to the trapping component of the noise by the expression for $n_{B.T.}(f)$ given in Eq. 22 in which $N^0_{B.T.}$ was used as a curve fitting parameter. The fit is found to be excellent for a value of $n^0_{B.T.} = 52\ e^-$. If only one type of bulk state is contributing to this noise and if it is assumed that this bulk state has an emission time of 0.7 μsec (so that the peak in the noise occurs at a 500 kHz clock rate), then a trap density of $1 \times 10^{11}\ cm^{-3}$ is required to obtain the measured noise level. Measurements as a function of clock rate, given later in this section, indicate there is a peak in the noise near 500 kHz so that the assumption of a 0.7 μsec trap emission time appears valid. It should be noted that the use of double pulse measurements discussed at the beginning of this section are a more accurate way to obtain the bulk state density[5] but it would require a high clock rate (> 5 MHz) to observe this .7 μsec level.

As discussed previously, as the size of the signal charge increases then the noise should increase. Figure 13 shows the spectral density of the bulk state trapping noise for signal levels from 1870 e^- up to $7.5 \times 10^5\ e^-$. As expected as the signal charge is increased, the amount of bulk state trapping noise, also increases. For each signal level the characteristic $(1 - \cos 2\pi f/f_c)$ spectral dependence is clearly observed. It is interesting to note that for the signal level of 6250 e^- the rms number of noise electrons was 42 e^-, whereas for the even lower level of 1870 e^- the rms number of noise electrons is only 16 e^-. For this range of input signal the number of noise electrons is decreasing almost proportionally with the signal level. This is due to the contraction of the charge packet to a reduced area in the center of the electrode. This result is significant for very low light-level imaging where it is important that trapping noise not degrade small signals.

A more direct plot of the bulk state trapping noise as a function of signal level is given in Figure 14 for three different

devices. In this figure the rms noise power is plotted as a function of signal level and is determined by integration of noise power curves like those in Figure 13 using Eq. 5. The noise is seen to rise rapidly at small signal levels (an increasing area of the electrode is being filled with signal) and then to rise slowly with further increases in signal size as the charge packet increases its volume by spreading toward the surface is shown in Figure 2. Even though all three of these devices were processed at the same time (in fact A and C were on the same slice), the bulk state trapping noise at $N_{SIG} = 4 \times 10^5$ e^- is quite variable ranging from 34 e^- for device B to 55 e^- for device D.

An important characteristic of bulk state trapping is its dependence on clock rate. Figure 15 shows a plot of the rms number of noise electrons for two devices, and the clock frequency dependence of the noise is readily observable. However, since there are no well-defined peaks and nulls in the noise, it is difficult to determine from this figure the individual emission times and densities of the bulk states that are giving rise to the noise. In fact, it seems likely that there are several states of varying densities and emission times which, when added together, result in the relatively smooth clock rate dependence seen in Figure 15. One aspect of this figure that can be commented on is the increase in noise of device A as the clock rate is decreased to 50 kHz. From double pulse measurements to be described in the next section identifies a bulk trap which has a 12 μsec emission time. From these measurements it is predicted that this trap should yield a peak noise of 55 e^- at a 45 kHz clock rate, which is consistent with the data presented here in Figure 16.

Figures 12 through 16 show data from only a few devices, but these results are typical of the much broader sampling that was measured. For a signal input of 5×10^5 e^- at a clock rate of 500 kHz the bulk trapping noise for 10 devices was found to range from a low of 37 e^- to a high of 96 e^-.

From spectral density measurements it is possible to unambiguously identify how much noise is due to bulk state trapping but it is difficult to extract information about which bulk traps are contributing to the noise. In the next section a different type of measurement will be described which measures the emission times and densities of these traps.

DOUBLE PULSE MEASUREMENTS OF LOSS

Equation 19 suggests a very simple measurement to determine the emission rates of the bulk traps[5] which is analoguous to the double pulse measurements first performed on surface channel devices by Carnes and Kosonocky.[11] The experiment proceeds by measuring the loss in the leading edge of a series of ones as a function of the number of zeros between sets of ones. If this is plotted on semi-log paper, using Eq. 19, emission times of the bulk traps can easily be identified.

In conducting these measurements on buried channel devices, a refined technique was developed. Reference to Figure 16(a) indicates the difficulty in accurately quantizing the transfer inefficiency of a very low-loss CCD shift register. It is unrealistic to expect accurate visual estimation of the leading edge loss or trailing edge residue. It is difficult to amplify this waveform and investigate the differences in the leading or trailing pulses without exceeding the dynamic range of the preamplifier or oscilloscope. Without an improved technique, the device in Fig. 16a would be described as having a charge transfer efficiency of about 0.99999. The improved procedure involves sequentially sampling-and-holding the CCD output resulting from the first and second packets in the pulse train. Since for a small amount of loss from the first packet, the sample-and-hold output is a dc level corresponding to the pulse-train level with a slight perturbation due to the difference in the first two pulse amplitudes, it is possible to ac-couple and amplify this difference without dynamic range problems. The resulting waveform is shown in Figure 16(b). The transition from the first pulse level to the second is clearly 10 mV. Since for devices with very small loss, the loss is confined to the first packet, the transfer efficiency can be calculated from this figure and is found to be .999992.

Figure 17 shows curves for two devices which give very close agreement with Eq. 19. The data are plotted as a function of time between pulse trains

instead of the number of zeros to facilitate the extraction of information about the emission time of the bulk states. The loss is expressed as a fraction of the signal packet lost out of the first one after N_z zeros. The solid lines in this figure are calculated curves using the expression given in Eq. 19. A summary of the results obtained from this measurement is given in Table I. The bulk state densities given in this table were calculated using a charge packet volume of 2×10^{-10} cm^{-3}, (which is obtained from a potential profile calculation) for devices A and B. The signal packet size used in the measurement was 7×10^5 e^- for both devices.

For device A there were two bulk states which contributed to the loss; one with emission time of 900 μsec and the other with a 12 μsec emission time. Device B only exhibited trapping by the bulk state with a 900 μsec emission time. Measurements of thermally stimulated capacitance[20] have shown that gold has an emission time of 900 μsec and on this basis the 900 μsec bulk state observed in these CCDs is identified as resulting from gold impurities. Further evidence for this identification is provided by Collett[19] who made variable temperature measurements on a buried channel MOSFET and determined that the bulk state which had a 900 μsec lifetime was located ~ .54 eV from the band edge which is the location of one of the gold trap energy levels.

The impurity which has a 12 μsec emission time that was observed in device A has not been identified.

DOUBLE PULSE MEASUREMENTS OF NOISE

From the double pulse measurements of loss several bulk states were identified. If a similar double pulse measurement is made but instead of measuring loss in the first "one" after N_z "zeros", the rms noise is measured, a peak in the noise should occur when the time between the ones, N_zT_c, is approximately equal to the emission time of these bulk states (Eq. 20). For example, for device A there should be a peak in the noise near 12 μsec and 900 μsec. In Figure 18 the measured noise of device A as a function of N_zT_c is shown and as expected the noise exhibits peaks near 12 μsec and 900 μsec. In addition, another peak is seen to appear which corresponds to an emission time of 20 ms which was out of the range of the loss measurements. In this Figure only the noise dependent on N_z is plotted, An expression for $n_{D.P.}^{N_z}$ can be derived from Eq. 20 by only keeping the terms dependent on N_z;

$$\left(n_{D.P.}^{N_z}\right)^2 = M\, V_{SIG} \sum_i N_i \, e^{\frac{-(N_zT_c + T_t)}{\tau_i}} \left[1 - e^{\frac{(N_zT_c + T_t)}{\tau_i}}\right] \qquad (23)$$

The solid lines in Figure 18 are a fit to the data using this expression in which the bulk state densities N_i are treated as a curve fitting parameter. The same emission times that were used to fit the data in the double pulse loss measurements in (Figure 17) were used in fitting this data.

The bulk densities determined to be a best fit are 2.0×10^{11} cm^{-3} for the bulk state with the 12 μsec emission time and 2.4×10^{11} cm^{-3} for the bulk states with the 900 μsec and 20 msec emission times. These values compare favorably with those obtained by the loss measurements which are given in table I for device A.

The two sets of data, shown as triangles and dots in Figure 18 correspond to two separate sets of measurements. The variation in these two sets of data gives an indication of the reproducibility of the measurement.

X. CONCLUSIONS

Noise measurements were made on a linear 150 stage buried channel CCD. The total device noise was found to be composed of four components; the electrical insertion of signal charge, bulk state trapping, dark current noise, and the output amplifier. We did not observe any of the extraneous excess noise sources such as pulser noise and abnormally high input noise which have been observed by previous authors.[13,20]

In making these measurements the concept of correlated double sampling[1] was used in an output amplifier which had a noise level which was equivalent to less than 30 noise electrons. The dominant noise sources in this amplifier were discussed.

A low noise input structure[2,3,4] for electrical insertion of signal charge was used which introduced a signal which had a noise level which ranged from 10 to 60 e^-.

The extremely low noise levels which were obtained at the input and output made possible direct measurement of the noise due to bulk state trapping. In fact, even for very high quality devices (transfer efficiency > .99999) because of the advances made in reducing the input and output noise, it was possible to observe the noise due to bulk states. The spectral density of the bulk state noise was presented as a function of frequency and signal level and was found to be in good agreement with the theoretical modeling for trapping noise.

APPENDIX A

ANALYSIS OF NOISE TRANSFER FUNCTION OF CORRELATED DOUBLE SAMPLING FOR BANDLIMITED WHITE NOISE

In this appendix the effect of the correlated double sampling on a band-limited white noise source, V_n, will be derived. The band-limiting will be assumed to be performed by an RC single-pole low-pass filter. If thermal noise in resistor R of this filter is non-negligible, it may be treated as all or part of V_n.

First, the autocorrelation function, R(t), of the band-limited noise must be derived. This can be found by taking the Fourier transform of the single-sided noise power spectrum $[V_n^2 H^2(\omega)]$,

$$R(t) = \frac{1}{2\pi} \int_o^\infty e^{j\omega t} V_n^2 H^2(\omega) d\omega \qquad \text{(A-1)}$$

where $H^2(\omega)$ is the transfer function of the low pass filter,

$$H^2(\omega) = \frac{1}{1+\left(\frac{\omega}{\omega_c}\right)^2} \qquad \text{(A-2)}$$

in which ω_c is the 3 dB point of the RC filter

$$\omega_c = \frac{1}{RC} \qquad \text{(A-3)}$$

Evaluating the integral of Eq. (A-1), the following result is obtained:

$$R(t) = V_n^2 B e^{-t/RC} \qquad \text{(A-4)}$$

where B is the noise bandwidth of a single-pole RC filter

$$B = \frac{1}{4RC} \qquad \text{(A-5)}$$

The rms output voltage of the CDS, V_{CDS}, is the difference in the input voltage level, V(t), at two points in time separated by a time interval Δt, which is given by[13]

$$V_{CDS}^2 = \lim_{T \to \infty} \frac{2}{T} \int_o^T [V(t)]^2 dt - \lim_{T \to \infty} \frac{2}{T_o} \int^T [V(t + \Delta t)]^2 dt \qquad \text{(A-6)}$$

where it has been assumed that V(t) is stationary. Using the definition of an autocorrelation function

$$R(\Delta t) = \lim_{T \to \infty} \frac{1}{T} \int_o^T V(t)V(t + \Delta t) dt \qquad \text{(A-7)}$$

$(V_{CDS})^2$ can be rewritten as

$$V_{CDS}^2 = 2 [R(o) - R(\Delta t)] \qquad \text{(A-8)}$$

Substituting (A-4) into (A-8) the following result is obtained:

$$V_{CDS} = [2V_n^2 B(1 - e^{-\Delta t/RC})]^{\frac{1}{2}} \qquad \text{(A-9)}$$

If this voltage level is referred to the CCD channel and then multiplied by the CCD output capacitance, the noise level is then converted into noise electrons, n_{CDS},

$$n_{CDS} = \frac{C_o V_n}{Aq} [2B(1 - e^{-\Delta t/RC})] \qquad \text{(A-10)}$$

where A is the amplification between the CCD output and the noise source v_n.

To obtain Eq. 7 the appropriate wide band noise, v_n, to substitute into A-9 is the thermal noise of R_{off}, $(4kT\ R_{off})^{\frac{1}{2}}$, which is band limited by $C_{o,1}$ resulting in a noise bandwidth of $B = \frac{1}{4R_{off}C_o}$.

For Eq. 10 the wide band noise of interest is given by Eq. 11 which is band limited by the R_1C_1 filter so that $B = \frac{1}{4R_1C_1}$.

REFERENCES

1. M. H. White, D. R. Lampe, F. C. Blaha, and I. A. Mack, "Characterization of Surface Channel CCD Imaging Arrays at Low Light Levels," IEEE Trans. Solid-State Circuits, SC-9, 1, (1974).

2. S. P. Emmons and D. D. Buss, "Techniques for Introducing A Low Noise Fat Zero in CCDs," presented at the Device Research Conference, Boulder, Colorado, June 1973.

3. M. F. Tompsett and E. J. Zimany, Jr., "Use of Charge-Coupled Devices for Delaying Analog Signals," IEEE Solid-State Circuits SC-8, 151 (1973).

4. J. E. Carnes, W. F. Kosonocky and P. A. Levine, "Measurements of Noise in Charge-Coupled Devices," RCA Rev. 34, p. 553 (1973).

5. A. M. Mohsen and M. F. Thompsett, "The Effect of the Device on the Performance of Bulk Channel Charge Coupled Devices," IEEE Trans. Electron Devices, Vol. ED-21, November 1974.

6. D. R. Collins et. al., "Electrical Characteristics of Long CCD Registers using Aℓ-$Aℓ_2O_3$-Aℓ Double Level Metallization," IEDM, December 1973, p.29.

7. Private Communication, Al Tasch.

8. R. H. Walden, et. al., "The Buried Channel Charge Coupled Device," BSTJ, September 1972, p. 1635.

9. R. W. Brodersen and A. F. Tasch, "Comparison of Two Types of Buried Channel Devices," Presented at the Device Research Conference, Santa Barbara, 1974.

10. S. P. Emmons and D. D. Buss, "The Performance of CCDs in Signal Processing at Low Signal Levels," CCD Applications Conference Proceedings, pp. 189-205, San Diego, California, September 18-20, 1973.

11. J. E. Carnes and W. F. Kosonocky, "Noise Sources in Charge-Coupled Devices," RCA Rev. 33, 327 (1972).

12. K. K. Thornber and M. F. Thompsett, "Spectral Density of Noise Generated in Charge Transfer Devices," IEEE Trans. on Electron Devices ED-20, 456 (1973).

13. Private Communication - George Root and Brock Barton.

14. D. F. Barbe, "Imaging Devices Using the Charge-Coupled Concept," Proc. IEEE, 63, 38 (1975).

15. A. F. Tasch, Jr., R. W. Brodersen, D. D. Buss, and R. T. Bate, "Dark Current and Storage Time Consideration in Charge Coupled Devices," Proc. of the CCD Applications Conference 1973, San Diego.

16. J. M. Early, "Effects of Bulk Trapping at Low Signal Levels," Presented at the Device Research Conf., Santa Barbara, June 1974.

17. A. M. Mohsen, M. F. Thompsett and C. H. Sequin, "Noise Measurements in Charge-Coupled Devices," IEEE Electron Devices, ED-22, May 1975, pp. 209-218.

18. D. D. Buss and W. Bailey, "Noise in Bucket Brigade Devices," To be published in IEEE Electron Devices.

19. W. G. Collet, "A New Method to Measure very Low Bulk Trap Densities in Silicon," Presented at Device Research Conference, Ottawa, Canada, 1975.

20. C. T. Sah, L. Forbes, L. I. Rosier, A. F. Tasch, Jr., and A. B. Tole, "Thermal Emission Rates of Carriers at Gold Centers in Silicon," Applied Physics Letters, Sept. 1, 1969, p. 145.

TABLE I

Device	Bulk State 1 Emission Time (μ sec)	Density cm^{-3}
A	900	1.7×10^{11}
B	900	1.7×10^{11}

Device	Bulk State 2 Emission Time (μ sec)	Density cm^{-3}
A	12	1.4×10^{11}
B	-	0

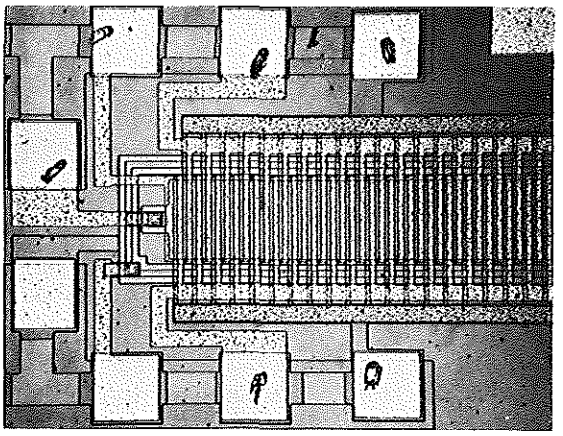

Figure 1. One end of the linear shift register used in the noise measurements.

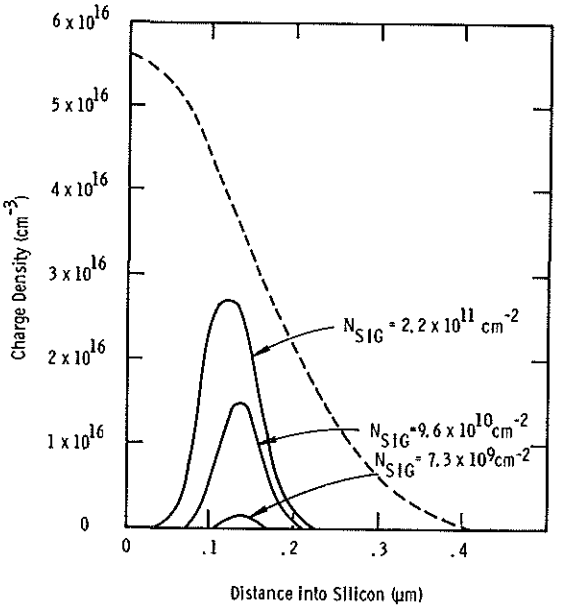

Figure 2. The charge distribution in the buried channel (solid line) shown with the impurity distribution (dashed line).

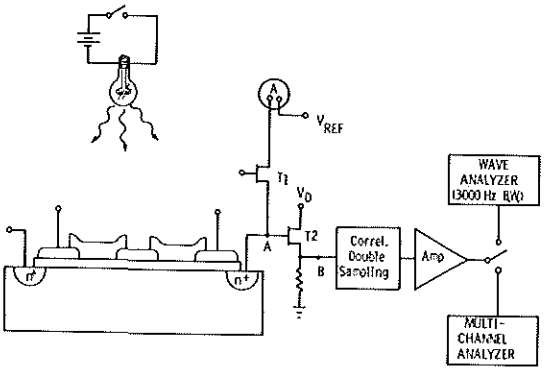

Figure 3. The test set-up used for the noise measurements.

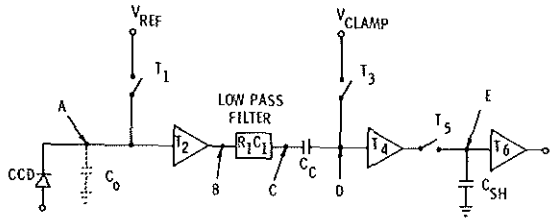

Figure 4. Schematic of the circuit used to implement correlated double sampling.[1]

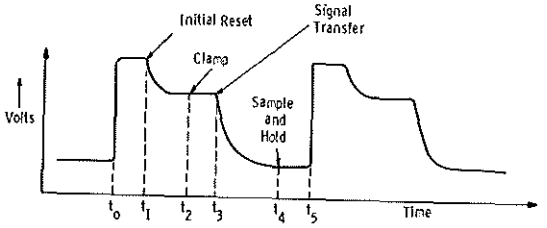

Figure 5. The voltage waveform observed at point B in Figure 4.

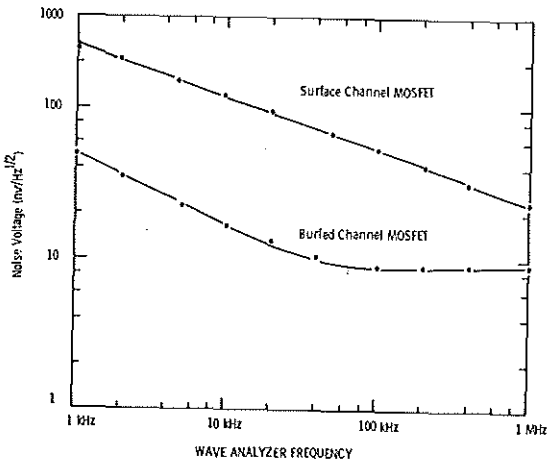

Figure 6. Comparison of noise voltage for buried and surface channel MOSFETS.

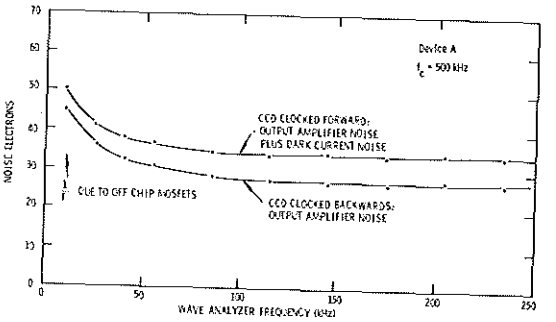

Figure 7. Output amplifier and dark current noise of device A.

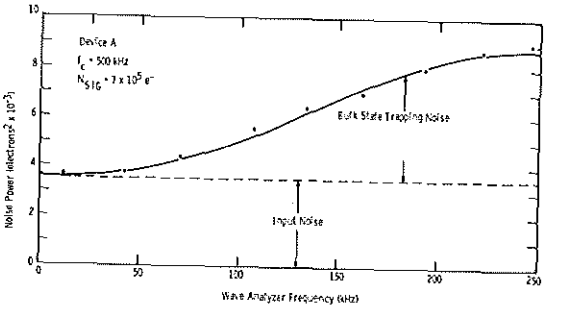

Figure 8. Measured spectral density of noise power showing peaking at high frequency due to bulk state trapping.

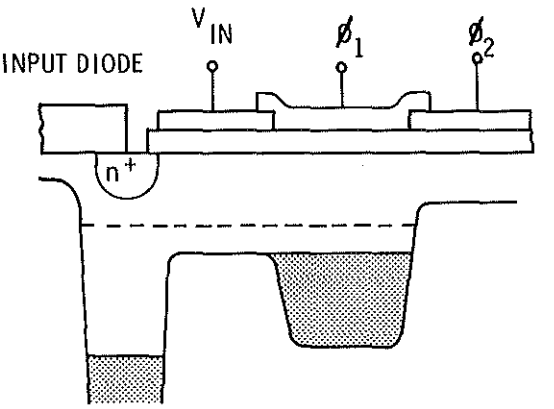

Figure 9. Input structure for the fill and spill input technique.[2,3,4]

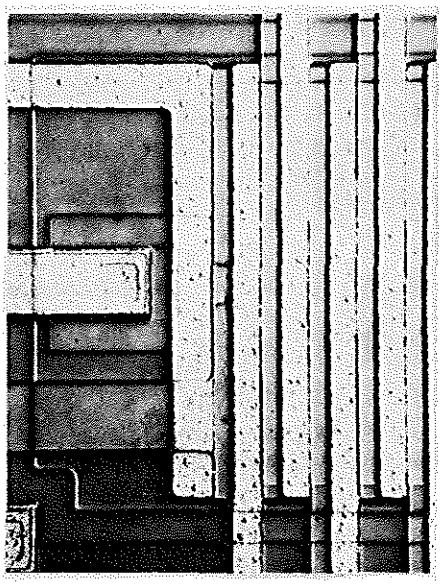

Figure 10. A photomicrograph of the low noise input structure.

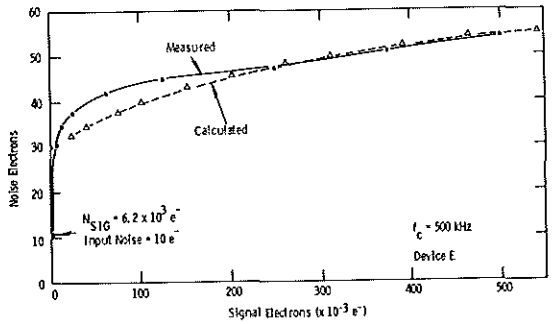

Figure 11. Input noise vs. signal level for device E.

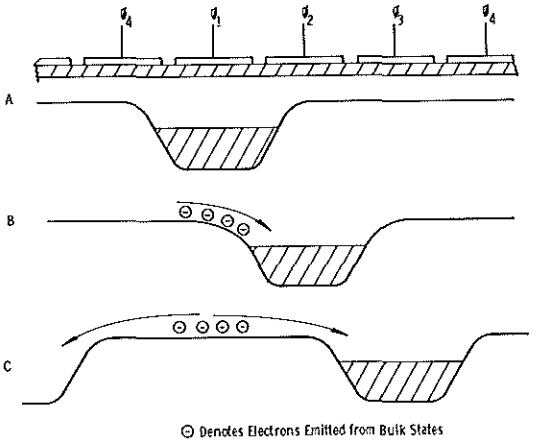

Figure 12. A simplified model for charge transfer used to estimate transfer time.

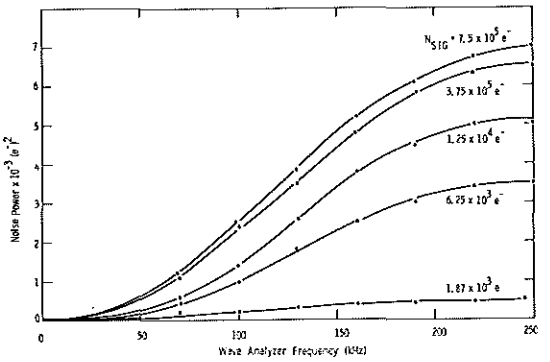

Figure 13. The spectral density of noise power due to bulk trapping as a function of signal level, N_{SIG}.

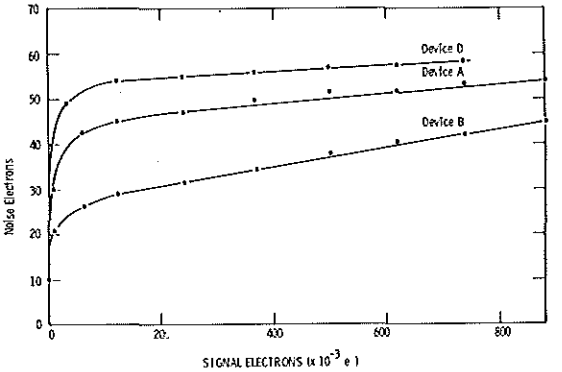

Figure 14. Measured dependence of bulk trapping noise on input charge level.

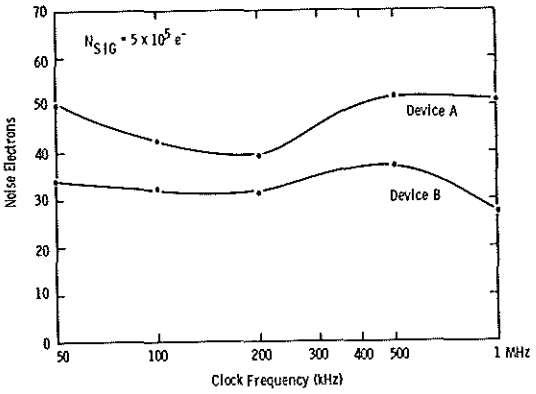

Figure 15. Measured dependence of bulk state trapping noise on CCD clocking frequency.

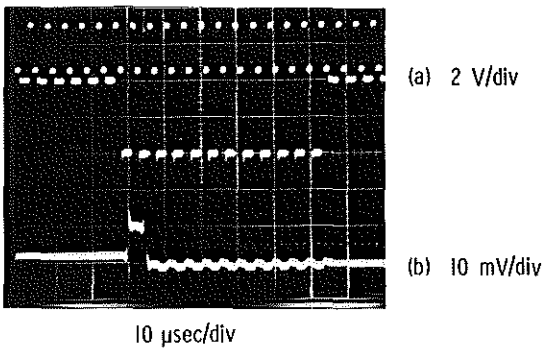

Figure 16. Measurement of transfer efficiency for CCD.
(a) Pulse Train Response
(b) Sample and Hold Output

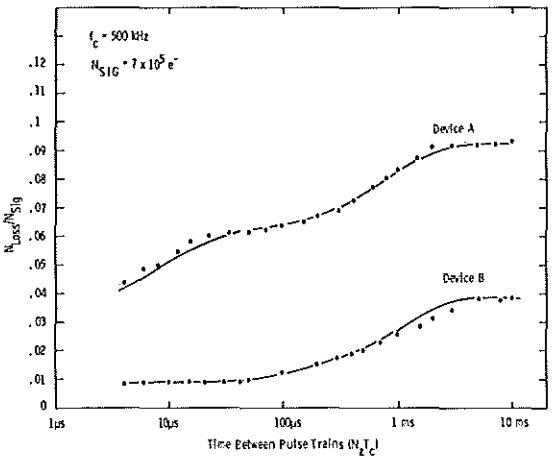

Figure 17. The double pulse measurements of loss due to bulk state trapping with the solid lines obtained by fitting to Equation 19.

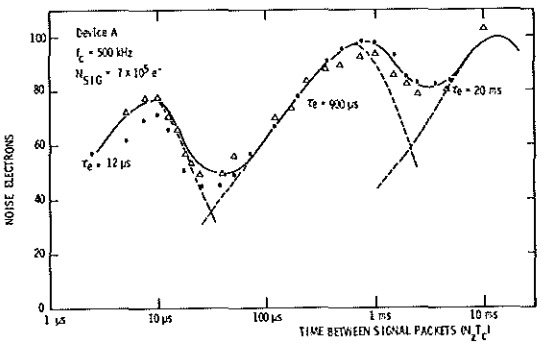

Figure 18. The double pulse measurement of noise due to bulk state trapping with the solid lines obtained by fitting to Equation 20.