RADAR VIDEO PROCESSING USING THE CCD CHIRP Z TRANSFORM

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ABSTRACT. Radar applications for CCD's appeared hopeless due to high data rate requirements until the realization that CCD's were applicable to pulse train processing instead of monopulse processing (e.g., SWD's). As a result, CCD's have found considerable applications in radar video signal processing. CCD implementation of the Chirp Z Transform is a powerful spectral analysis technique applicable to radar Doppler Processing. Successful integration of a small CCD Chirp Z Transform and associated peripheral electronics makes a small size, low power, and low cost Doppler processor for large multirange bin radar systems very attractive. The development of a 10 range bin, 17 point Doppler processor chip demonstrates the feasibility of such a processor.

INTRODUCTION

During recent years, basic radar transmitter, receiver, and antenna design has become relatively mature. Meanwhile, larger numbers of potential targets, higher resolution, and more stringent detection requirements are plaguing radar designers. As a result, more emphasis is being placed in signal processing development in recent years. The development of surface wave device pulse compression filters is a prime example. The use of digital Doppler processors based upon the FFT algorithm has similarly been a significant development within the past decade. The powerful computational equivalency of CCD transversal filters[1] in performing convolution operations as well as their small size and low power make the development of a CCD Doppler processor exciting from the aspects of size, weight, and power requirements.

The problem of detecting a target in the presence of Gaussian noise is well understood. However, the discrimination of multiple targets is less straightforward. The most common problem is the detection of a target in the presence of clutter, the radar return from land, water, trees, man-made structures, etc. In many cases, clutter returns may contain more power than desired target returns from the same range bin requiring target discrimination on the basis of a characteristic other than amplitude. This operational environment is indicated in Figure 1.

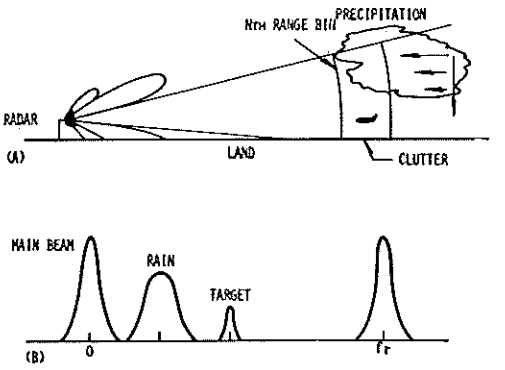


Figure 1. Relationship between (A) Radar Operating Environment and (B) Spectral Characteristics

VIDEO SPECTRAL ANALYSIS TECHNIQUES

The most common criterion for discrimination of multiple targets within a range bin is the use of Doppler frequency discrimination techniques. Since many clutter targets are stationary (or nearly so), the most common approach to clutter rejection is the delay line canceler moving target indicator (MTI) which in its simplest configuration delays a radar video return for a PRI and differences the delayed return from the succeeding new return. Since the returns from stationary targets occur at the same location in the data stream each PRI, such returns should be canceled. When considering the delay line canceler operation in the frequency domain, it may be observed to have a spectral response as indicated in Figure 2. This response has nulls near zero frequency and the PRF which attenuate the clutter returns and the aliased clutter returns.

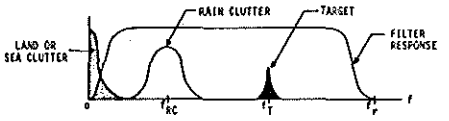


Figure 2. Canceler MTI Response

Internal clutter motion, high clutter rejection requirements, and system instabilities cause delay line cancelers to be more sophisticated than indicated above. Such cancelers have typically been implemented using A/D converters and digital delay lines. The use of analog CCD delay line cancelers[2] has been demonstrated and promises to be a less costly and smaller approach than conventional digital approaches.

As indicated in Figure 2, the delay line canceler MTI is ineffective in the discrimination of clutter returns having Doppler shifts. Rain clutter or chaff are two important examples which have Doppler shifts proportional to the local wind velocity. Internal motion within a rain cell will generally cause a spread in the spectral characteristics of the return as indicated in Figure 2. In order to discriminate against Doppler shifted clutter returns or against multiple targets within a range bin, more sophisticated spectral analysis is required.

The use of range sorting techniques followed by contiguous bandpass filter banks in each range bin is an obvious approach to frequency discrimination of targets within a range bin. This approach is generally impractical for large radars since the filter bank must be duplicated for each range bin.

Another crude frequency analysis technique is the single sideband modulation of an incoming signal with a repetitive linear FM (chirp) waveform which is then passed through a bandpass filter. The relative time of occurrence of the filter's output can be used as a measure of the incoming signal's frequency. This technique is conceptually similar to the Chirp Z Transform which can be shown to give the true power spectral density of the incoming signal.

Digital implementations of discrete (DFT) or fast (FFT) Fourier transforms have permitted the achievement of the necessary frequency resolution to inhibit the processing of Doppler shifted clutter targets. In addition to improving subclutter visibility, DFT processing provides coherent integration over N samples which ideally increases the signal-to-noise ratio by a factor of N for a signal in the presence of white noise.

While the use of DFT or FFT techniques to implement a pulse Doppler processor are well understood, such a processor is quite complex for practical multirange bin radars contributing to a significant fraction of the total cost of the system.

THE CCD CHIRP Z TRANSFORM

The powerful computational equivalency of CCD transversal filters in the solution of matrix equations, and particularly, the performance of convolution operations, has led to the observation that such a filter can provide an operational breakthrough

in performing high speed (up to 10 MHz) DFT's through use of the Chirp Z Transform (CZT). The CZT has been known for some time,[3,4] but has generally been considered a mathematical curiosity since on the order of $N \log_2 N$ computations are required, and thus, offers no simplification over a conventional FFT using digital implementations.

By starting with the classical DFT equation,

$$F_k = \sum_{n=0}^{N-1} f_n \, e^{\frac{-i2\pi nk}{N}} \qquad (1)$$

it may be shown that the DFT may be easily implemented using CCD transversal filters to perform the bulk of the required computation.[5,6] By substituting

$$-2nk = (n - k)^2 - n^2 - k^2 \qquad (2)$$

into Equation 1, the expression for the CZT is derived:

$$F_k = e^{\frac{-i\pi k^2}{N}} \sum_{n=0}^{N-1} \left(f_n \, e^{\frac{-i\pi n^2}{N}} \, e^{\frac{i\pi (n-k)^2}{N}} \right) \qquad (3)$$

This equation may be viewed as a series of operations performed with the complex linear FM, or chirp, waveform, $e^{\frac{-i\pi n^2}{N}}$. The calculation of F_k may be accomplished by (1) multiplication of the sequence f_n by a chirp waveform, (2) convolution of the new waveform with the oppositely sensed chirp waveform, and (3) a final chirp multiplication which gives the correct phase. When only the power density spectrum $|F_k|$ is desired, the final chirp multiplication may be replaced by a sum-of-the squares operation.

In order to calculate the complete spectrum (i.e., F_k for $0 \leq k \leq N-1$) in general requires 2N-1 calculations of the summation indicated in Equation 3 due to the filter loading time. The calculation of all N Fourier coefficients requires convolution of the input sequence $f_n \, e^{\frac{-i\pi n^2}{N}}$ with N values of a chirp waveform which has a total of 2N-1 values implying that the input data f_n must be blanked such that

$$f_n^* = \begin{cases} f_n & 0 \leq n \leq N-1 \\ 0 & N \leq n \leq 2N-1 \end{cases} \qquad (4)$$

in order that the undesired filter weighting coefficients do not contribute when calculating the appropriate Fourier coefficients.

Equation 3 can be more directly implemented using CCD's by substituting

$$n = k - m + N \qquad (5)$$

where m denotes the m^{th} CCD stage.

The Fourier coefficient is then

$$F_k = e^{\frac{-i\pi n^2}{N}} \sum_{m=1}^{2N-1} e^{\frac{i\pi (m-N)^2}{N}} \left[f_{k-m+N}^* \, e^{\frac{-i\pi (k-m+N)^2}{N}} \right] \qquad (6)$$

which implies convolution in a complex CCD correlator of length 2N-1. Due to the blanked nature of the input data, the chirp multiplication indicated in the bracketed term is only necessary over the range of n over which f_n was nonzero so that the input sequence f_n is required to be multiplied by

$$C_n = e^{\frac{-i\pi n^2}{N}} \qquad 0 \leq n \leq N-1 \qquad (7)$$

The CCD transversal filter tap weights are defined as

$$h_m = e^{\frac{i\pi (m-N)^2}{N}} \qquad 1 \leq m \leq 2N-1 \qquad (8)$$

The blanking of the input sequence f_n can be a problem when a continuous spectrum of a continuous signal is desired. This can be accomplished by two CZT's which have stag-

gered timing. However, the use of the continuous, or sliding, CZT[2] can be used to advantage in many such applications. Figure 3 indicates the primary differences between the exact CZT and the continuous CZT for a five point transform. The exact CZT utilizes input samples x_0 - x_4 to obtain Fourier coefficients X_0 - X_4. Input samples x_5 - x_9 are required to be blanked and a new set of Fourier coefficients are calculated from x_{10} - x_{14}. The continuous CZT calculates the first Fourier coefficient X_0 on the input samples x_0 - x_4, the second coefficient X_1 on input samples x_1 - x_5, etc. The continuous CZT is equivalent to the exact DFT in the calculation of power spectra for spectra unchanging over the time $2NT_C$ where N is the transform length and T_C is the sampling period. The continuous CZT calculates the same phase as the exact DFT for input signals periodic in N.

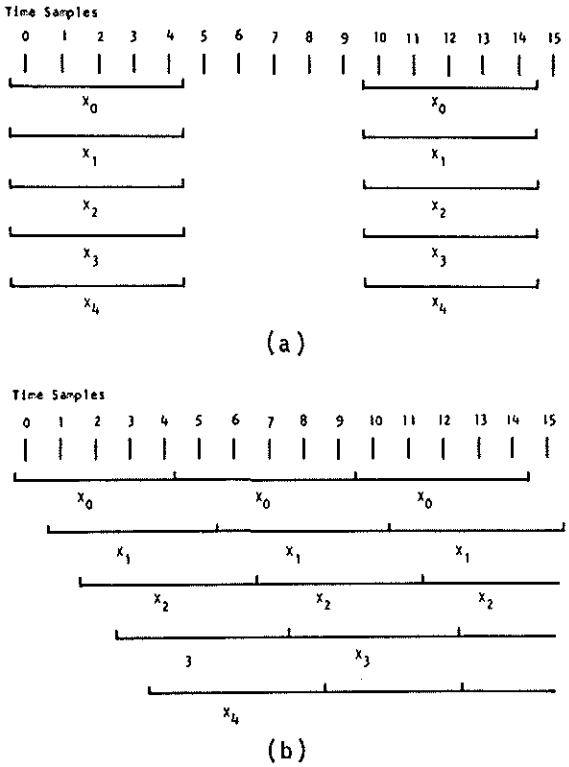


Figure 3. Comparison of the Exact CZT with the Continuous CZT

The continuous transform can be defined by the equation

$$F_k^c = \sum_{n=k}^{k+N-1} f_n \; e^{-i2\pi nk/N} \qquad (9)$$

In this case, an N point correlator is capable of generating N Fourier coefficients. By making a substitution similar to Equation 5 and a shift of the summation index, this expression can be reduced to an expression similar to Equation 6 in which chirp through zero frequency waveforms may be used. This is especially convenient for using CCD filters since it permits minimization of the Nyquist sampling rate. The input chirp waveform samples for this continuous chirp through zero case are defined by

$$C_n = e^{-i\pi(n-N/2)^2/N} \qquad 1 \leq n \leq N \qquad (10)$$

which implies Nyquist sampling at the frequency extremities.

Sidelobe reduction is a key factor in the achievement of high subclutter visibility. Apodization for reduction of sidelobes may be utilized on filter weighting coefficients for the continuous CZT, but must be accomplished on either the input chirp or signal waveforms for the exact CZT. Most apodization techniques are approximations to Dolph-Chebyschev weighting and are well documented.[7] Attendant with sidelobe reduction are correlation pulse width broadening which sacrifices frequency resolution and a decrease in processing gain. Sidelobe levels for CCD filters are ultimately limited by tap weight round-off inaccuracies, but computer simulation indicates sidelobe levels below 40 dB are achievable. Aliasing considerations are extremely important in the realization of low sidelobe levels when using the continuous CZT. Of particular importance is the generation of C_n such that

$$C_{n+N} = C_n \qquad (11)$$

in order that the phase of the product $f_n C_n$ is continuous through the folding frequency.

CCD CZT DOPPLER PROCESSOR IMPLEMENTATION

Figure 4 shows the conceptual implementation of a range-gated CZT Doppler Processor. Functionally, this processor is analogous to the FFT processor. The I and Q video signals for all range bins of given pulse return are multiplied by the properly weighted sample of the down-chirp signal as required in the first step of the CZT algorithm. Range gating may be accomplished by commutation or demultiplexing operations. Commutation is accomplished by sequentially switching the appropriate correlator into an analog data bus. Demultiplexing may be accomplished by storing video samples corresponding to M range bins in a serial in - parallel out CCD each PRI. At the completion of the PRI, the samples are simultaneously transferred out into M chirp correlators. It is seen that these chirped time samples propagate through the chirp filters at a rate of one position per PRI. Thus, one spectral sample is produced every PRI from the output of each chirp filter. That is, for a given range bin, the spectral samples emerge in sequence with N PRI's required to obtain an N-point spectrum of the input time series.

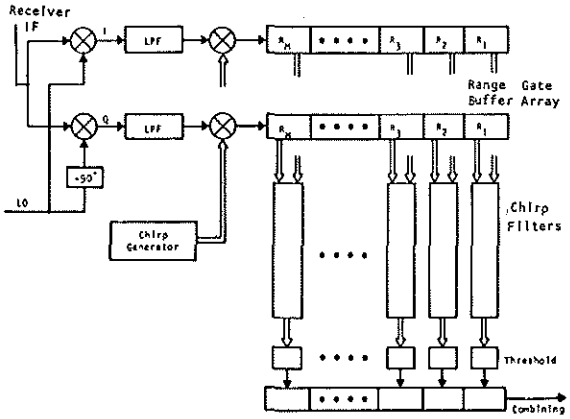


Figure 4. Range Gated Pulse Doppler Processor Utilizing the CZT

In general, all quantities in the previous CZT equations are complex. To perform complex processing in real hardware, parallel channels are implemented for the real and the imaginary components of each term. [The complex data sample f_n has already been separated into real and imaginary components by virtue of the I and Q radar video processing.] Figure 5 shows in more detail the implementation of the CZT by examining the processing for the K^{th} range bin. The range gate buffer array supplies sine and cosine components of the chirped time series at the sample rate (i.e., the PRF). Each of these components is then processed in sine and cosine filters. For example, the cosine components of the chirped series when applied to the cosine filter is performing the correlation operation:

$$\sum_{n=0}^{N-1} g(n)h(k - n), \tag{12}$$

where

$$g(n) = x_n \cos\left(\frac{\pi n^2}{N}\right),$$
$$h(k - n) = \cos\left[\frac{\pi(k - n)^2}{N}\right], \tag{13}$$

which is a component of the required correlation. This component is combined with the three other outputs as shown in the figure.

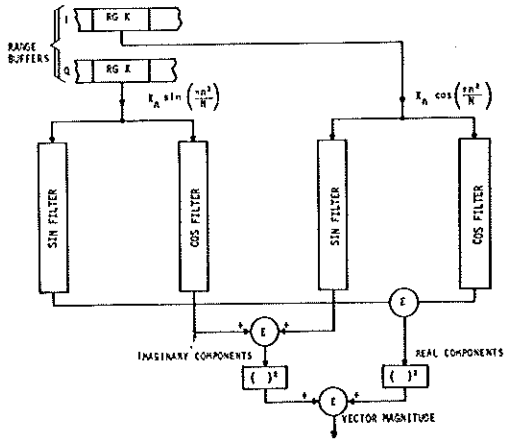


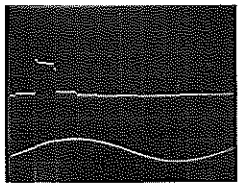
Figure 5. Filter for a Single Range Bin

In pulse Doppler radar processing, the power spectrum, rather than the complex Fourier transform, is usually the quantity of interest. Thus, the third step of the algorithm (multiplication by the second chirp) may be omitted. The I and Q channel components are finally combined in a vector magnitude algorithm. Output processing consists of thresholding, which may be adaptive or fixed (on an individual Doppler bin basis to reject clutter and detect moving targets), and Doppler bin combining.

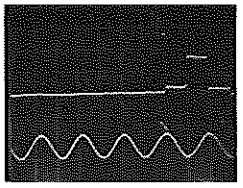
Since the number of range bins required for most radar systems varies between 50 and several thousand, a Doppler processor chip approach that can readily be expanded to accommodate any required number of range bins is desirable. This approach can best be effected by commutating the video return into a desired number of identical chips. These chips can be structured to perform the block diagram functions of Figure 4. The video return on the chip must first be sorted into appropriate range bins by a demultiplexing or commutating operation. This range-sorted video return must then be applied to in-phase (I) and quadrature (Q) matched filters whose outputs are squared and summed to eliminate an output amplitude - input phase dependence. Of significant importance in the successful integration of these functions is the ability to derive the output signal from the CCD matched filters, to perform a reasonable approximation to an analog squaring function, and to do an analog signal summation a multiplicity of times on a single chip. If such functions are not integrated on the chip, the package size quickly becomes dominated by the large pinout requirement. The small system size advantage of a CCD Doppler processor is not as obvious due to the requirement of additional circuitry to perform these processing functions.

The first attempt at designing such a chip was a single channel, four-range bin chip comprised of a sine and cosine filter pair for each range bin. A single on-chip differential current integrator (DCI) complete with dual MOS integrating capacitors was placed on this bar. Two filter chips (I and Q channels) as well as sixteen DCI chips were combined to construct a four range bin version of the system shown in Figures 4 and 5. Bipolar operational amps and analog multiplers were utilized to accomplish the majority of the remaining functions. The breadboard was operated assuming a PRF of 1 kHz and a transmitted pulse width of 10 μs.

A very elaborate SSB generation scheme was utilized to simulate I and Q baseband radar video signals over the frequency range from 30 Hz to 800 Hz which was determined by the sideband filter characteristics. The breadboard was capable of performing spectral analysis over the frequency range from 0 to 1 kHz with resolution of 58.8 Hz. Figure 6 indicates the response of the breadboard to sinusoids of 100 and 500 Hz. Figure 7 indicates the simultaneous response of the four range bins to a continuous sinusoid. Sampling the I and Q sinusoids during the appropriate range bin window permits the simultaneous response of Figure 8 to be achieved.



(a)



(b)

Figure 6. Single Range Bin Response of Doppler Processor Breadboard to (a) 100 Hz Sinusoid and (b) 500 Hz Sinusoid

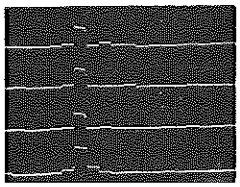


Figure 7. Simultaneous Response of Four Range Bins to a Continuous Sinusoidal Input Signal

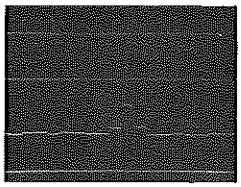
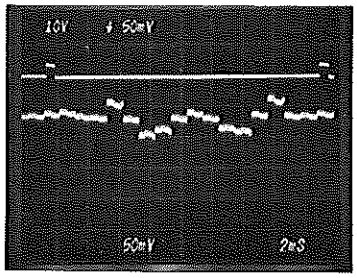


Figure 8. Simultaneous Response of Four Range Bins to a Sampled Sinusoidal Input Signal

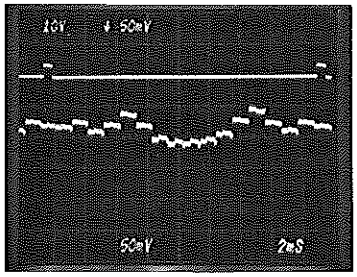
A second bar has been fabricated in an attempt to develop a modular Doppler processor chip which may be cascaded to achieve any desired number of range bins of processing. This chip contains complete I and Q processing of 17 point CZT's for 10 range bins. This bar has the dimensions of 275 mils by 280 mils and contain the following:

- 2 - Range Commutating Shift Registers
- 40 - 17 Point Chirp Filters
- 20 - Differential Current Integrators
- 20 - Sample and Hold Circuits
- 20 - Differential Amplifiers
- 20 - Transconductance Multipliers

This bar is perhaps the most ambitious attempt made to date in the integration of perihperal CCD electronic circuitry. Chip operation has been achieved as indicated in Figure 9 which shows the impulse response of two of the filters as well as an overall correlation response.



(a)



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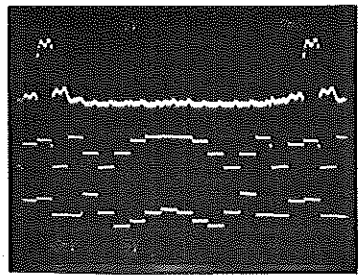

(c)

Figure 9. Impulse Responses for

(a) $-\sin \frac{\pi\left(n - \frac{N}{2}\right)^2}{N}$ and

(b) $-\cos \frac{\pi\left(n - \frac{N}{2}\right)^2}{N}$ filters and

(c) Correlation Response for 10 Range Bin, 17 Point Doppler Processor Chip

CONCLUSION

The development of the 10 range bin Doppler processor bar has demonstrated the feasibility of integrating short CCD transversal filters and the required peripheral electronics on the CCD chip to accomplish sophisticated functions such as multirange bin Doppler processing. Such integration is the key to an economical Doppler processor chip which can serve as a building block for large multirange bin systems. Improvements in circuit performance and minimization of chip size (or extension to longer transforms) are expected with improvements in peripheral circuitry technology.

ACKNOWLEDGMENT

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