DISCRETE-TIME ANALOG SIGNAL PROCESSING DEVICES EMPLOYING A PARALLEL ARCHITECTURE

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ABSTRACT. Analog signal processing devices which use a parallel rather than a serial architecture will be described. These devices perform the functions of delay, time-base expansion/compression and binary/analog correlation. The fundamental operating principles as well as the unique advantages of a parallel architecture such as

1. Independent input-output,
2. The ability to do permuted as well as sequential sampling,
3. The realization of long retention time (exceeding 5 seconds at 25°C), and
4. The ability to read out non-destructively,

will be discussed.

Key features of each device as well as performance tradeoffs inherent in differing device designs will be discussed. Device characteristics and performance such as delay-bandwidth product, signal to noise, linearity, etc., will also be discussed.

The variety of applications for these devices is extremely broad. It ranges from low-frequency geophysical or medical instrumentation to high-frequency communications and radar. Specific applications which will be discussed include adaptive transversal filters, binary and p-n sequence correlators, transient recorders, and time-base correctors.

Sampled-data signal-processing devices for producing delay, frequency scale change, time-base expansion or compression, etc., may be devised using either parallel or serial storage architecture. The parallel architecture has unique advantages in flexibility, linearity, and speed which complement rather than compete with those of charge-transfer devices; each has its field of application. Of necessity comparisons with CTD will be made. Figure 1 lists in tabular form some of the salient features to be discussed. Some of these features are not necessarily unique to the parallel-storage architecture, but parallel storage in many ways provides better means for exploiting the desired features.

Figure 2 is an updated version of a curve shown by Buss and Bailey about one and one-half years ago.[1] This updated version shows extension of the operating region into both a higher sampling-rate area and a longer time-delay area; both extensions are possible because of the parallel approach with its feature of independent input and output. Note that the independent control of input and output

permit operation within the area of the box above the $T_dW = 10^3$ line whereas the serial configuration only permits operation below the line. The parallel architecture thus allows considerable extension to permissible areas of operation.

To describe the devices and their features, let us take several concrete examples, each illustrating particular features or combinations. Figure 3 shows the simplified equivalent circuit for one fairly early example of the parallel-storage architecture. This particular device, called a Serial Analog Memory (SAM) because of its independence of input and output, has 64 memory cells. Two independent shift registers, one controlling the input and the second the output, sequentially activate elements from the two series of multiplex switches. The first register and its associated multiplexer sequentially time-samples an analog input signal, storing each of the samples on discrete capacitive storage cells. The second register and its associated multiplexer sequentially interrogate the memory elements, connecting successive stored values to the output line.

This device has a sampling-rate range from 5KHz to 12MHz and a greater than 55 db dynamic range. These devices have been successfully used in a number of applications ranging from simple time delay to time-base correction of video signals as obtained from video tape recorders.

Figure 4 shows a different example of the parallel architecture in the form of a 100-element Serial Analog Delay (SAD). Included in the figure is the peripheral control required. The device is similar to that of Figure 3 except that it does not have the independence of control of the input and output registers of Figure 3. Each of the delay channels in Figure 4 has 50 storage elements so arranged that each storage site is read out just prior to the receipt of a new sample, thus giving maximum delay. The two delay channels are normally processed in staggered fashion, thus giving a multiplexed 100-element delay unit. Additional delay or higher effective sampling rate can be achieved by further multiplexing additional packages. Note that this multiplexing is free from problems of ghosting - there is no tailing of the signal in one packet into adjacent packets; each sample is and remains discrete and unique. Improvements in processing have permitted a dynamic range exceeding 66 db with permissible input levels up to a peak value of approximately 5 volts.

Figure 5 shows the simplified equivalent circuit of a Serial Analog Memory which has buffered readout of the memory. Along with the independent readin and readout capability, the buffering permits nondestructive readout as well as the interrogation of more than one memory cell at a time. A binary sequence entered into the output shift register can thus be correlated with the signal (analog or binary as desired) entered into the memory input. Figure 6 shows the correlation function of two binary sequences derived from the same source, illustrating the functioning of the correlator.

The ability of devices with buffered independent readin and readout to provide correlation processing has proved so important that special devices have been designed to perform more complex processing. Figure 7 illustrates the simplified circuit of such a device. This device, referred to as a Serial Analog Processor (SAP), in its simplest form is similar to the memory devices illustrated previously except that the output control is by means of a static shift register whose flip-flop elements control dual output buffer amplifiers. Each memory cell is connected to two buffers, one to give positive or unit weighting, the other negative or zero weighting. Further, the static shift register may have its data circulated in either direction. Buffer outputs are in the form of currents which are collected by the positive- or negative-weight output lines. Thus, binary correlation may easily be obtained as above. If the circulation is reversed, convolution may be obtained.

The above devices are limited to a zero or one for each weight value. However, it is possible to parallel circuits such as

the above to obtain four-bit or greater quantization of each weight. Such a combination is not limited to binary signals; it permits discrete time correlation or convolution of two analog signals (one of which is converted to a binary quantized form). But correlation is the foundation for discrete-time filters, so that highly sophisticated discrete-time filters may be simply, easily and economically built. The manifold advantages of discrete-time processing are combined with the speed and convenience of analog processing to give an extremely flexible, highly precise key element for all forms of transversal and recursive filters, as well as being applicable to the more obvious correlation and convolution processing. A schematic arrangement is illustrated in Figure 8.

SAP devices have been made with 16, 32, 64 and 128 cells (or filter taps); four such devices can then give any of 16 possible positive weights (or 16 negative weights) to each tap.

Two other developments permitted by the parallel architecture are in late stages of development. The first takes advantage of recent technology to obtain very low residual thermal pair excitation (leakage) and hence very long memory retention times - of the order of ten seconds. Such devices have all the desirable features of the family such as high sampling-rate capability, wide dynamic range, good linearity, etc., with the added capability to operate at very low clock frequencies to give long delay, etc. Figure 9 illustrates performance of this device. The lower trace shows the input signal (with an abrupt frequency change). The upper trace shows the output signal with a delay of approximately 9 seconds. In 35 seconds, stored amplitude decayed to approximately 80% of initial amplitude.

The second development capitalizes further on the parallel-storage architecture to permit decoded random selection of the input storage sequence. Thus arbitrary time-slot selection of filter-tap elements is possible. A filter or processor of new and unique characteristics thus becomes possible.

In summary, the parallel architecture has features complementary to those of charge-transfer devices. Certain of those features such as convolution processing and decoded input-sequence selection are possible only with the parallel architecture; others are more easily and effectively implemented in the parallel form, for example the multi-bit weighting of a multi-tap device. Finally, the physical processing is such that functions such as switching and storage are more easily optimized in the parallel architecture.

REFERENCES

1 Dennis D. Buss and Walter H. Bailey: "Applications of Charge Transfer Devices to Analog Signal Processing"; IEEE Intercon 74.

FEATURES OF PARALLEL PROCESSING ARCHITECTURE

1. INDEPENDENT INPUT AND OUTPUT
   a. TIME SCALE CHANGES
   b. CORRELATION AND CONVOLUTION PROCESSING POSSIBLE
2. POSSIBILITY OF NONDESTRUCTIVE READOUT
   a. REPEATED READOUT
   b. ISOLATION
3. REALIZATION OF VERY LONG RETENTION TIMES
4. THE ABILITY TO PERFORM PERMUTED AS WELL AS SEQUENTIAL SAMPLING
5. HIGH SAMPLING RATE WITHOUT SUFFERING TRANSFER INEFFICIENCY
6. LINEARITY AND WIDE DYNAMIC RANGE
7. PERFORMANCE DIRECTLY RELATED TO CELL AREA

Figure 1. Advantages Available with a Parallel Processing Approach

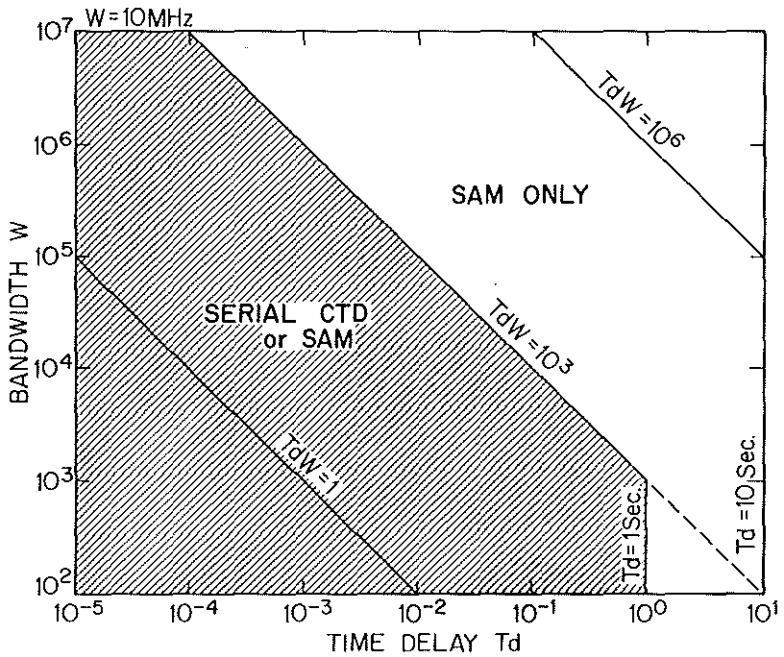

Figure 2. Useful Time Delay vs. Bandwidth

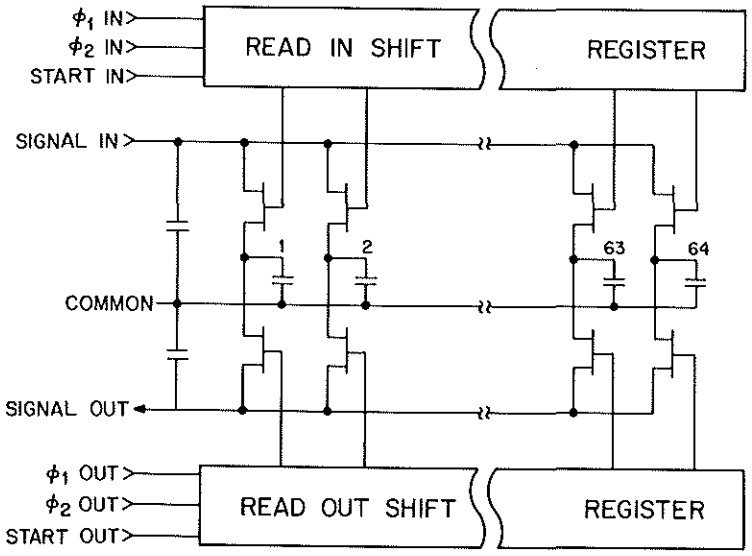

Figure 3. Parallel-storage Serial Analog Memory

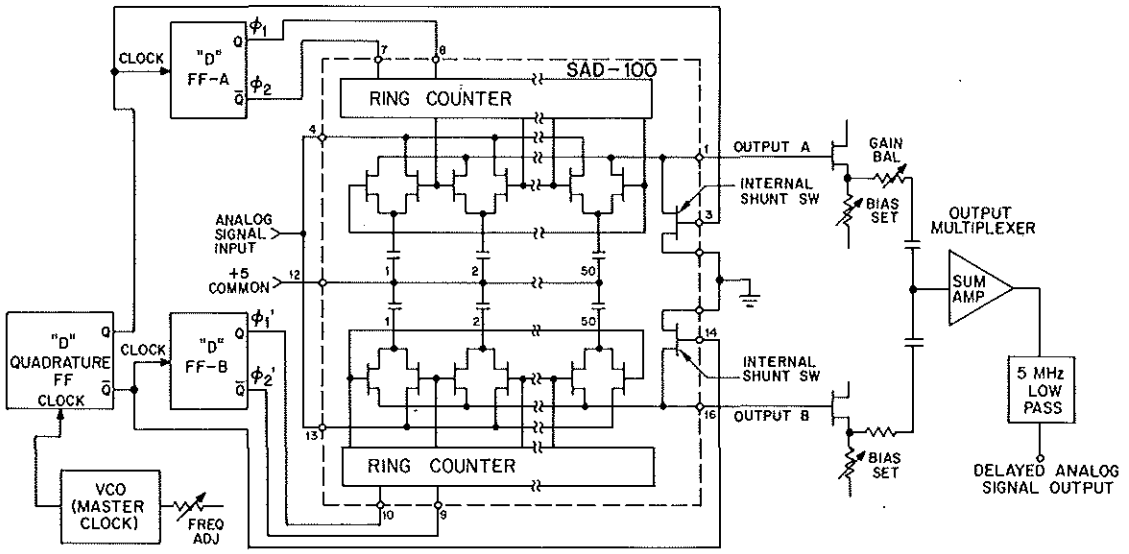

Figure 4. Duplex Parallel-Storage Serial Analog Delay

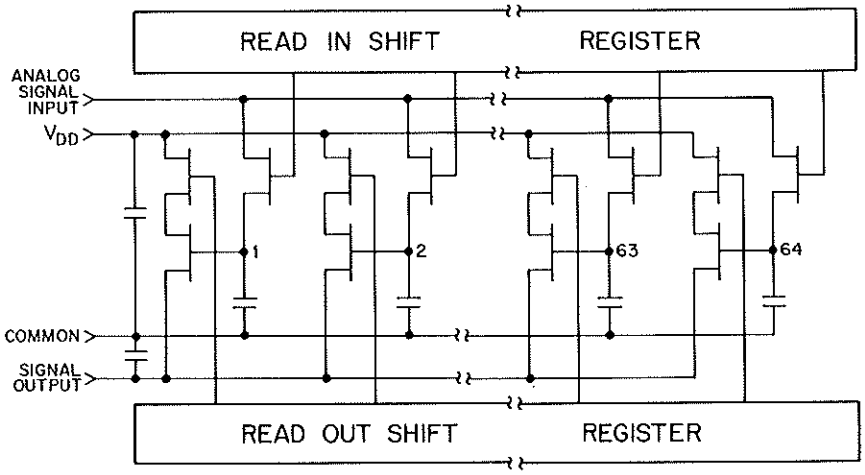

Figure 5. Buffered Parallel-storage Serial Analog Memory

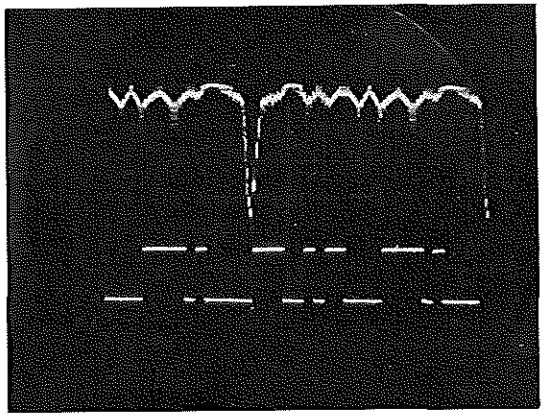

Figure 6. Correlation Oscillogram Obtained for Two Binary Sequences Using the Buffered Serial Analog Memory of Figure 5.

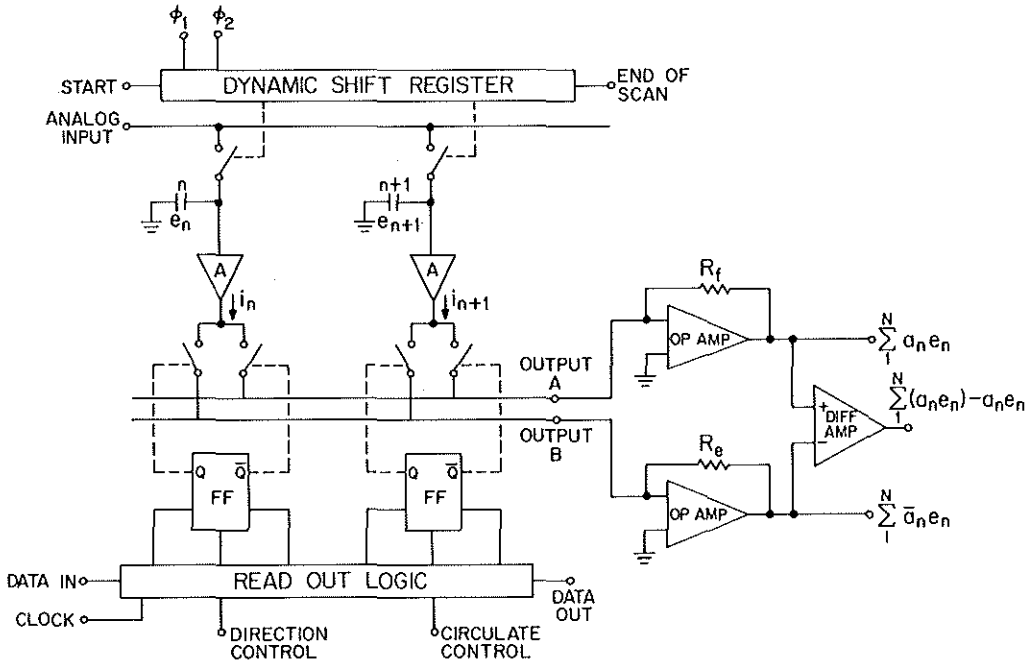

Figure 7. A More General Serial Analog Processor

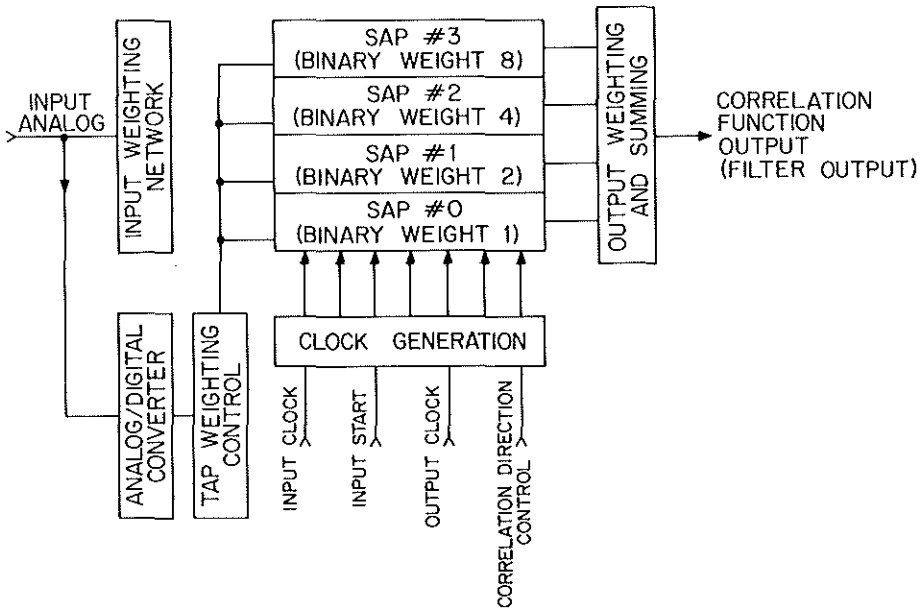

Figure 8. Schematic Diagram for a 4-bit Serial Analog Processor

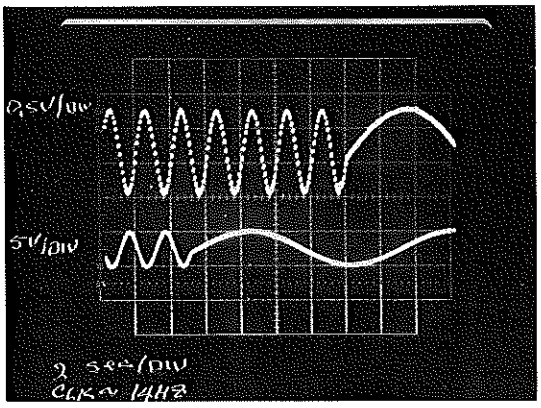

Figure 9. Retention Characteristics of a Long-retention SAM