SIGNAL PROCESSING CAPABILITIES OF A 100 x 100 CCD ARRAY

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ABSTRACT A prototype camera and signal processing unit has been built using three identical 100 x 100 interline transfer CCD arrays. Each CCD organization is in a SPS (series, parallel, series) format. A unique electrical interface allows the output to be compatible with standard EIA RS170 format monitors and recorders operating at 30 television frames per second. The system operation features both frame-to-frame subtraction and long-term recirculation of stored data. Details of implementation are presented along with suggested areas of application, particularly as a moving target indicator.

INTRODUCTION

Efficient analog signal processing in charge coupled devices is predicated upon the existence of compatible CCDs with electrical input capabilities for temporary storage and delay of the live signal. The number and variety of commercially available CCDs, especially those with electrical input capabilities, are still quite limited. Exclusion of those CCDs intended for digital applications further limits the number of devices available. This paper presents design experience with one commercially available device which is useful for both imaging and analog signal processing: Fairchild's CCD201. The use of interline transfer devices, such as the 201, necessitates special signal handling techniques.

CCD ORGANIZATION AND STRUCTURE

The CCD201 is a 2-phase, 10,000-element self-scanning image sensor, using buried channels with ion-implanted barriers. The active light sensitive portion of each element is 1.2 mils horizontal by 0.8 mils vertical. To allow for interline analog shift registers, the elements are center spaced at 1.2 mils vertical by 1.6 mils horizontal. Thus, 50 percent of the chip area is photosensitive and a 4 X 3 image aspect ratio is provided. One-hundred columns of 2-phase vertical analog shift registers are inter-digitated in the photosensor array. A 102-element, 2-phase horizontal analog shift register permits clocking of successive horizontal lines to an output detector/preamplifier which is balanced with a compensation output amplifier.

Additionally, the CCD201 includes a 100-element, 2-phase analog input shift register which, when properly clocked, will accept electrical signals through an input diode on the device. The actual input function involves applying a signal-modulated DC level to the input diode and gating the signal in by clocking the input gate at the proper time within the horizontal cycle. A 2-phase horizontal input clock is incorporated to shift charge through the register. The input register includes an output drain to prevent charge build-up in case of overclocking.

FULL FRAME MOVING TARGET INDICATOR (MTI) SYSTEM

Figure 1 shows the functional blocks of a full-frame MTI system using an interline transfer CCD imager and two matching CCD analog shift registers. Generalizing from the specific case of the 100 x 100 array discussed earlier, the CCD array is assumed to be composed of "N" rows by "M" columns of photosensitive cells. Readout, in the usual interline transfer manner, is accomplished by shifting

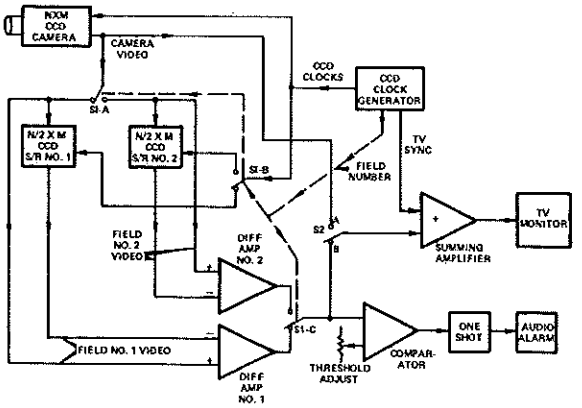


Figure 1. CCD MTI Block Diagram

alternate rows of photosite charge accumulations into the adjacent vertical shift-registers. Discrete charges are then clocked through the shift register array to the output. This inter-digitated format, necessary to give the camera its interlace feature, reduces the effective size of the shift register array to N/2 x M. Although this is generally of little importance in imaging systems, it directly impacts the scheme for using identical interline CCDs as shift registers. The effective storage capability has been reduced by 50 percent from that of the imager.

The CCD clock generator section of Figure 1 produces horizontal and vertical clock signals for the CCD. In addition, TV sync pulses and a signal referred to as "field number," which changes states on alternate fields, are generated. The system operation proceeds by initially assuming both shift-registers (S/R) are empty and the field number is such that information in field #1 is being read out of the camera. Switches S1-A and S1-B are connected to S/R #1 so that camera video is input to this device. At the end of field #1, the information stored in S/R #1 is identical, on a cell-by-cell basis, with that transferred out of the imager's shift-register. Once the field transfer has finished, the field number signal changes state, causing S1-A and S1-B to be connected to S/R #2. This second memory is now loaded with field #2 information. It is important to realize that the information stored in one shift-register remains static while the other is being loaded and read out. After field #2 is loaded and the field number changes state again, field #1 video is again read out from the camera. Simultaneously, S/R #1 video is read out and the "old" and "new" field #1 video is subtracted in differential amplifier #1. This subtraction occurs on a cell-by-cell basis in real time with the "new" field #1 video.

If the amount of charge collected on any individual pixel of the imaging CCD has changed from one frame to the next, there will be an output from differential amplifier #1 when the cell is simultaneously clocked out of the two devices. Otherwise, the amplifier has zero output throughout the entire field. An identical subtraction function is performed by differential amplifier #2 and the shift register #2 during the alternate field of video.

If S1-C is alternately switched between the two amplifiers, the wiper of S1-C will contain one entire frame of MTI video, which can be used in several ways, two of which are shown in Figure 1. With single-pole, double-throw switch S-2 in position B, TV sync pulses are added to the MTI video for display on a standard television monitor. Motion in any portion of the scene will be displayed, while all stationary scene components will cancel on a cell-by-cell basis with the stored field. Therefore, not only the presence of motion, but the location of the motion is derived.

The second (though less sophisticated) output which could be used in conjunction with, or in place of, the TV system is also shown. The MTI video is compared to a reference voltage and, when threshold is exceeded, a one-shot multi-vibrator is triggered to sound an audio alarm for some time period. While the TV compatible mode limits the system to standard 30 frame/second comparison times, the audio alarm could be used at frame rates from three to three hundred frames per second, allowing greater system versatility.

The modular design of the system allows considerable flexibility. Use of only one shift register and one differential amplifier degrades vertical resolution by 50 percent. For some applications where resolution is of secondary importance, this may be a desirable trade. Switch S_2 placed in position A, equivalent to a removal of all memory functions, returns the system to a normal, camera

only, mode capable of driving a standard monitor. The system in this configuration requires less than 20 square inches of breadboard circuitry for operation and easily fits in a 2 x 3 x 5 inch package.

This approach to motion detection has several advantages over others, the most important of which is exact registration. Since the imager and shift registers are operated from a common clock, there is no chance of improper timing causing imperfect subtraction. Also, this is the only feasible method of obtaining a true analog delay of 1/30 second. The alternative would be a complex and costly pseudo-analog approach using A/D and D/A converters with large numbers of digital shift-registers. Added to this is the inherent low power and small volume characteristics of CCDs and the low-light level capability of CCD imagers.

FULL FRAME RECIRCULATING MEMORY

Figure 2 represents the basic elements of a full-frame recirculating memory using the same interline transfer CCD imager and matching CCD analog shift resisters. Its operation is related to the state of the field number signal from the clock generator which, again, multiplexes the two CCDs on alternate fields. As before, the CCD clock generator produces all clock signals for the CCD and TV sync pulses.

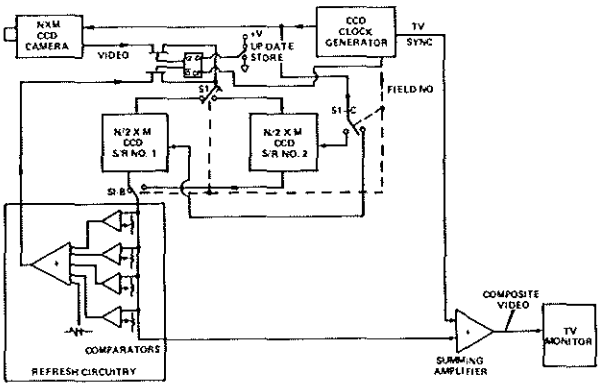


Figure 2. Recirculating Memory

The operation of the system begins when the UPDATE/STORE switch is placed in the UPDATE position. This allows the succeeding frames of video to be loaded into S/R #1 on the first field and S/R #2 on the second field. Since the CCD clocks are also switched on alternate fields, via contact S1-C, the video read into each CCD is stored for one field before being read out. Multiplexing of these outputs through switch S1-B provides exactly a one-frame delay between video being readout of the camera and that being displayed on the monitor.

Continuous recirculation of a given frame of data is initiated by returning the UPDATE/STORE switch to the STORE position. The D flip-flop signals the end of a complete frame of video stored in the two CCDs. Camera video is then disconnected from the shift register inputs and replaced with the output of the refresh circuitry. As shown, this circuit is composed of a group of comparators and a summing amplifier. The comparator thresholds are set to quantize analog outputs into several (five in this case) levels. For example, if the thresholds are set at 1, 2, 3, and 4 volts and the fixed offset into the summing amp is set at 0.5 volt, then the transfer function of the refresh circuitry would be as shown in Figure 3.

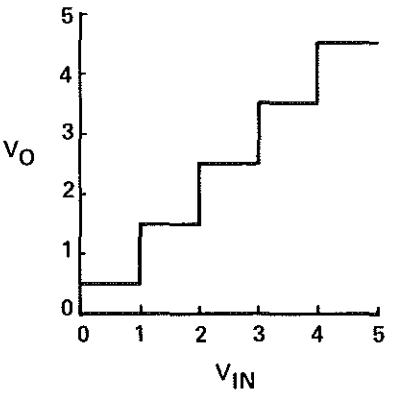


Figure 3. Transfer Function of Refresh Circuitry

The requirement for the refresh circuitry is a result of the finite transfer efficiency of the CCD as well as noise considerations. As an example, Fairchild's 100 x 100 element CCD201 with a transfer efficiency of 0.9995 will displace 50 percent of its charge after about 1380 shifts, or 9.2 cycles through the device. For a 30 frame per second system, this corresponds to a hold time of less than 1/3 second. In practice, dark current accumulation in the CCD and random noise associated with the input and output mechanisms further degrade the

signal. Addition of the refresh circuitry to the feedback loop corrects signal degradations of up to $\pm$ 1/2 volt (in this example) before the signal is fed back into the CCD.

By routing the multiplexed CCD outputs to the summing amplifier and/hence, the monitor, an image having perfect registration and five quantized grey shades can be continuously displayed. Obviously, there is a limit to the number of comparators that can be used effectively. Each quantized bin must be sufficiently wide to correct for degradations due to transfer inefficiencies and noise variations. A thermo-electric cooler to lower the operating temperature of the memory CCD would be expected to provide additional grey shade storage capability.

PROTOTYPE OPERATION

A modified version of the system described in the previous two sections was built for laboratory tests and evaluation. The principal change involved using only one CCD for each function. Therefore, both MTI and the recirculating memory functions are performed on a field, rather than a frame, basis. The entire system was constructed on four 4 x 6 inch circuit boards plus a 2 x 3 x 5 inch camera housing. Three Fairchild CCD201 devices are used.

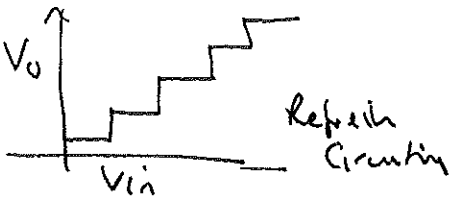
Figure 4 shows the logic circuitry incorporated in the system. Except for a few modifications, it is identical to the circuit given in the CCD201 data sheet. An oscillator with a frequency of 3.6 MHz is used as the clock for U2 and U3, which form the horizontal counting chain by dividing the oscillator by 224. Since the 1.8 MHz horizontal clock ϕ_H is derived by dividing the oscillator by 2, U3's carry output occurs each 112 horizontal clock pulses, corresponding to one horizontal line. This output is 7 ϕ_H periods wide and is used for horizontal blanking. The remaining 105 periods are used to clock the output register of the CCD. ϕ_R is active during the first quarter of ϕ_H, while ϕ_S occurs during the last quarter.

The vertical counting chain consists of U4 and U5. With single pole, double throw switch S1 in position A as shown, U8 and the associated 3-input AND gate are not involved in the active circuitry and the vertical clock is at the line rate. Fifty-one lines are counted before the load command at Q2 of U5 is generated. This command, vertical blanking #1, exists for one line. U6 is loaded at the same time as the vertical counting chain. This interrupts the clock to U4 for 13 lines, forming vertical blanking #2. Total blanking period is the sum of vertical blanking #1 and #2, or 14 lines. When added to the 51 active lines, a total field length of 65 lines results.

U7 is a multiplexer designed to produce ϕ_p and ϕ_V. ϕ_p goes low for the first half of vertical blanking #1 and then low for the whole of vertical blanking #1 on the alternate field. ϕ_V is basically horizontal blanking during the active field and high or low during vertical blanking on alternate fields. The relationship between ϕ_p and ϕ_V on the negative transition of ϕ_p determines which set of elements of the sensor is transferred into the vertical transport register.

Since each horizontal line requires 112 ϕ_H cycles, the line rate is 1.8 MHz $\div$ 112 $\cong$ 16 KHz, which is sufficiently close to 15.75 KHz (standard TV line rate) to be used with 525 line monitors. As mentioned before, a field is composed of 65 lines, resulting in a frame rate of 16 KHz $\div$ 130 = 123 frames per second. Forcing a 30 frame per second monitor to sync to this increased rate requires paralleling the resistor in the wiper of the vertical hold control with a smaller resistor, typically 100Ω. Of course, adjustment of the vertical height control is also necessary.

Operation of the 100 x 100 element CCD at the CCTV standard of 30 frame-per-second rate, while maintaining the 15,750 Hz line time, can be accomplished by using U8 to divide U3's output by 4. With double pole, double throw switch S_1 in position B, U8's output is used to clock the vertical counting chain, increasing the field time by a factor of four. Since horizontal sync pulses to the monitor are not divided, the overall result is that only one vertical shift of ϕ_V in the CCD occurs for each four lines displayed on the monitor. The monitor will now run at 30 frames per second making it compatible with the requirements of EIA RS-170 standards. The CCD imager's inte-



gration time, being increased four times, allows operation at lower light levels ($\sim$ 2 f-stops).

The clocks, as generated in Figure 4, are used to drive both imager and storage CCDs; Figure 5 indicates the arrangement for driving the imager. Each of the T^2L level clocks needed is amplified and level shifted by one of the clock driver circuits of Figure 6. The normal state of the clock waveform at the CCD determines which circuit is used. These drivers offer the high speed operation necessary to clock the CCD at TV compatible rates and the low power dissipation desirable for a minimum system heat generation. Since ϕ_{V1} and ϕ_{V2} require identical voltage levels, some component reduction is accomplished by sharing power supply transistors (Q1 and Q3) between these two complementary signals. The same is true of ϕ_{H1} and ϕ_{H2}.

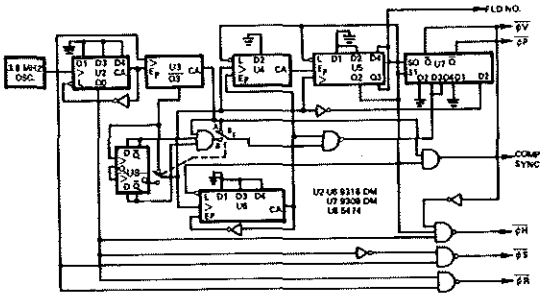


Figure 4. CCD Clock Generator

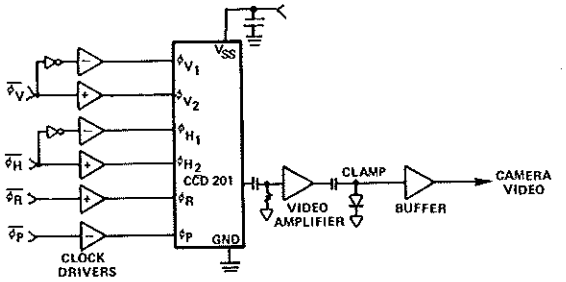


Figure 5. CCD201 Camera

The output signal level of about 75 mV is capacitively coupled to remove the DC offset. The signal is then amplified and clamped to a DC level near ground potential. A unity gain buffer offers a low output impedance for transmitting the camera video to three other functional blocks of Figures 7, 8 and 9.

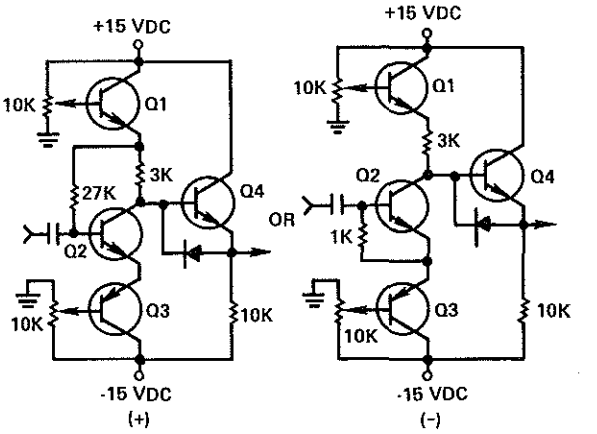


Figure 6. Clock Driver Circuits

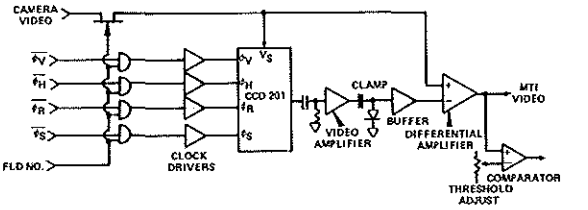


Figure 7. Single-Field MTI

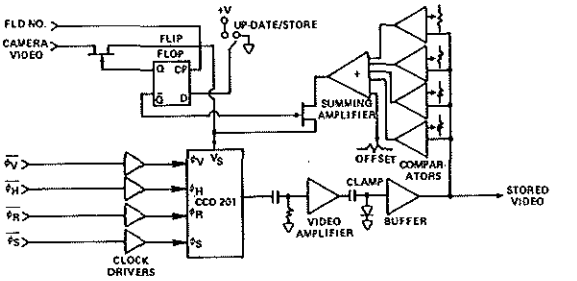


Figure 8. Single-Field Storage

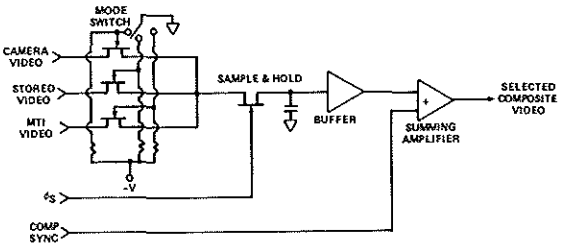


Figure 9. Video Processing

The single-field MTI circuit is shown in Figure 7. Here, a single CCD201 array is used as an analog shift register. It is worth noting that the device, when operated in this mode, is interfaced with peripheral circuitry in much the same manner as the imager. Both modes of operation require vertical, horizontal, and reset clocks. A photogate clock is not required for the memory mode since the photosites are not addressed. However, additional clocks in the form of input horizontal ($\phi_{H\ IN}$) and sampling (ϕ_S) are required. Figure 10 is a timing diagram showing the relationships between horizontal clocks and the sampling clock. Input horizontal clocks (ϕ_{H1-IN} and ϕ_{H2-IN}) are held low during the vertical transfer. Otherwise, the input horizontal clocks are identical to the output clocks.

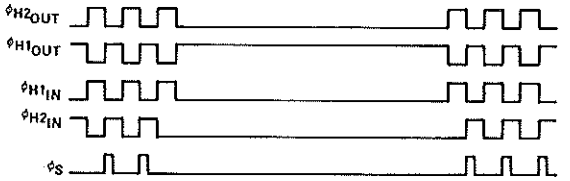


Figure 10. CCD201 Shift Register Waveforms

Although the waveforms of Figure 10 are sufficient for producing a delayed field of video, the problem of registration must be dealt with before the device can be used for element-by-element comparison with camera video. The output register on the CCD201 requires 102 horizontal clocks to empty completely, while the input register requires 100 clocks to fill completely. The simplest solution to this registration problem, and the one that leads to the greatest useful scene area, is to clock all horizontal registers 102 times. The input register will dump the overfill, resulting in each element holding the charge associated with the equivalent element on the sensor. For the prototype system under discussion, the sensor was clocked 105 times (as previously described), and the shift register array was clocked 102 times by inhibiting the first three clock pulses from the clock generator. Although this approach does give perfect horizontal registration, the last three elements of each line from the shift register contain no information. Vertical registration must also be considered. The 51 vertical shifts per field derived from the clock generator board is exactly the number required to transfer data through the CCD 201 shift register.

Figure 7 showed that the clocks are applied to the shift register on alternate fields only. This provides same field comparison on odd numbered fields (for instance), and no MTI output video on even fields. The resulting resolution is 50 x 100 elements. Background suppression to 2 percent of white level has been demonstrated with the prototype system over the entire dynamic range of the imager. This type of performance is achieved only after careful clock level and amplifier adjustments. In the system being discussed, a comparator with its threshold set at 5 percent of white level was added to the differential amplifier's output. This completely eliminated stationary components of the viewed area from the displayed video.

The single-field storage (Figure 8) is similar to the full-frame storage discussed previously, except that only one CCD is employed, removing the requirement for the multiplexing circuitry. The prototype system uses from two to four comparators in the refresh circuitry, giving up to five levels of recirculating storage. Again, registration is important since each cycle through the CCD must result in the same element-time relationship. The same clocks are used in this scheme as those in the single field MTI. False alarms, defined for this discussion as a charge degradation of sufficient magnitude to cause the CCD's output to be quantized incorrectly in the refresh circuit, are very much a function of the number of comparators and their threshold settings. With two properly adjusted comparators, the false alarm rate (FAR) is virtually zero. Increasing this number to four comparators greatly increases the FAR for the first few recirculation cycles, but it then settles to about one per minute. This transient phenomenon can be attributed partly to charge-spreading in the CCD for large contrast changes between adjacent cells, and partly to electronic transients when the input of the CCD is switched between camera video and video from the refresh circuit.

Figure 9 shows the essential elements of the video processing electronics used in

the prototype system. Here, one of the three available videos (direct camera, stored, or MTI) is chosen for display. Due to the format of the CCD video output (see the CCD201 data sheet), a sample-and-hold is required to remove clock components. Finally, composite sync is added to the video in a summing amplifier before routing the composite video to the monitor.

SUMMARY AND CONCLUSIONS

A 100 x 100 CCD array, organized in a SPS (series, parallel, series) format, has shown itself to be a very versatile device. Although normal operation is a 2-phase, 10k element, self-scanning image sensor, the device design includes a 100 x 1 bit input register which may be used for electrical input. By using a common set of clock voltages to drive the electrical input register of the identical (storage only) devices in synchronization with the imaging chip, data has been shown stored in temporary memory and subsequently read out for frame-to-frame subtraction on succeeding fields. Or the output of the memory chip may be tied back to its own input and the information recirculated for an indefinite period if appropriately refreshed.

Operation in the frame-to-frame subtraction mode allows the detection of moving objects in the field of view. Operation in the recirculation mode, with refresh, increases the storage capability of the device since each bit now has several analog levels associated with it. Areas of application include security systems for detection of unauthorized entry, storage of the scene at the time of the alarm, and slow scan transmission to a remote monitoring point.

A prototype camera and signal processing unit, operating in the above described modes, has been built with one imaging chip and two storage CCDs.

Operation of the unit is simplified by a unique electrical interface allowing the output to be displayed on an unmodified 30 frame/second CCTV monitor. This allows the camera mode of operation to be compatible with EIA RS170 format monitors and recording devices. It is believed that the use of this smaller device in a CCTV compatible format offers cost advantages in those applications where the higher resolution, and consequently higher cost, of larger devices is not necessary.