Charge Coupled Device (CCD) Analog Signal Processing*

Marvin H. White Donald R. Lampe

Westinghouse Defense & Electronic Systems Center, SDD,
Advanced Technology Laboratories, P.O.Box 1521, Balto.,Md. 21203

ABSTRACT

CCD basic building blocks provide a flexible approach to analog signal processing in systems. The Serial In/Serial Out (SI/SO) block provides time-base translation through electrically alterable time delay and recursive, programmable, filter-banks may be realized with the addition of PROM's or EAROM's (adaptive programming) to determine filter center frequency, bandwidth, and gain. The Parallel In/Serial Out (PI/SO) block may be used for time-division-multiplexing (TDM) of signals from a number of parallel channels into a serial data stream; and through the "delay and add" mode of operation, the PI/SO block permits sensor array beam forming and steering as well as convolution. The Serial In/Parallel Out (SI/PO) block provides variable tapped delay lines and transversal filters/correlators. Electrically reprogrammable analog weights combined with these building blocks offer adaptive filtering for communications. Combinations of the above linear or one-dimension blocks may be employed for Fourier transforming, filter banks and multiple correlators. Applications of CCD's are discussed for Radar, Sonar and Communication Systems.

1.0 Introduction

A simplification of the charge-coupled (CCD) analog shift register is shown in Figure 1. The timing is arranged so the switch toggling frequency is one half of the four-phase clock frequency. Thus, the input sampling switch, S_1, alternately samples data and zero reference. At the output, switch S_2 clamps during zero reference, samples during data, and holds when it is not actually sampling. The output holding capacitor, therefore, contains only the "time-stretched" data samples. In a shift register having N pairs of stages, there will be N signal samples and N zero reference samples, each of duration T/2.

Figure 2 illustrates some key waveforms which are applied to the CCD analog shift register. The waveforms ϕ_1 through ϕ_4 are the four-phase clocks whose function is to propagate charges down the line without dispersion. Waveform S_1 demonstrates the switch functions; data is sampled in the up position and zero reference is sampled in the down position. V_o demonstrates the appearance of the delay line output voltage with the alternate data and zero reference outputs confined to 3/8T. S_2 demonstrates the output processing functions: the data is sampled in the up position, the zero is clamped in the down position, and the data is held when it is not sampled (center). The interval from data sample to data sample is T and the total transport time is NT where N is the number of CCD analog delay line data stages. Thus, the signal delay for a serial in/serial out (SI/SO) CCD analog shift register is,

$$\tau = NT = N/f_c \qquad (1)$$

which illustrates the electrically alterable delay feature of the CCD delay line.

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Since the Shannon Sampling Theorem requires the analog signal to be sampled at least twice during its period we may write,

$$f_s \leq 1/2T = f_s(max) \qquad (2)$$

and the time-delay signal bandwidth product becomes,

$$\tau f_s \leq N/2 \qquad (3)$$

The low frequency limit is set by the thermal leakage current which accumulates in each stage, and the upper frequency limit is determined by input injection limitations and transfer efficiency.

Figure 3 illustrates a cross-section of a four-phase electrode CCD with transfer and storage electrode dimensions. The CCD is fabricated with PMOS silicon-gate technology and the insulator is a dual dielectric comprised of silicon nitride (Si_3N_4) over thermal silicon dioxide (SiO_2). The electrodes are fabricated with polycrystalline silicon and aluminum, to give coplanar but overlapping electrodes. The overlapping electrode feature provides a "sealed" CCD surface and stable operation over temperature-bias excursions.

2.0 Signal Transport in a CCD

The CCD delay line[2,3] provides a unidirectional transfer of signal charge $q_s(x,t)$ from one storage cell to another adjacent cell. The signal charge is designated in cell x at time t, where x and t assume integer values; i.e., the unit of distance is the cell-to-cell separation X_0 (center-to-center), and the unit of time is the stepping interval T (clock period).

The frequency response of the CCD delay line may be calculated from a discrete frequency expression for the signal charge:

$$q_s(x,t) = \epsilon\, q_s(x,t-1) + (1-\epsilon)\, q_s(x-1,t-1) \qquad (4)$$

where ϵ is the transfer inefficiency per stage delay with typical values of $\epsilon \leq 10^{-4}$ for $f < 1$ MHz. Since equation (4) is a discrete set of signal values in the time domain, we may transform the signal charge to the Z-domain:

$$Q_s(x,Z) = Z^{-1}[\epsilon Q_s(x,Z) + (1-\epsilon)Q_s(x-1,Z)] \qquad (5)$$

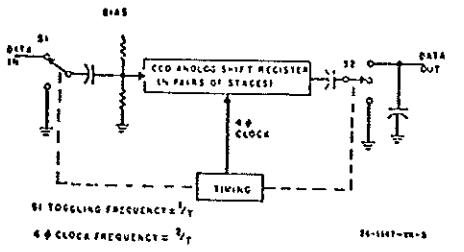


Figure 1. Charge Coupled (CCD) Analog Shift Register[1]

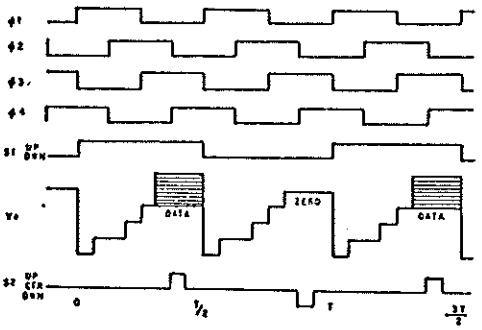


Figure 2. Basic CCD Four-Phase Clock Timing [4]

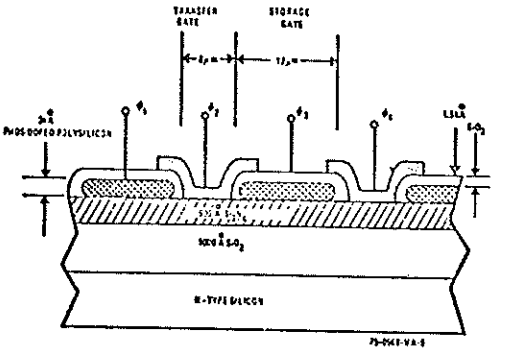


Figure 3. Cross-section of Four-Phase CCD Stage Delay

The transfer function of a N-stage CCD delay line becomes[4]

$$H(Z) = \frac{V_{out}(Z)}{V'_{in}(Z)} = \frac{g_m R_F C_{in}}{C_{out}} \left[\frac{1-\epsilon}{1-\epsilon Z^{-1}}\right]^N Z^{-N} \quad (6)$$

and the substitution of $Z = e^{j\omega t} = e^{j2\pi f_s/f_c}$ into equation (6) yields the amplitude and phase characteristics shown in Figures 4 and 5, respectively,[5] for various values of $N\epsilon$. The signal frequency, $f_s \leq 0.5 f_c$ as restricted by the Shannon Sampling Theorem; which states that a band-limited signal, f_s, may be reconstructed from samples taken at time intervals $T = 1/f_c$. The phase deviation $\Delta\phi(f_s)$ is the departure from linear phase shift. The insertion loss of the CCD delay line is less than 2 dB at the Nyquist limit ($f_s = 0.5\, f_c$) if $N\epsilon < 0.10$ and the maximum phase deviation at $f_s = 0.25 f_c$ is less than 3°.

2.1 Frequency Dispersion

This dispersion can be viewed in the frequency domain as a shift in the filter response frequency with the maximum shift at one-half the clock frequency.

$$f'_s = f_s + \frac{\epsilon f_c}{2\pi}\left[\sin\frac{2\pi f_s}{f_c} - j\left(1 - \cos\frac{2\pi f_s}{f_c}\right)\right] \quad (7)$$

2.2 Amplitude Dispersion

The signal is "dispersed" or spread-out in time as a result of the finite transfer inefficiency ϵ and the number of cells, N. The dispersion of a single data sample of unit height (i.e., one propagating storage cell through the delay line) may be determined by the binominal expansion theorem:

$$[(1-\epsilon) + \epsilon]^N = \sum_{t=0}^{N} \binom{N}{t} (1-\epsilon)^{N-t} \epsilon^t \quad (8)$$

$$\doteq \sum_{t=0}^{N} q_s(N, t)$$

$$\binom{N}{t} = \frac{N!}{t!\,(N-t)!} \quad (9)$$

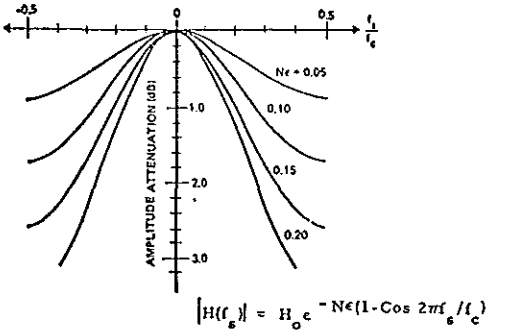


Figure 4. Amplitude attenuation characteristics as a function of f_s/f_c for various values of $N\epsilon$.

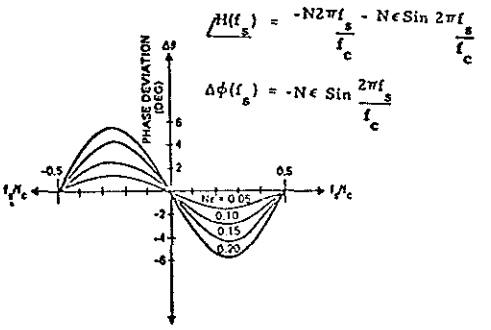


Figure 5. Phase Deviation as a function of f_s/f_c for various values of $N\epsilon$.

Figure 6 illustrates the effect of $N\epsilon$ product[6] on the shape of a single data sample of unit height. The total area under the output waveforms is identical to the area under a single sample at $\epsilon = 0$. The peak of the signal lags by one clock period when $N \approx 1/\epsilon$ and dispersion is minimal for $N\epsilon \leq 0.10$.

3.0 CCD Basic Building Blocks for Discrete Analog Signal Processing (DASP)

Any signal processing system that involves the linear transformation of analog signals such as correlation, discrete Fourier transformation (DFT), filter banks, matched filters, multiplexing/demultiplexing, array scanning, orthogonal scan transformation, time base translation, etc., can be realized with combinations of CCD basic building blocks. In discrete analog signal processing (DASP),

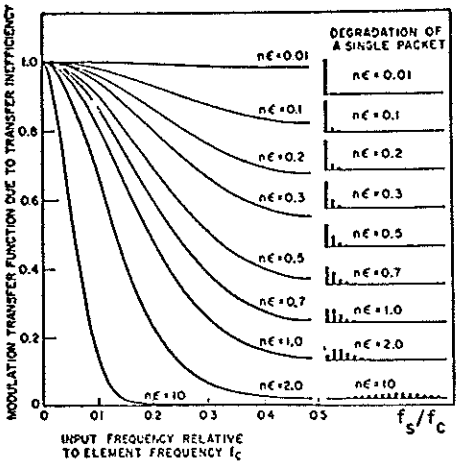


Figure 6. Degradation (Amplitude Dispersion)[6] of a Single Charge Packet as a function of Nε.

analog data samples are stored, transferred, and operated upon by analog means, whereas in conventional digital signal processing (DSP), digital or quantized samples are handled with binary logic. A major advantage of DSP is retained by DASP, namely the precise transport delay, particularly in relation to coherent signal processing. The dynamic range of an analog bit in DASP may be thought of as composed of 6-dB equivalent DSP digital bits. Thus, a typical example of 100 Stage (N = 100) CCD delay line with 60-dB dynamic range and transfer inefficiencies of $\varepsilon \sim 10^{-4}$ at 1-to-2 MHz clock rates will have an overall signal degradation of 1 percent (i.e., less than 0.1-dB insertion loss) without the need of A/D conversion.

One-dimensional basic building blocks[7] (linear arrays) may be classified according to the characteristic information flow patterns:

(1) Serial in/Serial out (SI/SO)
(2) Parallel in/Serial out (PI/SO)
(3) Serial in/parallel out (SI/PO)

These fundamental linear arrays may be combined to form area arrays (2-dimensional matrices) with increased signal processing capabilities. Table 1 provides a partial listing of applications for these basic building blocks.

Table 1

Array Configuration	Basic Information Flow: Serial In; Serial Out (SI/SO)	Parallel In; Serial Out (PI/SO)	Serial In; Parallel Out (SI/PO) - Nondestructive Sensing Taps - Unweighted	Serial In; Parallel Out (SI/PO) - Nondestructive Sensing Taps - Weighted
Linear	Pure Delay; Time Base Interchange	Time Division Multiplexing; Array Scanning	Beam Focusing; Focus Scanning Multiple-Beam Forming; Beam Steering	Transversal Filtering; Correlation/Convolution; Adaptive Filtering; Sampled Data Smoothing or Interpolation (Scan Format Converter)
2-d Matrix (Area)	Bulk Serpentine Analog Storage*		Corner Turn (Orthogonal Scan Transformation)	Discrete Fourier Transformers; Filter Banks; Multiple Cross Correlators
	Bulk Serial-Parallel-Serial (SPS) Analog Storage*			

*As for Video Refresh Memories

3.1 Serial In/Serial Out (SI/SO)

The SI/SO block is a simple CCD shift-register with the characteristics discussed in sections 1 and 2. In a linear array configuration the SI/SO block provides pure analog signal delay with the ability to provide time base translation. Typical dynamic range for present-day SI/SO blocks is 60-80dB with ±1 percent linearity and clock frequencies from 1KHz-1.0MHz for a 64 analog bit delay line. The clock requirement may vary from device to device with voltages varying from TTL to MOS compatible. In general, MOS-type voltage swings are needed to obtain dynamic range and frequency response. The capacitance loading for the drivers is typically 0.2pF/mil^2 of active bit area; for bit areas of 1.5 mil^2 we have 0.3pF/analog bit. Thus, a 64 bit delay line will offer a loading of ≈20pF/driver. In general, CCD

structures have not been built with interface/buffer circuits on the chip because of the advanced development nature of the work; however, CCD chips can be fabricated with MOS, CMOS, or bipolar interface circuits. In order to test SI/SO blocks without on-chip buffer circuits, a so-called "open collector" driver may be employed. This driver is relatively inexpensive and provides clock voltage swings of 30V up to 2 MHz clock frequencies. Clock shaping may be accomplished if desired by the use of a series resistor, which also protects the drivers in the pull-down transient. A CCD chip should have protective resistor/diode combinations, similar to MOS-type circuits, to limit the displacement current and prevent shorting of the input electrodes.

For analog signal processing, as discussed in the introduction, a desirable feature is the incorporation of an a-c zero reference between successive signal samples, particularly for PI/SO and SI/PO blocks. In addition, sample and hold techniques are required for analog signal reconstruction which attenuates the response with a $\frac{\sin \pi f_s/f_c}{\pi f_s/f_c}$ shape factor. The input to a CCD may also be filtered with a $\frac{\sin \pi/\Delta t f_c}{\pi/\Delta t f_c}$ roll-off where Δt is the sampling window aperture. The output after sample and hold requires filtering with a low-pass filter with ideal "brick-wall" cut-off at $f_c/2$, the Nyquist limit. Figure 7 illustrates an analog output swept frequency response of a CCD SI/SO block with sample/hold and a 7-pole Butterworth filter (-3dB @ 750 KHz) to filter the clock and limit the aliasing of frequencies higher than $f_c/2$. Thus, in a properly designed CCD Analog Delay Line the frequency response is limited by the sample/hold and low-pass filter characteristics.

A time multiplexed CCD filter bank[1] which used SI/SO blocks is shown in the block diagram of Figure 8. The Filter-Bank Characteristics are illustrated in Figure 9 for the case of uniform filter spacing. Storage and sequencing of the constants is accomplished digitally using programmable read only memories (PROM) or electrically alterable ROM's (EAROM's). Weighting of the analog signals by the filter constants is accomplished by means of multiplying digital-to-analog converters. The serial output data is multiplexed onto N lines by the output sampler which stretches each sample to a width, $T_s = NT$. Timing circuitry provides the CCD clock waveforms, the PROM addresses, and the sampler address. Applications of this filter bank include Doppler spectrum processing in radar, sonar and communications systems with advantage of low total part count combined with variable filter parameters.

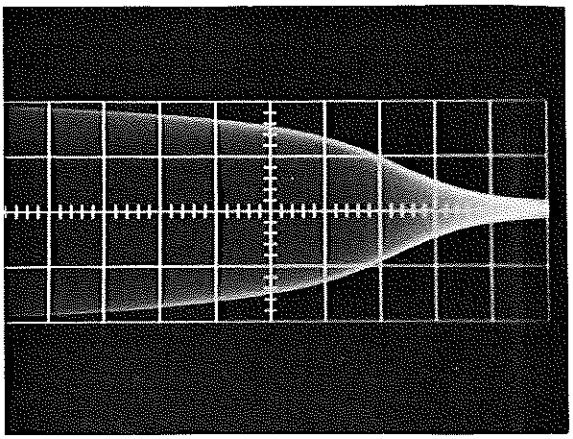


Figure 7. Frequency Response of Sampled Data CCD Analog Delay Line. 100 KHz/Div. Horizontal, $f_c = 2.0$ MHz. Transfer inefficiency ε ($f_c = 2.0$ MHz) = 2×10^{-3} for L = 12μm electrodes. Sample/Hold and Filter Responses are included in the overall response.

The main signal processing function in a moving target indicator (MTI) radar is the main beam clutter (MBC) canceller. A three pulse canceller using CCD's is illustrated in Figure 10. Each delay line contains a number of range cells (or bins) adequate for the required resolution and range coverage. Low pulse repetition frequencies (PRF's) with interpulse periods (IPP) of 0.5 to 5 milliseconds are use to provide unambiguous range detection. The delay in each CCD shift register for a given range cell is one IPP. In MTI radars with more than 500 to 1000 range cells, the CCD shift register may be arranged in the serial-parallel-serial (SPS) configuration to minimize the effects of charge transfer inefficiency. The dual sampling scheme of figures 1 and 2, then automatically

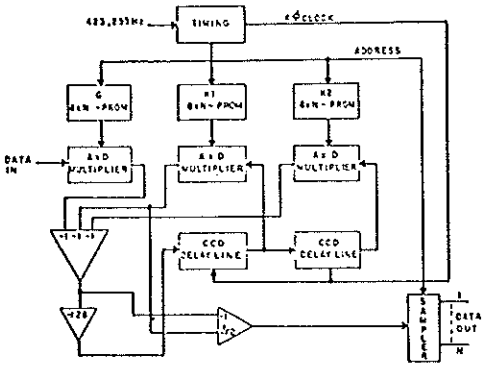
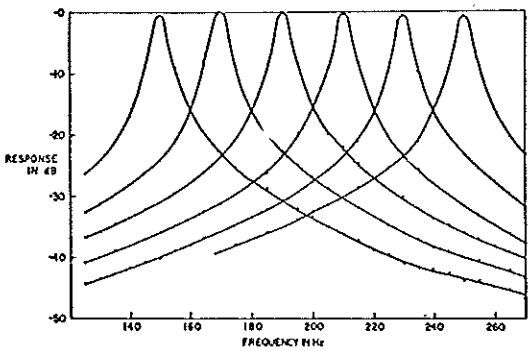


Figure 8. Block Diagram of N-channel CCD Filter Bank[1]



CENTER FREQUENCY IN Hz	BANDWIDTH IN Hz	G	A1	A2
150	5	1.00	0.75	-0.96
170	5	1.00	0.46	-0.96
190	5	1.00	0.15	-0.96
210	5	1.00	-0.15	-0.96
230	5	1.00	-0.46	-0.96
250	5	1.00	-0.75	-0.96

Figure 9. Uniform Filter Characteristics[1]

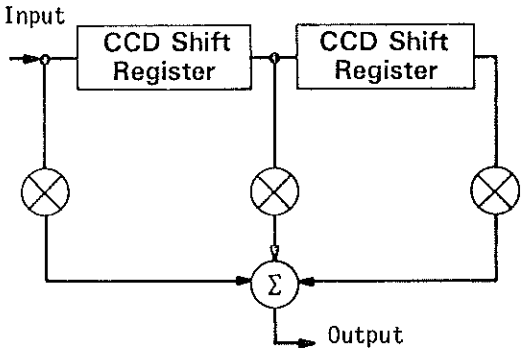


Figure 10. CCD Clutter Canceller for a Moving Target Indicator (MTI) Radar

eliminate most effects of leakage current nonuniformities since both "signal with reference" and "reference only" samples follow identical paths.

3.2 Parallel In/Serial Out (PI/SO)[8]

The PI/SO block may be used to time division multiplex a number of low data rate signal channels into a higher date rate output channel. The variations in electrical input may be minimized with the use of a stabilized charge injection circuit. An N-channel multiplexer converts N parallel input channels into a single-channel pulse amplitude modulated (PAM) signal. The input signals are synchronously sampled and the sampler information is entered into a unique spatial and temporal position in the CCD delay line. Applications include the multiplexing of many sensor input channels (e.g. electro-optical sensors, acoustical sensors) into a single video output channel. Figure 11 illustrates a photomicrograph of a PI/SO CCD chip with stabilized charge injection and parallel injection of alternate stage delays along the CCD delay line to minimize interchannel cross-talk and provide for the injection of an a-c reference for threshold voltage cancellation. Figure 12 illustrates the response of a PI/SO block with N = 20 and a simultaneous unit impulse at each parallel input. The injection of a reference and a signal and reference permits subsequent subtraction at the CCD output to remove input variations. Voltage variations,referenced to the input, not exceeding 100μV

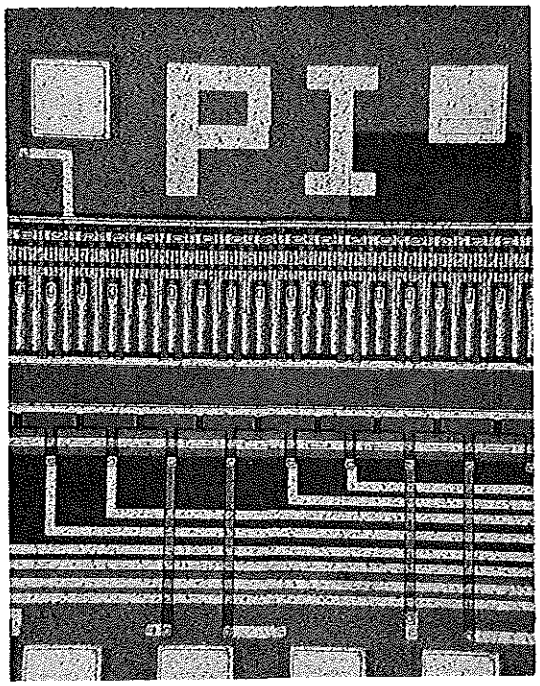


Figure 11. Photomicrograph of PI/SO CCD Basic Building Block.

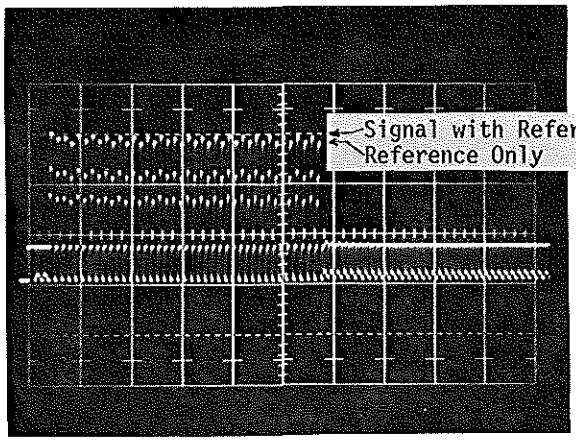


Figure 12. Impulse Response for Uniform Weighting Prior to Subtraction of Signal and Reference and Reference Inputs.

have been obtained to remove fixed pattern noise and place the limitation on noise with the charge injection uncertainty associated with the input capacitance.

The PI/SO block may also be operated in the time delay and add or integrate (TDI) mode to give such signal processing functions as sonar beam forming and steering or convolution. Formation of sonar or any acoustic beams using an array of transducers is illustrated in Figure 13.

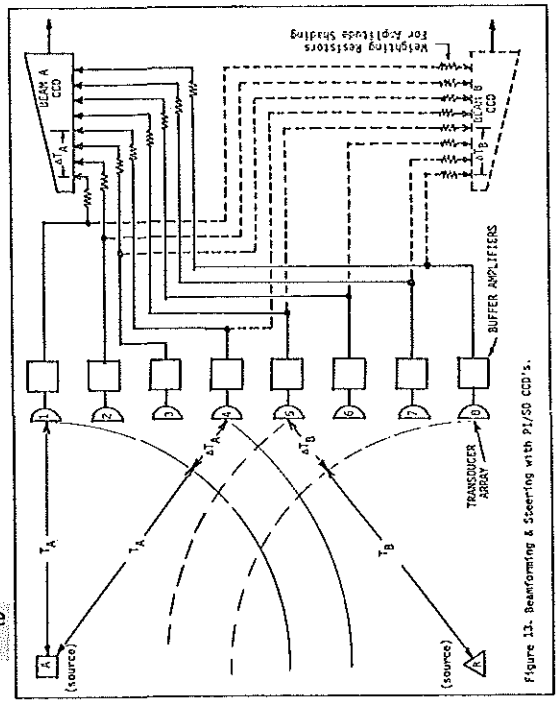


Figure 13. Beamforming & Steering with PI/SO CCD's.

Transducer "1" is first to receive the signal from source A which is suitably weighted and injected into the "Beam A" CCD, where it is delayed. The signal next arrives at transducer "2" and is weighted accordingly. When it is injected into "Beam A" CCD, the weighted signal from transducer "2" is added to the weighted signal from transducer "1". As the signal from source A arrives at each transducer in turn, it is weighted, injected into the "Beam A" CCD, and added to the previously accumulated signals that were injected and delayed from the closer transducers. The output charge integrated in any charge packet during transit through the "Beam A"

CCD may be written

$$Q_{out}(t) = \sum_{k=1}^{N} V_k\,(t-kT) \cdot W_k \cdot C_k \qquad (10)$$

where W_k = k^{TH} weighting coefficient, C_k = k^{TH} input capacitance, $V_k(t)$ = signal from k^{TH} transducer, T = CCD clock time. [Note: A common signal source applied to all weighting resistors, i.e., $V_k(t) \equiv V(t)$ for all k, gives a convolution of the signal V(t) with an impulse response function determined by the quantities $(W_k \cdot C_k)$.] Although the use of the PI/SO block in the TDI mode typically involves a progressively larger charge packet as the packet propagates from the initial input to the final output, such an approach has some advantages over the use of the SI/PO block for the same functions: ease of fabrication and yield, interface simplicity, and lower power dissipation.

3.3 Serial In/Parallel Out (SI/PO)

The SI/PO block features INDEPENDENT nondestructive, low-impedance voltage readouts of the analog signals at specified locations or taps corresponding to various delays through the CCD shift register. In general, the signal voltage at each tap may be multiplicatively weighted by conductance to give a current proportional to the PRODUCT of the signal voltage by the weighting conductance. Summation of the product currents provides such functions as transversal filtering, correlation, or sampled data smoothing/interpolation for line arrays. Two dimensional weighting matrices driven by the independent low-impedance taps of the SI/PO block can give discrete Fourier transformers, filter banks, or multiple cross correlators. Figure 14 illustrates a photomicrograph of a SI/PO block (N = 20 outputs) which uses a floating clock electrode sensor at alternate stage delays along the CCD delay line. This permits the use of a "reference-only" and "signal and reference" to compensate for nonuniformities in the SI/PO structure. Figure 15 shows the tapped output signal from the SI/PO block. Numerous taps with multiplicative analog weighting can be accomodated without signal amplitude degradation due to stray parasitic capacitance, by paralleling SI/PO blocks of feasible size due to the summation of product currents. Furthermore, the independent nondestructive voltage taps of the SI/PO block can provide the analog voltage signals needed by multipliers[9] to give CCD real-time analog correlation.[9] Use of programmable conductances such as the nonvolatile MNOS type[7] or conventional MOS type permit such device applications as adaptive transversal line equalizer or programmable matched filter (or correlation detector) for secure voice/data communications systems

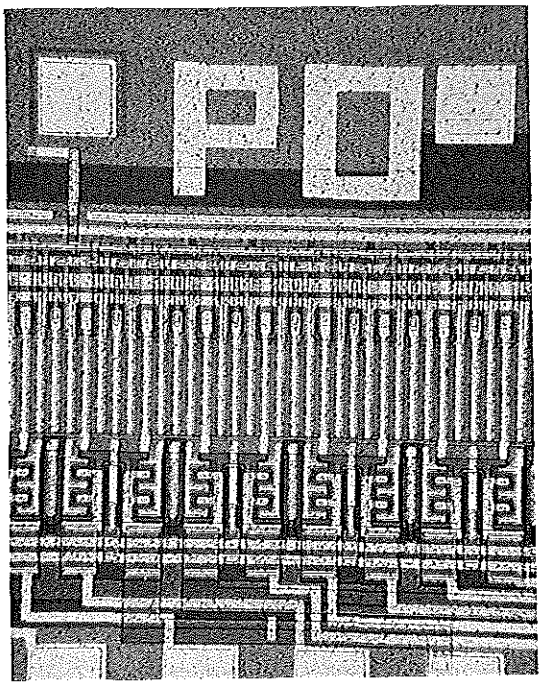


Figure 14. Photomicrograph of SI/PO CCD Basic Building Block

4.0 Conclusions

Many signal processing systems which involve the linear transformation of analog signals, such as matched filters or multiplexing/demultiplexing, can be realized with a finite number of CCD basic building blocks. To impact future electronic systems, the CCD basic building blocks should be flexible in the sense that systems design engineers can use them in a variety of applications. Thus independent unweighted taps keep the active device relatively simple yet require the use of external resistors and output buffer/reconstruction circuitry for trans-

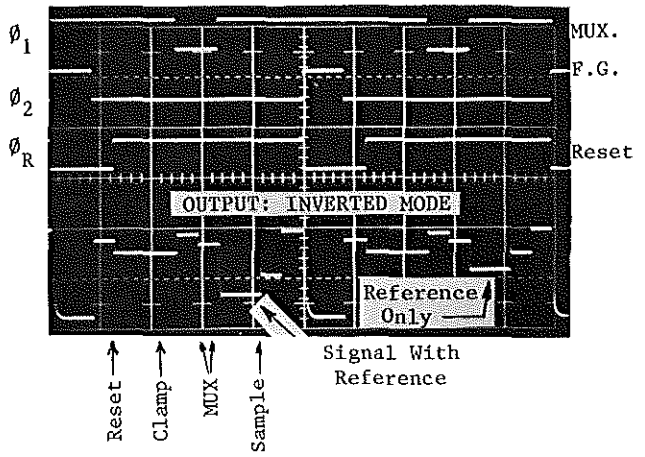


Figure 15. Floating Clock Electrode Sensor for SI/PO Block

form operations. But the main advantage is that a single device design may be used to satisfy many applications requirements. In systems where the external resistors are too clumsy, but tap weight adjustment is desired, electrically alterable tap weights are appropriate. This is clearly the most powerful method of tap weighting, which can lead to real-time analog correlators and/or adaptive filtering as well as tap error compensation. Devices having electrically alterable taps are substantially more complicated than fixed tap or unweighted devices but can be used as universal filter/correlator building blocks. Such universal blocks can benefit from the economics of high volume production and find diverse applications ranging from one-of-a-kind R and D to production systems.

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