CCD-TV CAMERAS
UTILIZING INTERLINE-TRANSFER AREA IMAGE SENSORS

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ABSTRACT

A recently developed Fairchild CCD area array image sensor of 190 x 244 elements, described in a paper by Kim, Steffe, and Walsh at this conference, and a 380 x 488 element device currently being developed have design features which simplify application of these sensors in compact, highly ruggedized solid-state TV cameras. Sensor characteristics are reviewed with emphasis on the reduction of camera circuit complexity resulting from the use of two-phase charge transport principles in combination with interline-transfer device organization.

Several camera designs using the 244 and 488 devices are described including a 488 LLLTV camera and a 244 camera pair which effectively doubles the image format pixel density along the row direction. Experimental results demonstrating low-light-level and multiplexed camera pair operation are presented.

The MV201, Fairchild's commercial camera product is described. The design employs the 190 x 244 element image sensor. The electronic circuit blocks comprising the camera are described as well as the techniques employed for miniaturization.

Variations on the basic MV201 design are discussed. These include a two-piece camera with a 1-½ inch diameter ¾-inch thick sensing head, a "G" hardened version designed to withstand howitzer shell launch conditions, and a version for use in borehole applications where the output is converted to slow-scan video for transmission over several miles of cable.

INTRODUCTION

The interline transfer (ILT) organization has been adopted for a family of charge coupled image sensors, including designs with 100 x 100, 190 x 244, and 380 x 488 elements [1,2,3]. Each design employs two-phase (2ϕ) charge transport principles which, in combination with the ILT organization, minimizes the number and complexity of gate drive waveforms necessary for device operation. In addition, each design employs buried channel principles which eliminate the surface channel device requirement for bias charge or "fat-zero" insertion. For the 190 x 244 sensor, buried channel operation is combined with an on-chip low noise distributed floating gate amplifier (DFGA) with a resultant significant increase in low light sensitivity [3,6]. Threshold signal packets of a few tens of electrons can be efficiently transferred and detected.

As shown in Figure 1, the total number of gate drives or forcing-functions for ILT operation is significantly less than for a typical 3ϕ frame-transfer design-simplifying the utilization of ILT sensors in compact, all solid state TV camera equipment. The 3ϕ design requires the generation of 3 different waveforms for each of the 3 sets of vertical (V) and horizontal (H) transport gates. Only two V and H transport waveforms are required for the 2ϕ ILT since the inputs for each H and V pair are complementary.

Figure 2 illustrates the ILT organization and the forcing-function inputs required for self-scan operation as a TV image sensor. The unit cells contain one photosensor site and an adjacent light-shielded site which is one-half stage of a 2ϕ vertical-transport register. Cell dimensions are defined by comb channel stop boundaries on three sides of the photosite. Alternate cell rows are uniquely assigned to each of the two fields comprising a TV frame resulting in higher vertical MTF than for beam-scanned or frame-transfer type image sensors. An implanted potential barrier at the photosite/transfer site interface inhibits transfers to the vertical column register, except when the photogate (ϕ_R) is LOW and the adjacent transfer gate (ϕ_{V1} or ϕ_{V2}) is HIGH. Thus, 2/1 interlace readout is achieved by pulsing ϕ_R LOW during each vertical blanking interval and applying complementary ϕ_{V1}, ϕ_{V2} waveforms with HIGH states during alternate V-blanking periods.

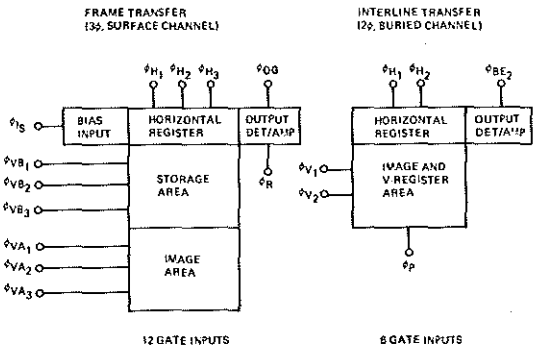


FIGURE 1. GATE DRIVE INPUTS FOR CCD-TV IMAGE SENSORS

At the start of the ODD field readout, elements corresponding to odd number rows are first shifted in unison into adjacent ϕ_{V1} sites for row transport along the column registers to the output register. The EVEN field sequence is similar except the initial shift is into ϕ_{V2} sites. Row transfers at the output register interface (for both ODD and EVEN rows) are effected by holding ϕ_{V1} LOW and ϕ_{H1} HIGH during the horizontal blanking interval. Complementary square wave pulses at element rate are applied to the ϕ_{H1}, ϕ_{H2} transport gates to serially shift packets to the output detector.

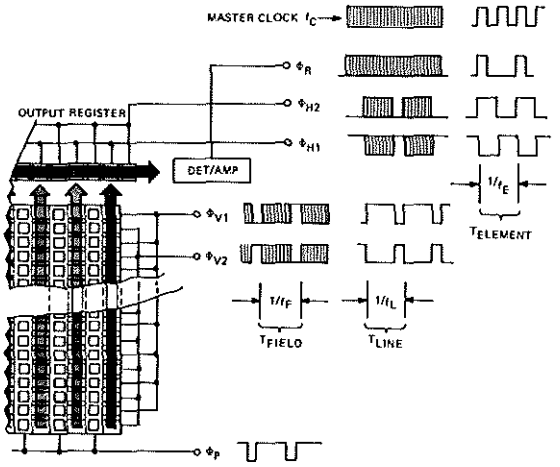


FIGURE 2. INTERLINE TRANSFER CCD ORGANIZATION AND DRIVE INPUT WAVEFORMS

CAMERA DESIGN FOR 525 LINE TELEVISION

Circuit functions for a TV camera using interline-transfer image sensors are illustrated in the block diagram, Figure 3. With the exception of the CCD and its associated gate drive waveforms, similar functions (plus horizontal and vertical scanning) are necessary for conventional camera designs using beam-scanned image sensors. A typical ILT-CCD camera logic design employs a crystal clock at frequency $f_C = 2f_E$, where f_E is the element readout rate, to provide decoding edges for pulses shorter in duration than an element period. All CCD gate waveforms, and the display sync and blanking signals are derived from f_C by divide-down counters and combinational logic circuits.

A beam-scanned camera design requires relatively complex logic circuits to conform with 525 line TV system specifications such as EIA RS-170. In this case, the function of the logic is to synthesize synchronization and blanking waveforms with timing edges defined from the output of a master clock operating at a high multiple of the line scan frequency f_L. A typical single-chip MOS-LSI TV signal generator, such as the Fairchild type 3262, is controlled by a crystal clock operating at 910 f_L, facilitating the generation of a synchronous NTSC color subcarrier output at the nominal US Standard 3.58 MHz rate[4]. Decoding edges for either monochrome or color system outputs are derived from an on-chip square wave clock at 130 f_L.

Although existing waveform generators such as the 3262 do not provide CCD gate signal outputs, a modified CCD/RS-170 compatible design is feasible if the CCD design conforms to system specifications. For CCD imaging sensors, conformance implies a precisely defined number of readout lines per field. Also, if the CCD sensor element counts per line are properly defined, a simplified camera logic design using a single master clock input is possible.

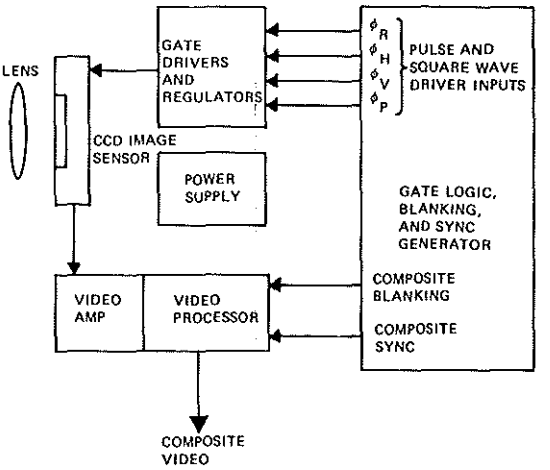


FIGURE 3. FUNCTIONAL REQUIREMENTS FOR A CCD-TV CAMERA UTILIZING AN ILT AREA IMAGE SENSOR

In accordance with 525-line monochrome system specifications the nominal values required for readout scan parameters are: line rate f_L = 15,750 Hz ; field rate f_F = 60 Hz; and frame rate f_R = 30 Hz (with 2/1 field/frame interlace). The RS-170/3262 vertical blanking interval is (20 + 22/130) line periods/field, defining a minimum of (525-40) = 485 active scan lines, hence sensor element rows per frame.

Horizontal blanking is defined as (22/130) horizontal line periods, which is equivalent to: (22/130) $(n_A + n_B)$ = (22/130) n_T where n_A, n_B and n_T define the active, blanked, and total number of element periods/line period, respectively. If n_T is selected to be 910/2 = 455, a single master clock can be used to satisfy the requirements for both RS-170 and CCD gate-drive waveform synthesis. For this condition, n_B = (22/130) 455 = 77, and n_A = $(n_T - n_B)$ = 378. The CCAID-488B sensor currently being developed has 380 elements/row, and 488 rows, hence a few terminal rows and columns can be blanked off when blanking signal edges are properly centered with respect to the active format region.

CAMERA DESIGN USING 190 X 244 ELEMENT SENSORS

Semiconductor industry economic considerations clearly indicate a power function relationship between device cost and silicon chip size.[2] In addition, there are a number of TV camera applications which can be satisfied by sensors with fewer pixels/frame than required for 525 line broadcast-TV systems. These applications are being addressed by utilizing the small format (0.44 cm x 0.57 cm) 190 x 244 element sensor, as described below.

OPERATING MODES

The 190 x 244 element counts of exactly half the full format 380 x 488 design were selected to facilitate modes which are interface-compatible with existing TV system equipment including VTR's, display monitors, and TV receivers. These modes include:

FORMAT INSET MODE – All camera waveforms are identical to those required for operation of a 380 x 488 sensor, except for an extension of the horizontal and vertical blanking intervals. Thus, an NTSC compatible video signal can be generated over a portion of the full display format equal to ½ the active height and

width. The outputs from up to four cameras can be displayed on a single monitor by appropriate phasing of the active and blanking signal intervals prior to composite signal mixing.

FULL FORMAT, SYNTHETIC INTERLACE-MODE– By modifying the camera timing generator to enable counting an integral number of lines/field near the normal 262-1/2 line value, a non-interlaced display raster can be generated with horizontal and vertical scanning rates within a few percent of industry standards. A raster thus generated is "synthetically" interlaced by alternatively addressing the display with video lines of normal sensor and blanking signal followed by an artificially generated line signal with 100% blanking. During an ODD field sensor readout, lines 1, 3, 5, ---, N_{odd} of the active format contain sensor video signal while 2, 4, 6, ---, N_{even} are blanked off, with the video/blank line sequence reversing for the following EVEN field readout.

FULL FORMAT, FAST FRAME MODE – Camera timing logic, including display synchronization and vertical-blanking signals, are altered to generate a true 2/1 interlaced display with approximately half the usual number of active scan lines per field. VTR compatibility is achieved by selecting a 120-Hz vertical rate, which is an even multiple of the standard rate. Display circuit modifications are required, however, these modifications can be limited to the vertical scan generator if the horizontal scan frequency is selected to be within a few percent of 15,750 Hz. Advantages of the fast-frame mode include the elimination of interline display flicker, enhanced resolution for rapidly moving scene information, and reduction of dark signal effects limiting dynamic range at high operating temperatures.

MULTIPLEX MODES – Other system compatible modes are possible if two (or more) 190 x 244 element sensors are arranged to view identical scene information; by utilizing optical beam splitters and a single lens, or by employing matched individual lenses in a boresight configuration. The outputs of each sensor can then be combined, i.e., multiplexed, into a single video information channel. Thus a pair of ILT sensors with 190 elements/row and 244 rows/frame can be used to generate multiplexed video for a display with twice the pixel information content. Sensor outputs can be combined to yield 380 pixels/line with 244 lines/frame or 380 pixels/line pair with 488 lines/frame. A camera utilizing one of these modes is described in the next section.

THE BORESIGHT-244 CAMERA

Interline transfer image sensors can be operated in a unique element multiplexed-pair (E-MUX) mode which doubles the pixel density in the row direction [5]. The combined E-MUX video has characteristics similar to the video from an ideal single sensor with 380 contiguous pixels/line and 244 lines/frame. This effectively doubles the sampling density in the horizontal direction while maintaining the high MTF in the horizontal direction. Implementation principles are based on two characteristics of the ILT sensor organization:

1) element aperture response in the row direction is defined by a photosensing site width ≤ 0.5 cell width, and,
2) the readout signal interval corresponding to each sensing element is approximately 1/2 the element transfer period.

A camera pair, known as the Boresight-244 System, has been constructed to evaluate multiplexing principles. This system, as shown in Figure 4, consists of two identical cameras each employing the 190 x 244 sensor. A third assembly, the Multiplex Control Unit (MCU) allows the two cameras to interact in a variety of ways. Each camera can be operated as a stand-alone unit. As such, the element readout rate is 3.75 MHz, with a frame rate of 60 Hz. With both cameras and the MCU interconnected,

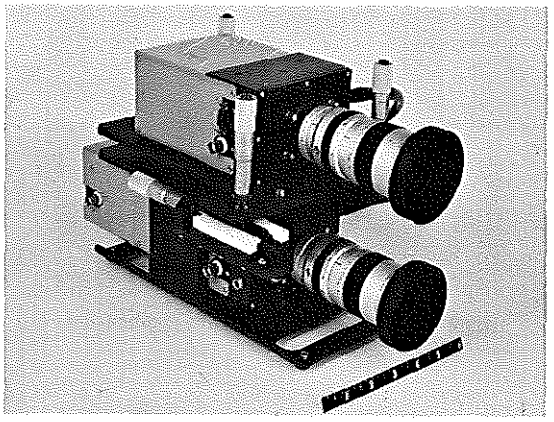


FIGURE 4. BORESIGHT-244 CAMERA SYSTEM

the cameras run synchronously in a master/slave relationship and the combined video signals can be displayed on a single monitor. After rough image alignment adjustment, the MCU is switched to the align mode. In this mode the signals from each camera are subtracted, thus an ideally boresighted pair results in a blank video display. Micrometer adjustments on one of the cameras are used to achieve alignment; once boresighted the adjustments are locked in position.

Following boresight alignment, the MCU can be switched to one of two operating modes. For resolution enhancement the MCU gates the video from each camera so that there are 380 (190 x 2) pixels per display line. In this mode the boresight alignment is modified to result in a 1/2 cell pitch offset between the image information viewed by the master and slave cameras, as indicated in Figure 5. The resolution in this mode is twice as much in the horizontal direction as for either of the contributing cameras. Vertical resolution is unchanged.

Figure 6 shows an enlarged portion of the displayed video output for the boresighted pair operating in the E-MUX mode. Horizontal resolution equivalent to the 285 TVL/PH Nyquist limit condition is obtained with both cameras operating. Applying identical techniques to a camera pair using 380 x 488 image sensors would yield a composite video output with 760 TV elements per format width; i.e., 570 TVL/PH horizontal resolution.

The other operating mode, known as the E-SUM mode, is concerned with signal-to-noise ratio enhancement. By boresighting the system and then summing the two outputs, the combined signal is twice that of a single camera viewing the same scene with the same lens T-value. Since the on-chip amplifier noise of each camera is uncorrelated, the SNR of a camera pair will be enhanced by a $\sqrt{2}$ factor.

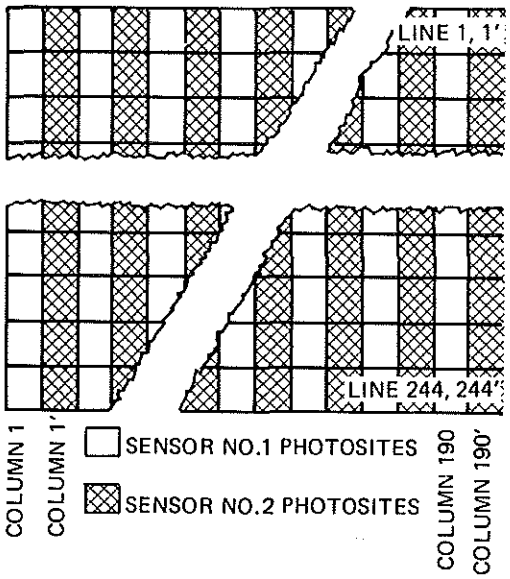
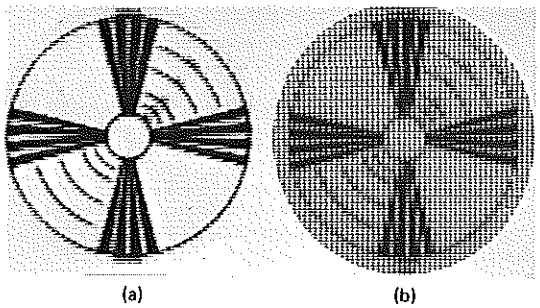


FIGURE 5. E-MUX SPATIAL ALIGNMENT FOR 244 X 190 SENSOR PAIR



(a) Enlarged portion of multiplexed-pair video display; (b) same as (a), except lens of one camera is capped. Resolution wedge calibration is 470 TVL/PH at center circle. 1st to 4th arc markings denote wedge resolutions of 312, 235, 156 and 117 TVL/PH, respectively.

FIGURE 6. BORESIGHT-244 CAMERA SYSTEM IMAGING

THE MV201 CCD-TV CAMERA

The Fairchild MV201 is a recently introduced TV Camera product utilizing the 190 x 244 element CCD-211 image sensor. Circuit design features have been included which permit packaging in a variety of compact camera configurations for specific application requirements.

The standard MV201 is housed in a near-cylindrical case, 2-½ inches in diameter and 3-½ inches long (approximately 17 cubic inches), as shown in Figure 7. It is a lightweight and rugged assembly requiring less than 4 watts from an external ±12 volt

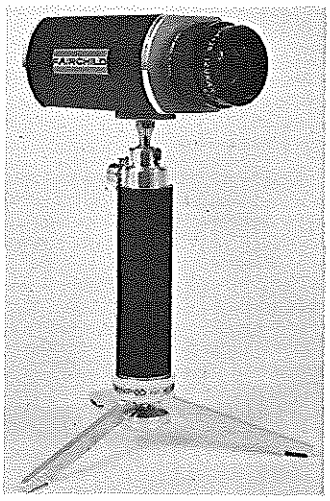


FIGURE 7. FAIRCHILD MV201 CCD-TV CAMERA

power supply. The lens bushing is a 16mm C-mount type, however, a number of small format TV and camera lenses can be used, including Super-8mm types.

The camera electronic circuits are arranged in three major functional groups: Logic Control, Gate Drivers and Video Processing. The logic is a crystal-controlled CMOS system which provides clocking at the nominal element rate of 3.766 MHz. A choice of frame rates is available, depending on user preference. The standard camera operates at 30 frames/second using the synthetic interlace mode; a 60/second fast-frame mode is available as an option. The line rate for either mode is 16.02 KHz.

Hybrid circuits are used for both Logic and Gate Driver functions. A total of six clock signals are applied to the CCD, however, these are derived from only three input waveforms due to the inherent simplicity of drive requirements for the two-phase interline-transfer CCD.

The Video Processor contains sample and hold, gamma compensation, and automatic gain control (AGC) circuits. The AGC feature extends the operating range to sensor highlight levels of less than 10^{-3}fc (2854°K). Camera output is a composite video, sync, and blanking signal suitable for driving up to 500 feet of coaxial cable. A typical camera output image is shown in Figure 8.

MV201 VARIATIONS

Due to its small size and low power, the basic MV201 design has been used as the basis for a number of interesting applications.

In environments where space is at an absolute minimum, the MV201 can be operated as a two-piece system comprised of the camera body, containing the electronics, and a remotely located sensor. The length of the cable may be two feet or longer, depending on the availability of space for electronics at the sensor location. A cable containing less than 20 wires connects the sensor to the electronics. The applications for such a system, wherein the sensor head (excluding optics) can be 1-½ inches in diameter and less that ¾-inch thick are widespread. The remote head may be substituted directly for the standard camera-housed sensor. One such application for this type of system is in aircraft with limited windshield space, where a camera is required to view the forward scene, as well as the heads-up-display superimposed

thereupon. Any obstruction to the pilot's view is undesirable, so a 1-½ inch diameter sensor head represents a near-ideal solution.

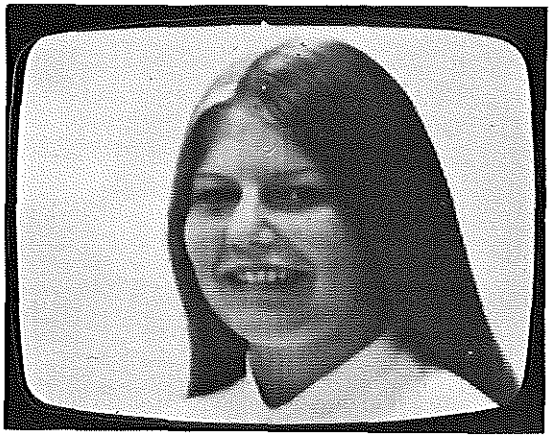


FIGURE 8. MV201 CCD-TV CAMERA IMAGE

The MV201 is being incorporated in a camera system to be used for underground inspection in the event of a mine disaster. In this situation a hole is first bored into the earth to reach the site. A long 2-½ inch diameter cylinder containing the camera, coupled to a scan converter, is then dropped into the borehole at the end of a connecting cable which can be up to 24,000' long. Single frame slow scan video is then transmitted to a receiving site at ground level. Due to the possibility of explosions in this type of environment, a standard vidicon system, with its associated high voltage, cannot be used without a large diameter explosion proof housing. The CCD approach overcomes these limitations.

The objective of a recently initiated development program is to incorporate the MV201 concept into an artillery-launched system. This system will provide real-time observation of preselected areas using a parachute-deployed TV camera and RF link. The system makes use of the major components of the XM485 illuminating round for the 155 mm howitzer, in which the illuminant is replaced with a ballistically matched package comprising the CCD TV camera, battery, RF transmitter, and antenna. The TV pictures are received and displayed in real time on a monitor and simultaneously recorded on video tape. During the launch of the shell, the camera system must endure accelerations of 14,000 G's. A completely solid state image sensor is clearly needed for such an environment.

A two-camera system, similar to the previously mentioned Boresight Pair, can be used to generate video corresponding to two different views of the same object suitable for reconstruction as three-dimensional stereo display images. The applications for stereo TV are numerous, including the inspection and control of objects or vehicles in remote or hazardous areas. The additional circuit requirements for paired-camera operation are relatively modest; over 75% of the electronics can be shared.

LLLTV CAMERA DEVELOPMENT

An all solid state TV camera is being developed with features designed to extend the illumination-sensitivity threshold to sensor highlight levels of 2×10^{-5}fc (10^{-5} W/m^2, 2854°K). Camera design parameters are based on utilization of a 380 x 488 element image sensor. The element clock rate is 7.16 MHz, with a 30 frame/second rate. The composite video output signal is designed to be fully compatible with 525 line TV display and VTR equipment.

Preliminary evaluations of camera circuit concepts and LLLTV performance have been made using the 190 x 244 image sensor, which incorporates the same design principles as the larger 380 x 488 version.

The images of figures 9 and 10 were obtained by processing and displaying the output signal from the on-chip 12-stage distributed floating gate amplifier (DFGA)[6]. Output imaging was observed for an 8000/1 range of sensor highlight illumination. The sensor readout rate was 30 frames/second, simulating 380 x 488 operation. Figure 9 illustrates imaging of a high-contrast pattern consisting of test bar groups at 1/4 and 1/2 Nyquist-limit horizontal resolution. Pictorial scene imaging for the same device, at similar highlight signal levels, is shown in Figure 10. The image sensor highlight level equivalent to the 25 electrons/pixel/frame threshold condition is approximately 2×10^{-5}fc –2854°K.

Figure 11 illustrates the camera configuration to be employed. The sensor is enclosed in a hermetically-sealed region containing a thermoelectric cooling module. The cooling feature has been included to minimize the dark current and dark current noise effects which can limit image detectability at very low signal levels.

CONCLUSIONS

CCD area image sensors of the interline transfer type are being utilized in all solid-state TV cameras for applications where very small size, low power/low voltage operation, high sensitivity, and extreme ruggedness, are either desirable or mandatory system requirements.

The CCD-ILT sensors, particularly the 190 x 244 and 380 x 488 designs, have features which make these devices useful for many operating modes not feasible with other types of solid-state and beam-scanned image sensors. Operation at very high frame rates is feasible, since the line transfer rate is never required to exceed line readout rate. Low light level operation has been demonstrated at threshold levels corresponding to signal packets of the order of tens of electrons. The ILT organization is adaptable to multiplexed operating modes, one of which demonstrates image resolution element densities in excess of 66 pixels/mm; comparable with silicon-target beam-scanned image sensor performance. Also, these ILT sensors have a unique capability for accepting information from an electrical input register. These features, when fully exploited, may be expected to result in significant new applications for solid-state TV cameras.

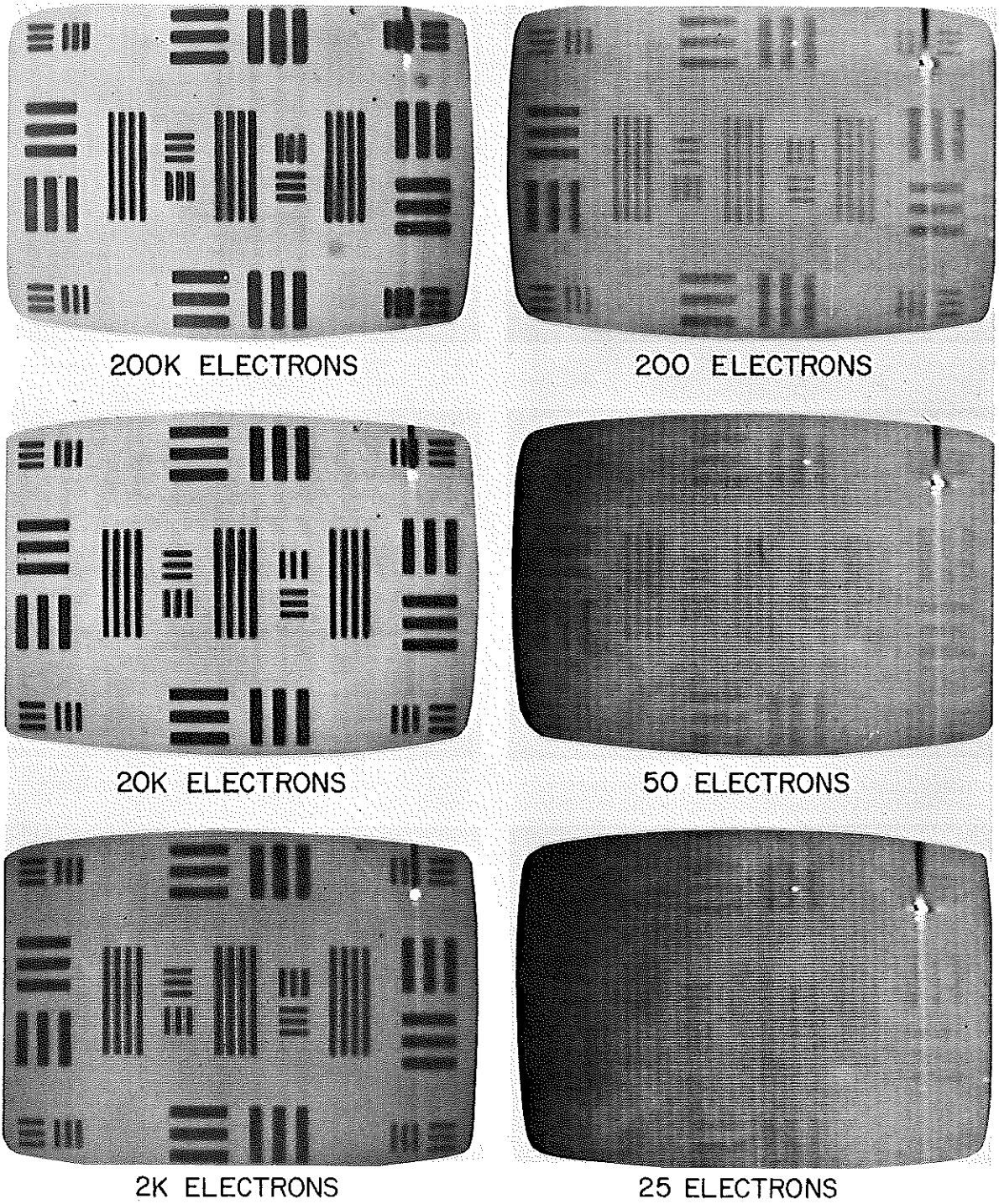


FIGURE 9. TEST BAR IMAGING WITH THE DFGA OUTPUT OF A 190 x 244 SENSOR
EXPOSURE TIME: 0.1 SECOND, TEMPERATURE: 0°C, 30 FRAMES/SECOND
ELECTRON COUNTS REPRESENT ELECTRONS/PIXEL/FRAME IN
IMAGE HIGHLIGHT REGIONS

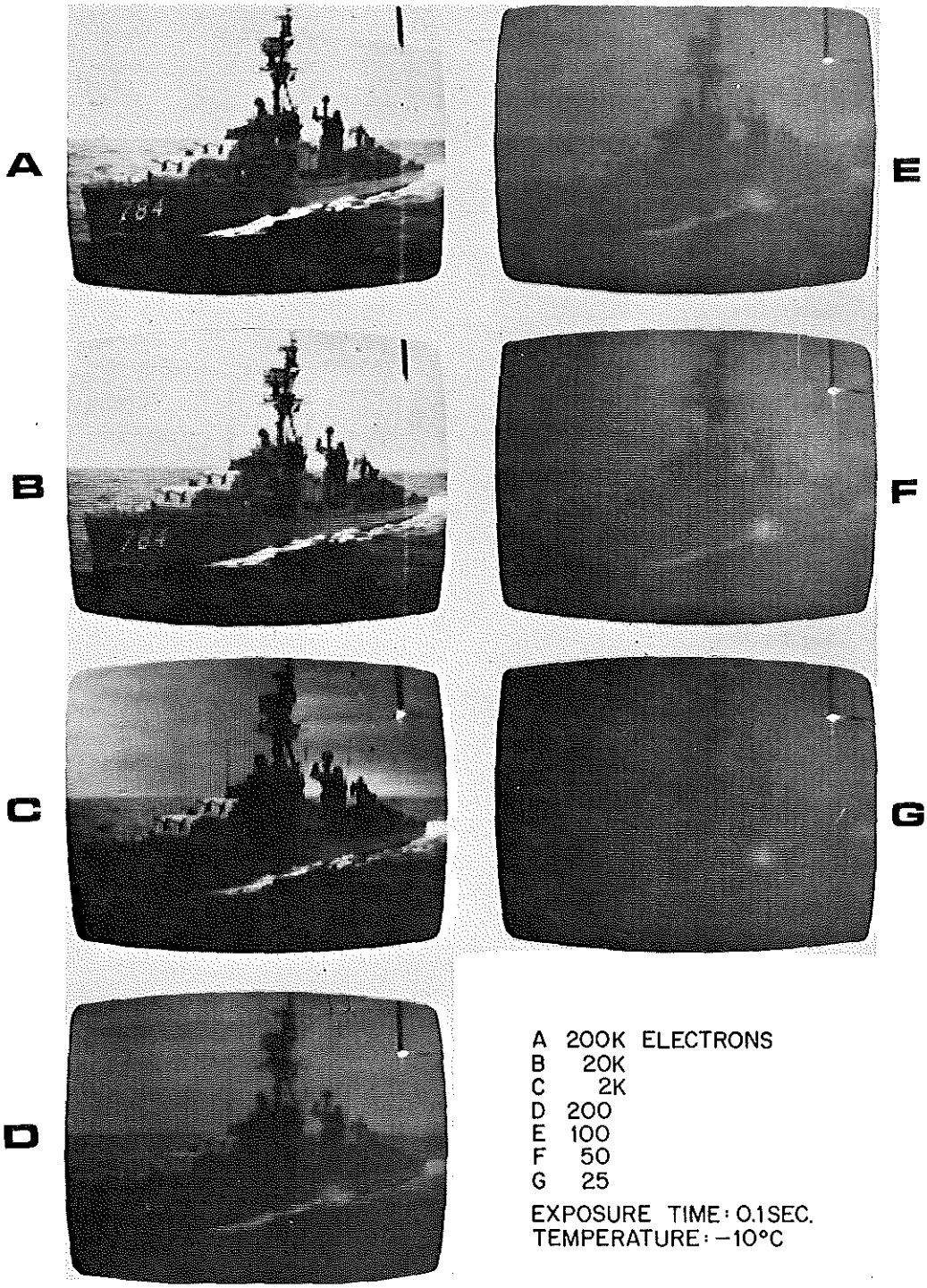


FIGURE 10. PICTORIAL SCENE IMAGING WITH THE DFGA OUTPUT OF A 190 X 244 SENSOR
ELECTRON COUNTS REPRESENT ELECTRONS/PIXEL/FRAME IN IMAGE HIGHLIGHT REGIONS

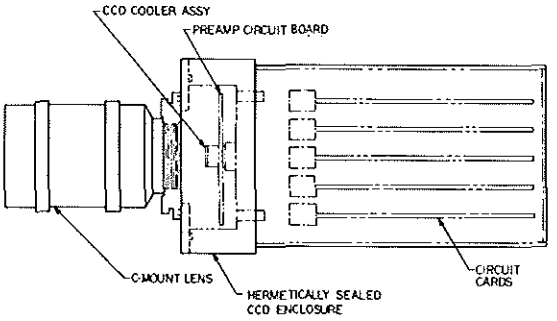


FIGURE 11. LLL-TV CAMERA CONFIGURATION

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