# LOW LIGHT LEVEL PERFORMANCE OF CCD IMAGE SENSORS

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ABSTRACT This paper reports the low light level performance of CCD image sensors. Theoretical limitations of transfer efficiency for small charge packets in CCD shift registers are reviewed. Low noise charge detection techniques are discussed. Specifically, the operation of a distributed floating-gate amplifier (DFGA) is described. A DFGA employs several charge amplifiers which repeatedly sense a signal charge packet in a CCD. The outputs of the charge amplifiers are coherently summed in a second CCD shift register. Signal-to-noise ratio is improved so that extremely small charge packets can be detected.

Low light level imaging performance of both linear and area arrays are reported. The linear array contains 1728 photoelements and uses a single-stage floating-gate amplifier (FGA) as the on-chip detector. The area array has 244 x 190 photoelements and contains a twelve-stage DFGA and an FGA. Both arrays employ two-phase, buried channel CCD shift registers. Low light level images at 50 and 25 electron levels have been achieved with the linear and area sensors, respectively.

## INTRODUCTION

The low light level performance of CCD image sensors is reported in this paper. The basic requirement of transferring a small charge packet in a CCD shift register is considered first. It is well known[1] that in a surface channel CCD shift register, a background charge (fat zero) is required at all times to suppress charge-trapping effects of surface states. The noise[2] associated with the generation of the fat zero makes the surface channel CCD sensor inadequate to perform low light level imaging functions.

In a buried-channel CCD register[3], the signal charge packets are stored and transferred in the bulk of the semiconductor so that surface state trapping can be avoided. However, the signal charge packets may be trapped by the crystalline imperfections in the bulk of the semiconductor. The effect of these bulk traps on charge transfer efficiency plays a dominant role in the low light level performance of buried-channel CCD image sensors. This effect has been analyzed and reported previously by J. Early.[4] Some of his principal assumptions and conclusions are repeated in the first part of this paper. It is shown that signal charge packets of approximately 10 electrons can be transferred in a buried-channel CCD register.

In order to fully exploit the low light level capability of buried-channel CCD image sensors, a special low-noise, high-gain amplifier must be used. Such an amplifier is the distributed floating-gate amplifier (DFGA)[5]. A DFGA employs several charge amplifiers with floating gate inputs to sense repeatedly a signal charge packet in a CCD register. The outputs of the charge amplifiers are summed using a second CCD register. Since the random noise of the charge amplifiers is uncorrelated, the resulting signal-to-noise voltage ratio is enhanced by a factor equal to the square root of the

number of charge amplifiers used. Signal charge packets of the order of 10 electrons can thus be detected. Operation and experimental results of a twelve-stage DFGA are discussed.

Low light level imaging performance of both linear and area arrays are reported. The linear array contains 1728 photoelements. Charge packets in the photosites are transferred in parallel into an adjacent opaque, two-phase, buried-channel, implanted-barrier CCD shift register. A single-stage floating-gate amplifier is positioned at the end of the register to detect the signal charge packets. The area array has 244 x 190 photoelements and employs the interline transfer organization. Signal charge packets from each column are transferred into an adjacent opaque two-phase vertical shift register. The vertical shift register in turn transfers each row of signal charge packets into a two-phase horizontal shift register. The signal charge packets are then transferred along the horizontal register and detected by a twelve-stage DFGA and an FGA. Image resolution and noise performance are examined at different light levels.

## LOW LIGHT LEVEL CHARGE TRANSFER CONSIDERATIONS

In buried-channel CCD image sensors, the signal charge packets may be trapped by crystalline imperfections in the bulk of the semiconductor. The effect of bulk traps and dark current on charge transfer efficiency and signal-to-noise ratio for a hypothetical 500 x 500 element CCD area image sensor, operating in the standard NTSC mode has been analyzed by J. Early. His analysis revealed the following:

1) A reduction in operating temperature reduces dark charge and thereby increases the signal-to-noise ratio.

2) An increase in dark current improves charge transfer efficiency because bulk traps can be filled by dark charges.

3) Under worst-case conditions, for an average dark charge of 10 electrons per pixel and a signal of 10 electrons per pixel, the overall transfer efficiency is approximately 0.8, and the signal-to-noise voltage ratio is 1.4.

4) Bulk trapping is of consequence only in long registers operating at conventional television horizontal line repetition rates of 15 .75 KHz.

5) Transfer efficiency and signal-to-noise ratio are excellent at the high horizontal transfer rate of 5MHz.

Charge transfer efficiency of a 15-electron charge packet in a two-phase buried-channel CCD was measured, using statistical methods.[6] The device was cooled to obtain an average dark charge of 4 electrons per pixel. It was observed that after 238 transfers at a 15.7 KHz clock rate, approximately one electron was lost. This data confirms the theoretical analysis that in a buried-channel CCD shift register there is useful transfer efficiency after 500 transfers in a signal charge packet of approximately 10 electrons.

## DISTRIBUTED FLOATING-GATE AMPLIFIER (DFGA)

In a CCD register, the signal charge packet can be detected by a sensing "floating-gate" electrode as shown in Figure 1. It can be seen that the floating gate provides a capacitive coupling between the signal charge packet in the CCD register and the current in the MOS channel without making physical contact with either of them. Since the signal charge packet is not destroyed by the floating gate, it can be transferred along the CCD register and be detected repeatedly by similar structures. In a DFGA[5], the outputs of several floating-gate structures are summed with a

second CCD register. The signal-to-noise ratio of the summed output is enhanced so that extremely small charge packets can be detected.

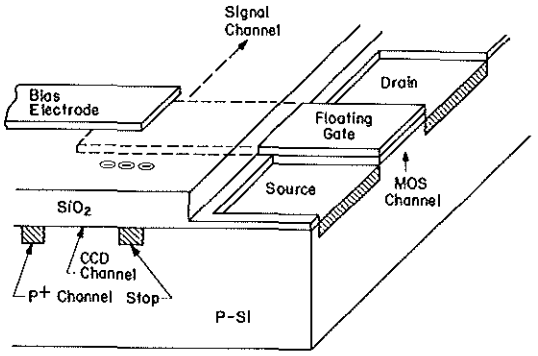



FIGURE 1 Schematic of FGA.

A schematic diagram of a twelve-stage DFGA is shown in Figure 2. It consists of an input register, a bank of twelve charge amplifiers with floating-gate inputs, an output CCD register, and an output amplifier. A signal charge packet is sensed by the floating gates when it is transferred in the input register. The operation of the charge amplifier is illustrated in Figure 3. During the period when the signal charge packet in the input register is under the floating gate, the control gate is pulsed "on" so that a small amount of charge flows into the output register. The magnitude of this charge is determined by the signal charge in the input register through the coupling of the floating gate. This is a charge inverting amplifier in the sense that the larger the signal charge in the input register, the lower the floating gate potential, and the less the charge that flows into the output register. A dc gate is used to eliminate clock coupling from the control gate to the floating gate.

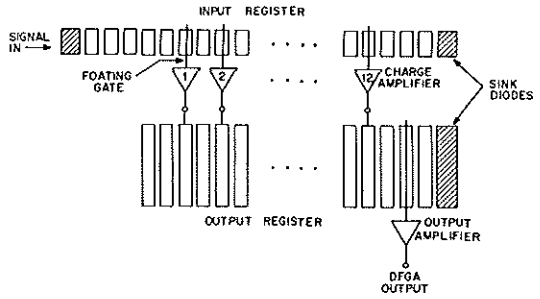



FIGURE 2 Schematic of DFGA.

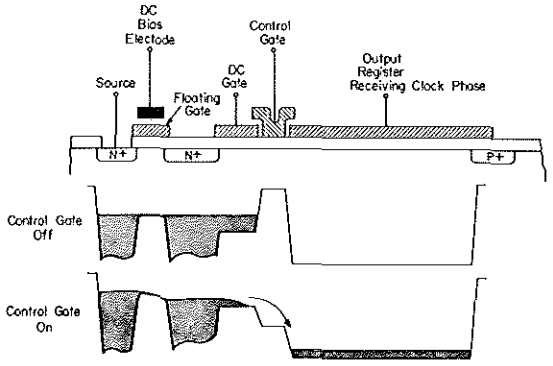



FIGURE 3 Charge amplifier in DFGA.

The operation of a DFGA can be illustrated by considering a hypothethical three-stage structure. Figure 4(a) illustrates the initial charge distribution in the DFGA after a long series of empty charge packets have been transferred along the input register. Figure 4(b) shows that one clock cycle later ($t = t_c$) a large charge packet D has been transferred under the floating gate of the first charge amplifier stage. After the control gate has been pulsed "on" a small amount of charge D' is injected into the output register. Figure 4(c) shows that at $t = 2t_c$, charge packet D has been transferred under the floating gate of the second charge amplifier stage while charge packet D' in the output register has also been

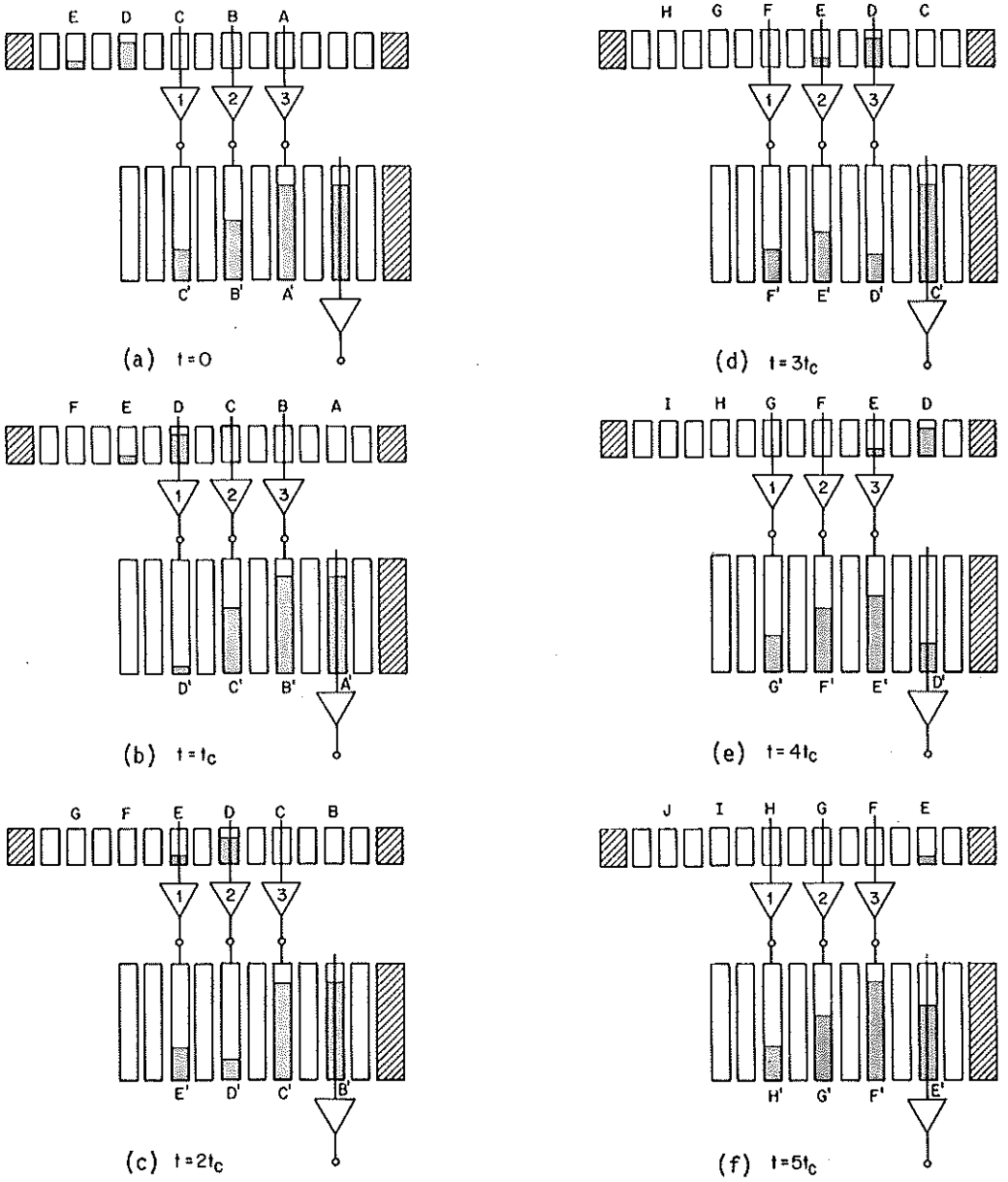



FIGURE 4 Charge distribution in DFGA.

transferred to the corresponding position. After the control gate is pulsed "on", another small amount of charge is added to the charge packet D'. Figure 4(d) illustrates the charge distribution at $t = 3t_c$. At $t = 4t_c$, the charge packet D' has been transferred to the output amplifier where it produces the final DFGA output. Charge packets E and E' in the same sequence illustrate the situation when a small charge packet is transferred along the input register. At $t = 5t_c$, charge packet E' is detected by the output amplifier.

The DFGA output waveform is illustrated in Figure 5. The DFGA output at $t = 4t_c$ corresponds to the initial charge packet D. For zero initial charge in the input register, a maximum amount of charge is injected into the output register. The corresponding output is $V_{BIAS}$. The signal output for charge packet D which is the difference between the DFGA output and $V_{BIAS}$, is designated by $V_S$. The DFGA output at $t = 5t_c$ corresponds to the small charge packet E in the input register.

Twelve-stage DFGA test structures have been built and tested. A typical transfer characteristic curve for a 50nsec control gate "on" time, $t_{on}$, at 3 MHz bandwidth and room temperature is plotted in Figure 6. The smallest signal level measured is approximately 30 electrons. The RMS Noise measured is 10 to 20 electrons.

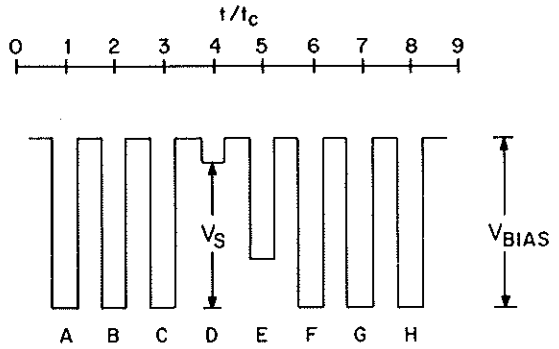



FIGURE 5 DFGA output waveform.

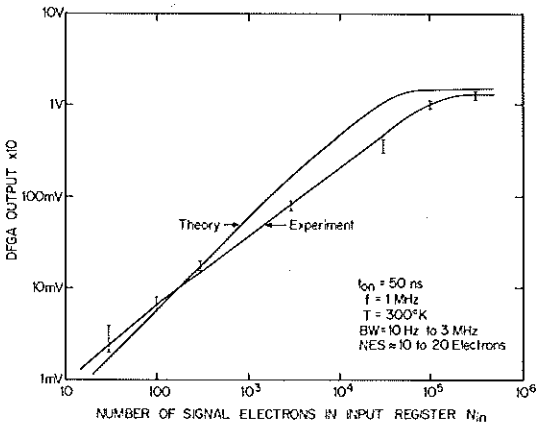



FIGURE 6 DFGA characteristics.

## EXPERIMENTAL RESULTS OF CCD IMAGE SENSORS

### Linear Image Sensor

A block diagram of the 1728-element interlaced linear image sensor is shown in Figure 7. It consists of an array of 1728 photosites, a two-phase CCD shift register, and a single-stage floating-gate amplifier. An opaque aluminum layer is deposited over the device to block incident light except in the photogate $\phi_p$ area. A positive dc voltage is applied to the photogate to collect the signal electrons in the potential wells formed. The 1728 photosites under the photogate are defined by the p-type channel-isolation diffusion shown in this figure. The center-to-center spacing of these photosites is 13μm.

At the end of an integration period, the transfer gate $\phi_X$ is pulsed "high" to transfer the signal electrons in two fields into the neighboring two phase CCD shift register. The signal electrons are then transferred along the shift register and detected by the single-stage floating-gate amplifier. A sink diode and exposure control gate $\phi_{EC}$ are incorporated to provide exposure control and antiblooming functions(7). The CCD

shift register is constructed using two layers of polysilicon with self-aligned ion-implanted barriers[8] as shown in Figure 8. The buried channel is accomplished with the ion-implanted N-layer.

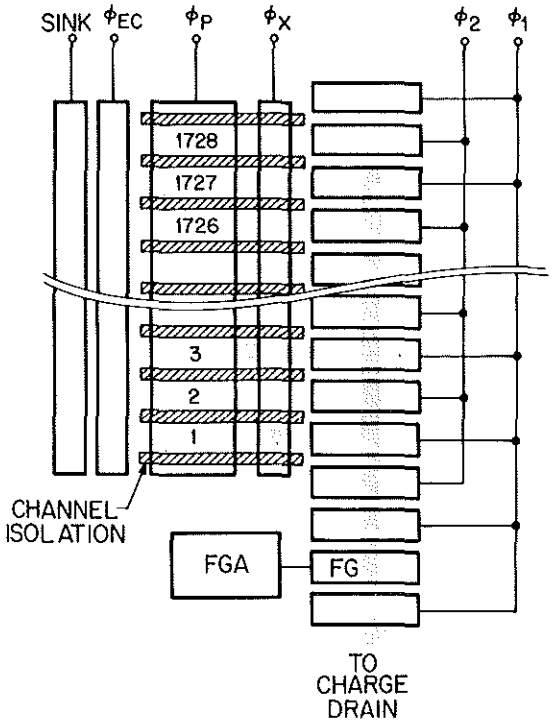



FIGURE 7 A 1728-element linear sensor.

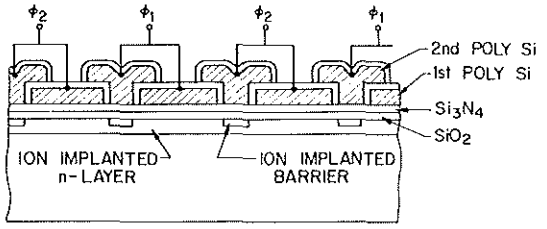



FIGURE 8 Two phase CCD structure.

A CRT monitor display of the IEEE Facsimilie Test Chart is shown in Figure 9. The image was horizontally scanned by the image sensor, while vertical scanning was obtained by mechanical rotation of the test chart. A portion of this displayed image is also shown with an expanded monitor sweep. The maximum resolution obtained is approximately 36 line parts/mm.

Low light level performance of this image sensor is illustrated by the photographs in Figure 10. This series of single-frame photographs show the display of approximately 700 photosites at illumination levels successively reduced from near saturation. The ambient temperature was 25°C and the clock rate was 1.5MHz. The high-light area in Figure 10(a) represents an illumination of 200μW/cm$^2$ with a maximum charge per photosite of approximately 500,000 electrons. At a 1/1000 reduction in light intensity, a high-quality image is retained although some dark current spikes appear as vertical streaks. At a 1/10000 reduction in light intensity, the brightest area in the picture represents approximately 50 electrons per photosite. The dark charge per pixel is approximately 800 electrons, resulting in a dark charge noise of 28 electrons. The noise-equivalent-signal per pixel in Figure 10(e) is approximately 100 electrons. The low light level performance of this sensor is therefore limited by the noise in the amplifier.

Area Image Sensor

A photograph of the 244 x 190 area image sensor [9] is shown in Figure 11. This device employs the interline transfer organization where the signal charge packets are read out in two successive fields. In operation, signal charge packets are generated and stored under the 190 vertical photogates. At the end of an integration period the photogates are pulsed "low" to transfer the signal charge packets from half of the photosites into an adjacent opaque two-phase vertical shift register. The vertical shift register in turn transfers each row of the signal charge packets into a two-phase horizontal shift register. The signal charge packets are then transferred along the horizontal register and detected by the output amplifiers. After all the signal charge

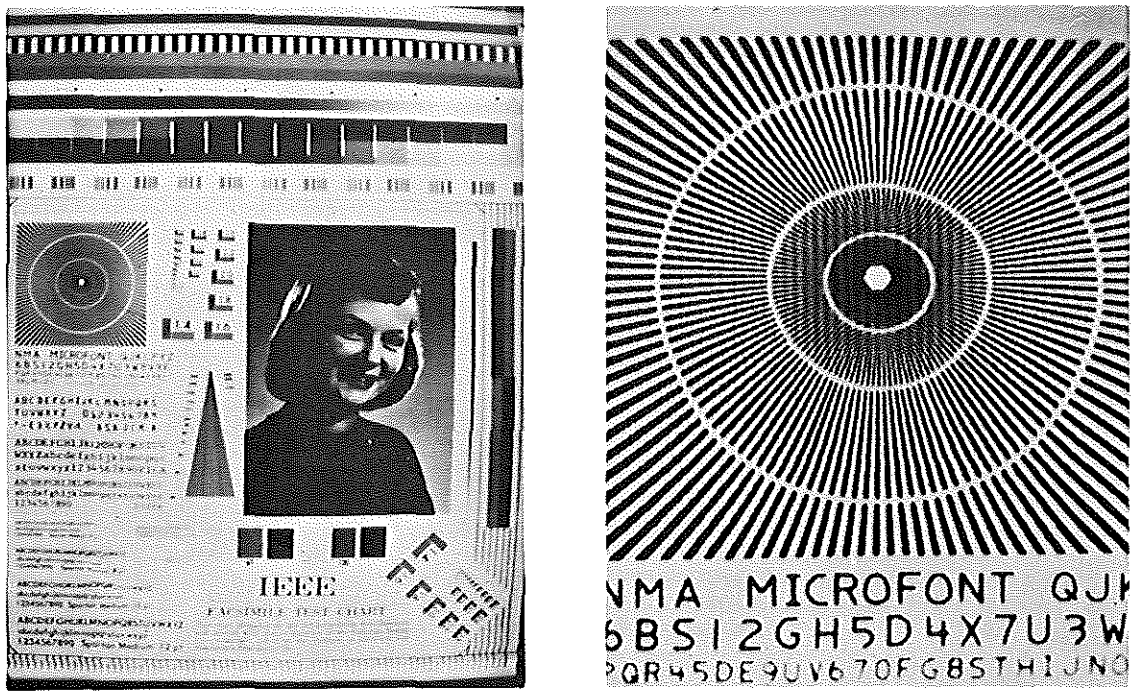



FIGURE 9 Image of linear sensor.


| (a) | (b) | (c) | (d) | (e) |
|---|---|---|---|---|
| 500K Electrons | 50K Electrons | 5K Electrons | 500 Electrons | 50 Electrons |

FIGURE 10 Imaging performance of linear sensor.

packets have been detected, the process is repeated to read out the signal charge packets from the remaining photosites. Both the vertical and horizontal shift retisters are two-phase, buried-channel structures identical to that shown in Figure 8. The photoelement center-to-center spacing is 30μm horizontally and 18μm vertically.

This device employs a twelve-stage DFGA, and a single-stage floating-gate amplifier similar to that used in the linear image sensor described earlier. A photograph of the DFGA area is shown in Figure 12. This DFGA is identical to the twelve-stage DFGA test structure described in Section III, except that the structure of the output register has been modified.

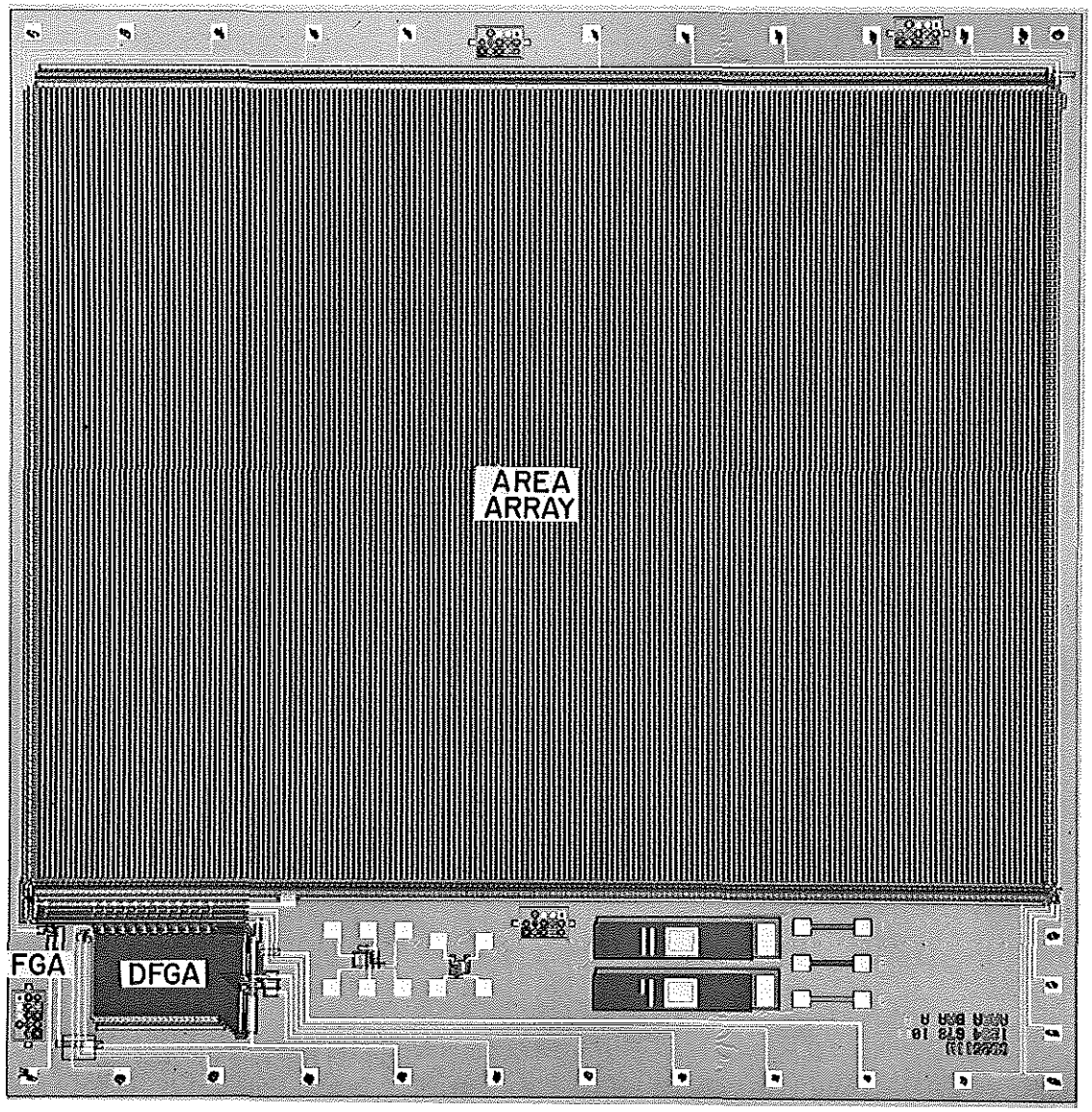



FIGURE 11 Photograph of the 244 x 190 area sensor.

It can be seen that the output register separates into two parallel registers after the twelfth charge amplifier stage. An output amplifier is provided at the end of each register, one being delayed from the other by one half horizontal clock period. By summing these two outputs off chip, the large output swing $V_{BIAS}$ can be cancelled, as illustrated in Figure 13 and the resulting waveform can be much more easily processed. A theoretical analysis indicates that the noise equivalent signal of this DFGA is approximately 17 electrons at room temperature and 3 MHz bandwidth.

A block diagram of the imaging test set-up is shown in Figure 14. The regular and delayed DFGA outputs are combined to remove $V_{BIAS}$ in the output waveform. The output is amplified and then dc restored during each horizontal blanking period with the line clamp circuit. It is amplified again and displayed on a monitor.

Low light level imaging performance of this sensor is illustrated in Figure 15. These photographs show DFGA images at $-10^{o}C$. The horizontal clock frequency was 2MHz, resulting in a frame rate of 23 frames/sec. The light integration time was 43 msec. The width of the coarse bars is 120μm, and the width of the fine bars is 60μm on the CCD image plane. Figure 14(a) shows the image at a near saturation exposure of approximately 4.7 $\mu W/cm^2$. The bright areas in this photograph contain approximately 200,000 electrons per photoelement. Figure 15(b) and (c) show the same image when the

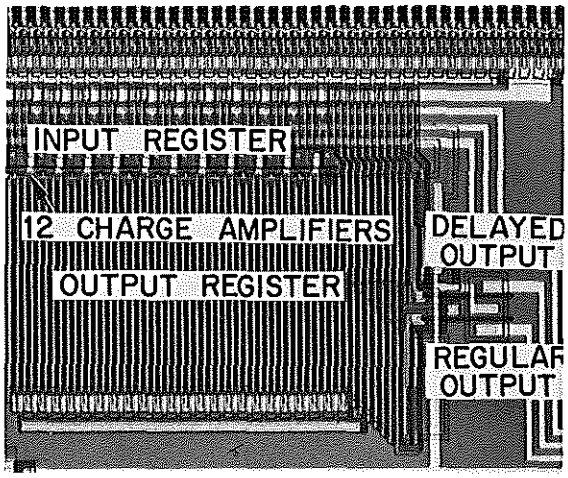



FIGURE 12 DFGA on the area sensor.

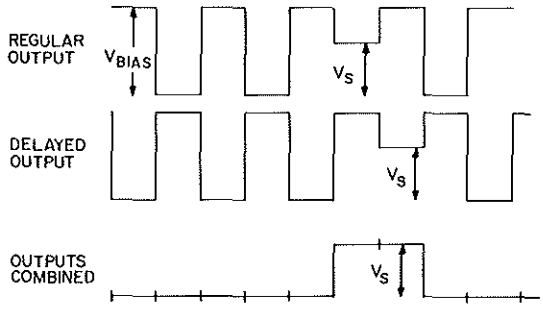



FIGURE 13 Modified DFGA output waveform.

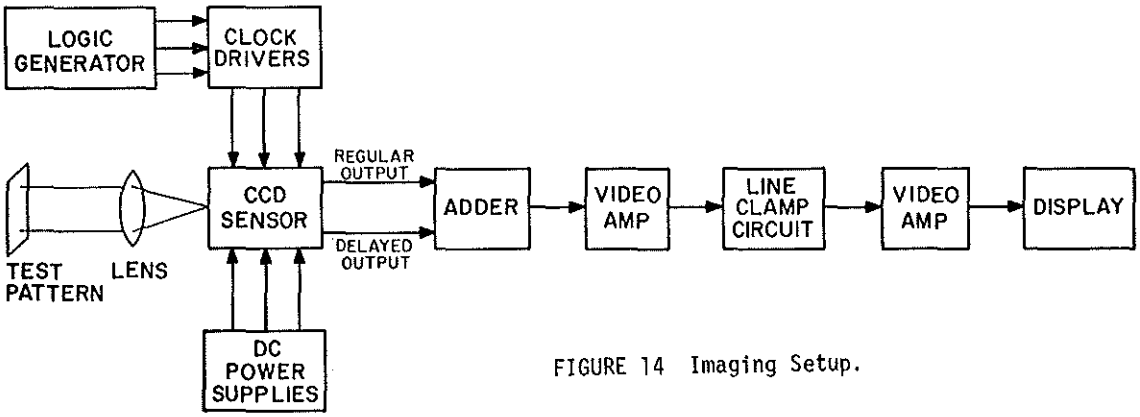



FIGURE 14 Imaging Setup.

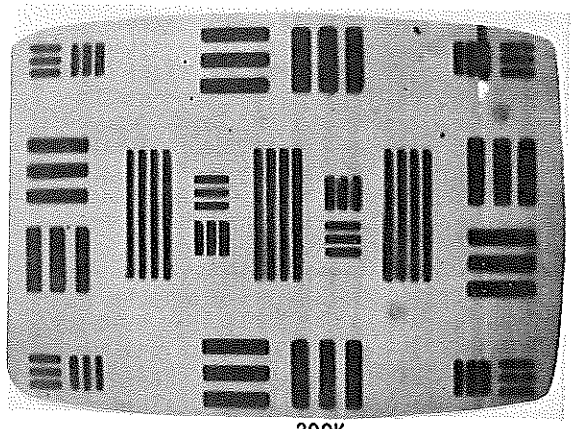
light level is reduced by a factor of 1000 and 8000, respectively. At the 1/8000 reduction in light level, there are approximately 25 electrons per photoelement. A good transfer efficiency is maintained. The coarse (1/4 Nyquist) bars are visible and some of the fine (1/2 Nyquist) bars can also be recognized. Noise-equivalent-signal per pixel is probably 2 to 3 times higher than the 10 to 20 electron level which is predicted and measured on separate DFGA test structures.

At -10°C, the dark charge per pixel is approximately 1000 electrons. The dark charge noise should be approximately 32 electrons. The dominant noise source in Figure 15(c) is not the dark charge noise since it can not be reduced by cooling the array further. The limiting factor of the low light level performance of this array is not known. The most probable sources are the noise on the clock drivers, power supplies, and signal processing circuits.

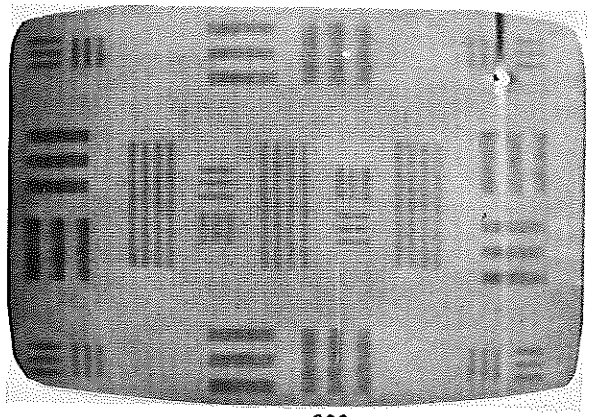
## CONCLUSION

The low light level performance of CCD image sensors have been examined. An analysis of bulk trapping indicates that signal charge packets of ten electrons can be transferred in large buried-channel CCD sensors operating at the NTSC mode. 1728-element linear arrays and 244 x 190-element area arrays both showed excellent transfer efficiency at signal levels well below 100 electrons. Using a twelve-stage DFGA, the area image sensor has demonstrated half Nyquist limit (60μm width) bar images at a signal level of approximately 25 electrons at -10°C. The corresponding irradiance was $6 \times 10^{-4}$ μW/cm$^2$, and the integration time was 43 msec.

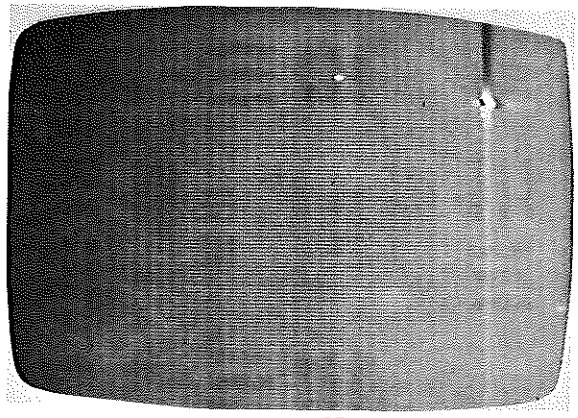
Separate measurements on twelve-stage DFGA test structures have shown noise level of 10 to 20 electrons. Actual images obtained with the DFGA on the area array, however, showed 2 to 3 times higher noise per pixel. The dominant noise source is suspected in the external supplies and signal processing circuits rather than in the sensor itself. It is expected that a factor of 2 to 3 improvements in the lwo light level imaging performance can be achieved with the present CCD sensors by improving the external supplies and signal processing circuits.



(a) 200K Electrons



(b) 200 Electrons



(c) 25 Electrons

FIGURE 15 Imaging performance of area sensor.

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