A HIGH PERFORMANCE 190 x 244 CCD AREA IMAGE SENSOR ARRAY

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ABSTRACT: The first of a new generation of buried channel CCD area image sensors based on a gapless silicon-gate technology has been developed. The first product to be completed is a 190 x 244 element device which is the successor to a similar device previously developed in undoped polycrystalline silicon isolation technology. In addition to the area array, which uses the interline transfer system, the device includes a floating gate output amplifier, a distributed floating gate output amplifier, two electrical inputs and a column antiblooming structure. The device has been operated at data rates greater than three times the design center of 7 MHz. At low light levels images of half Nyquist frequency bar patterns have been observed at signal levels of less than 30 electrons.

INTRODUCTION

A new generation of processing technology has been applied to an improved design of a 190 x 244 element Charge Coupled Area Imaging Device (CCAID). This device, the AID244 is a member of a family of CCAID's which have been developed during the past two years, using the interline transfer system and undoped polycrystalline gate isolation technology. In this paper the design aspects, processing technology, antiblooming characteristics and low light level performance of the device will be discussed.

DEVICE DESIGN

The front side illuminated area array using the interline transfer system[1] has been retained in the design of the new device family. One hundred ninety columns of 244 elements alternating with optically insensitive vertical shift registers, form the array of the AID244 device. Two other members of the new family of gapless technology devices are currently in development. A gapless version will supersede the Fairchild CCD201, a 100 x 100 element device, introduced almost two years ago. A larger device designed with 380 columns of 488 elements is being developed for full frame NTSC TV compatible performance.

The overall organization of the AID244 is shown in Fig. 1. The optically sensitive area of the array, detailed in Fig. 2 has an aspect ratio of 4:3. A diagonal of 7.2 mm makes the device compatible with lenses designed for the super 8 mm format. The photoelement cell size is 14 μm x 18 μm with 4 μm of vertical overlap in the channel stop and 16 μm of horizontal separation due to the interleafed vertical shift registers. These dimensions are compatible with the resolution and alignment capabilities of the fabrication process developed for this family of devices. The output signal format provides two interlaced fields of line sequential information in conventional left to right, top to bottom TV sequence. Two output amplifiers are provided in the AID244 design. A single stage floating gate amplifier (SFGA) provides an output level of 300 mV into a 510 Ω load for near saturation level signals at the 7.16 MHz

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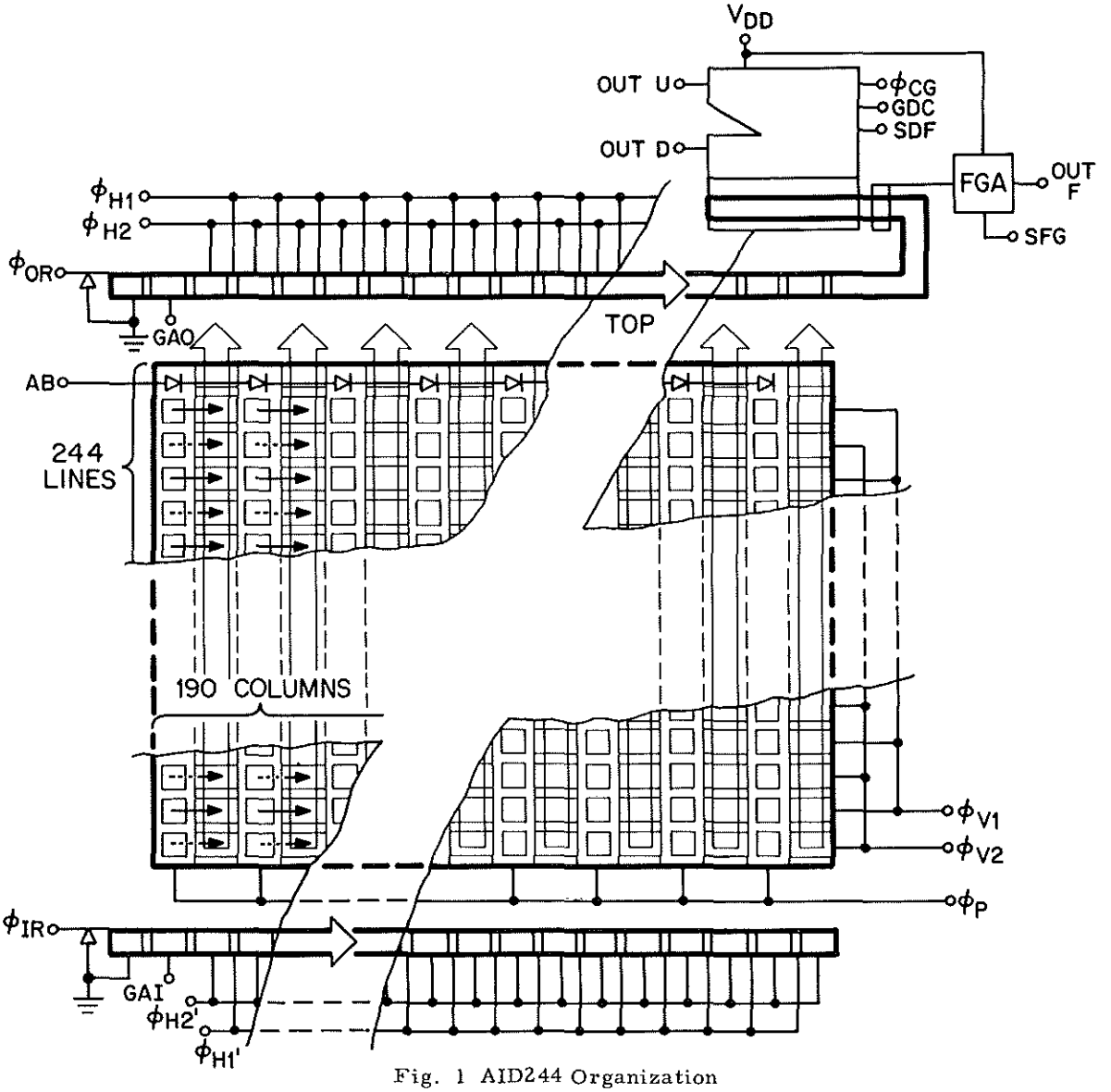

Fig. 1 AID244 Organization

data rate. The floating gate amplifier design was chosen for the AID244 because it provides a video signal free from reset noise and operates with a random noise level of less than 10^2 electrons.[2] A twelve state distributed floating gate amplifier (DFGA) is provided for very low light level applications. The DFGA features two outputs, one of which is delayed from the other by half a horizontal clock period. By summing these outputs off chip, clock voltage components in the video output are cancelled. Details of the amplifier design are discussed in another paper presented at this conference by D. Wen.

Two linear electrical input circuits are used in the AID244 design, one associated with the input shift register and the other with the horizontal shift register. The latter is intended primarily as a test tool

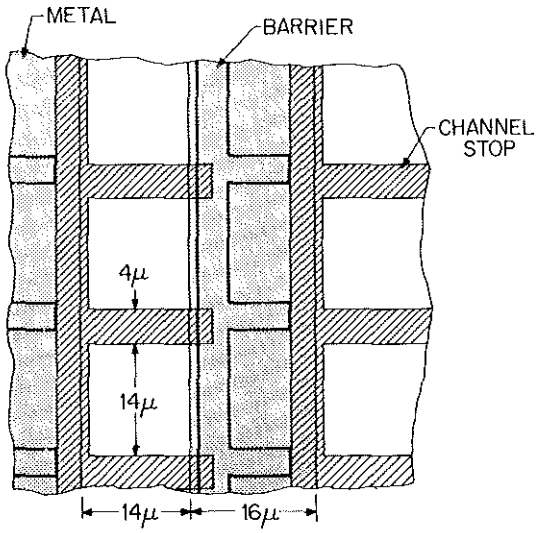

Fig. 2 AID244 Area Array Detail

for calibrating the DFGA signal level, while the former is intended for application of the device as an SPS analog shift register. Both input transducers are identical in design, and are represented

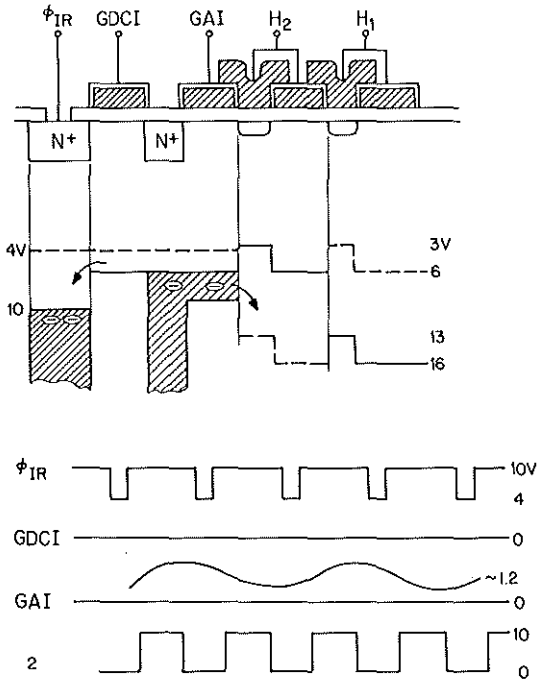

Fig. 3 AID244 Input Structure

by the cross section in Fig. 3. This is similar to the input system referred to by Tompsett[3] as the charge equilibration method, in which the input source (ØIR) is pulsed to a low voltage to inject charge across a barrier formed under GDCI, the DC control gate. Then the source is reversed biased and drains back the excess charge. The input signal is impressed on the analog input gate (GAI) and controls or modulates the flow of charge to the channel. Fig. 4A shows input and output ramp excitation waveforms. The full signal range linearity from the input register to the output is shown in Fig. 4B. Approximately 1500 mV of input signal swing is required to achieve the maximum linear output signal. The nonlinearity for 90% saturation is less than 3%.

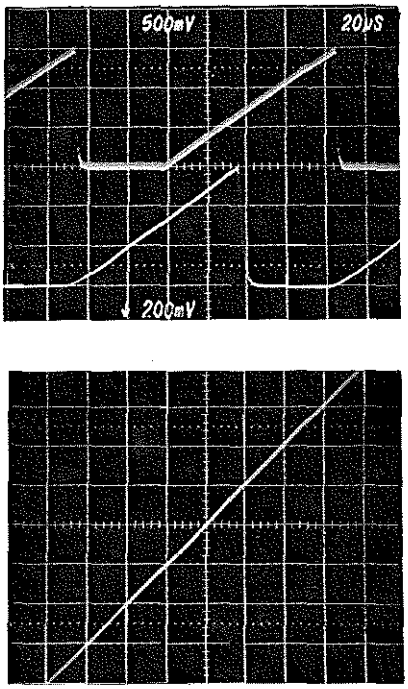

Fig. 4 Electrical Input Characteristics

FABRICATION TECHNOLOGY

The performance of CCAID's, particularly at low light levels, is strongly influenced by the fabrication technology employed. Buried n-channel technology is used for all Fairchild CCAID's, i. e., an n-type layer is ion implanted in a p-type substrate. P+ doped channel stops define the photosite regions and the CCD register channels. The photoelectron

charge packets are moved within the bulk silicon, away from the silicon-silicon dioxide interface. Since they do not contact surface states at the interface, a fat zero charge, which is needed in surface-channel devices to obtain high transfer efficiency, is not required in this technology. Furthermore, the location of the channel in the bulk of the silicon subjects the photoelectrons to a stronger horizontal component of the clock electrode field than it has near the surface. This fringe field aids carrier transport and results in improved transfer efficiency, particularly at high frequencies. The transfer efficiency of the AID244 at a 20 MHz data rate has been measured to be 0.9998.

Undoped polycrystalline silicon gate isolation technology previously applied to similar CCAID's has been replaced by gapless technology in the AID244.

Two principal advantages are attained with the gapless polysilicon gate isolation technology of Fig. 5, which uses two levels of polysilicon to form the gate electrodes. The first level of polysilicon is deposited on the gate dielectric over the substrate which already contains the N-channel but no implanted barriers. This layer is patterned to form the V_1 and V_2 electrodes over the non-barrier sections of the channel. The barrier implant, following next in the fabrication cycle, is masked by these electrodes, providing truly self aligned barriers for 2 phase shift register operation.[4] A second layer of polysilicon is subsequently used to form the electrodes over barrier sections of the channel. This self alignment of the barrier to the gate electrodes eliminates potential well irregularities caused by misalignment of the gates with respect to the barrier in the undoped gate isolation process. Potential well irregularities due to the misalignment have caused poor transfer efficiency at low signal levels and at high operating frequency in devices manufactured with undoped polysilicon isolation technology. In the gapless polysilicon isolation technology silicon oxide provides the electrical isolation between gate electrodes, whereas undoped polysilicon provided this function in the older technology. The insulating characteristics of silicon oxide are superior to those of undoped polysilicon, particularly after subsequent high temperature processing cycles required to fabricate the device. Reductions in gate to gate shorts and leakage have been observed on devices manufactured with the new technology.

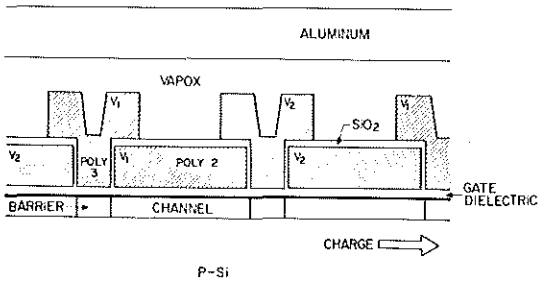

Fig. 5 Gapless Polysilicon Gate Isolation Cross Section

BLOOMING SUPPRESSION

A column antiblooming technique has been successfully applied in the design of the AID244. The function of the antiblooming structure is to prevent excess carriers generated by overexposure of one or more photosites in a column from spreading to

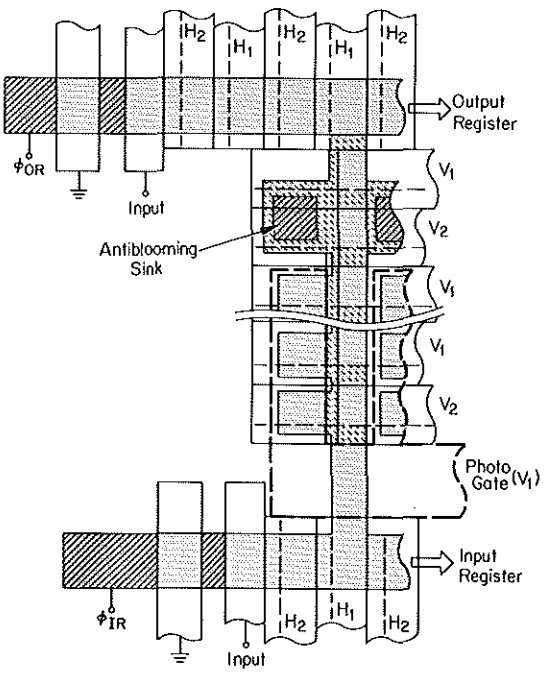

Fig. 6 Blooming Suppression Structure

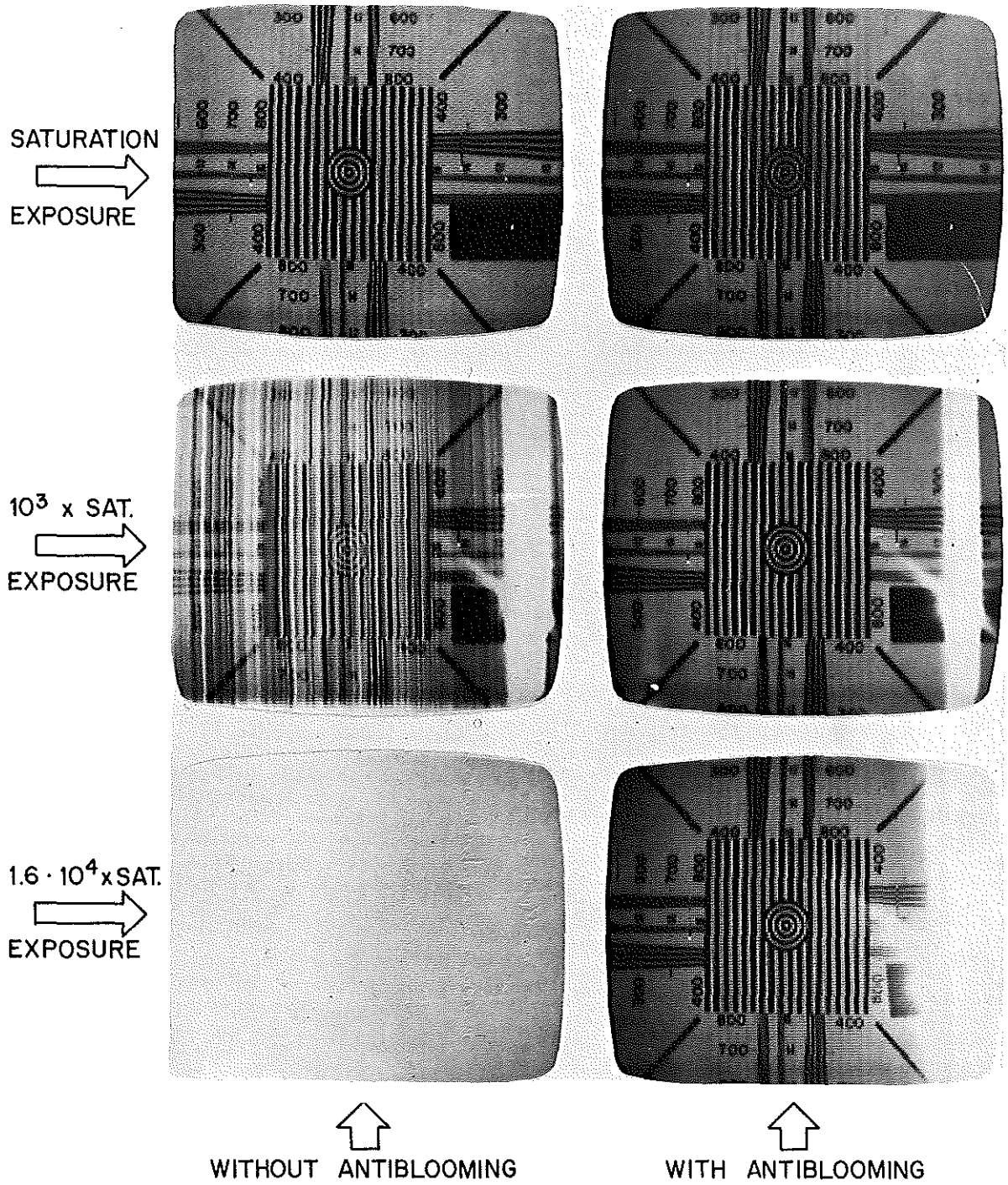

Fig. 7 Blooming Suppression Characteristics

adjacent columns. A sink for excess carriers is provided at the top and bottom of each vertical shift register, as shown in Fig. 6. At the top, above the last photosite, between the horizontal output register and the area array, a line of N+ regions is diffused into the structure. These N+ carrier sinks are electrically separated from the vertical shift register by a barrier. The N+ regions are connected together by metallization and connected to the antiblooming terminal. When an appropriate positive bias is applied to the antiblooming terminal, any carriers exceeding the barrier potential will be removed before they can reach the horizontal output register, where lateral spreading would occur. At the bottom of each column the horizontal input register, appropriately biased, provides a similar sink. In Fig. 7 the device performance with and without blooming suppression is compared. The intensity of a light spot approximately six elements wide was varied from near saturation to 10^3 times saturation and 1.6×10^4 saturation. At 10^3 times saturation severe image degradation occurred over the entire picture area without blooming suppression; with antiblooming bias applied, the image degradation was limited to about 10% of the picture area. At 1.6×10^4 times saturation exposure the device was completely flooded without antiblooming, while 75% of the image remained unaffected with antiblooming. Some evidence of lens flare is evident in Fig. 7, causing the diagonal white streaks emanating from the fiberoptic light source used to generate the overload image.

LOW LIGHT LEVEL PERFORMANCE

Low light level performance of the AID244 has been demonstrated under a variety of conditions. Application of the device to low light level cameras and results obtained are reported in a paper by K. Hoagland and H. Balapole at this conference.

In all cases custom designed electronic systems consisting of drive electronics and video processors were used. Details of these systems are beyond the scope of this paper but it must be emphasized that careful attention to both systematic and random noise is essential to avoid shading and noise patterns and to minimize random noise.

In all tests, the calibration technique was based on the measurement of output register current for images near the saturation charge level of 3×10^5 electrons per pixel. Single neutral density filters and lens diaphragm settings were used to reduce the image intensity. Room temperature and cooled measurements have been made using the DFGA output. Images of half Nyquist frequency bar patterns were observed with highlight charge packets of 25 electrons at 0°C. Fig. 8 shows images obtained at -10°C for signal levels ranging from near saturation to 25 electron highlight charge packets. Equivalent images at room temperature required about twice as much signal charge as required at -15°C. The signal level in the 25 electron image of Fig. 8G is less than the noise equivalent signal.

CONCLUSION

The application of gapless polysilicon gate isolation technology to a 244 x 190 element CCAID has improved the low light level performance characteristics of the device, to provide useful images with charge packets of 25 electrons. Fabrication yields obtained with this technology are now making commercial introduction of the device possible.

A new distributed floating gate amplifier provides suppression of clock signals to the video output further enhancing the low-light level performance of the device.

New design features, such as a linear electrical input and column antiblooming are expected to extend the range of applications for this family of devices.

ACKNOWLEDGEMENT

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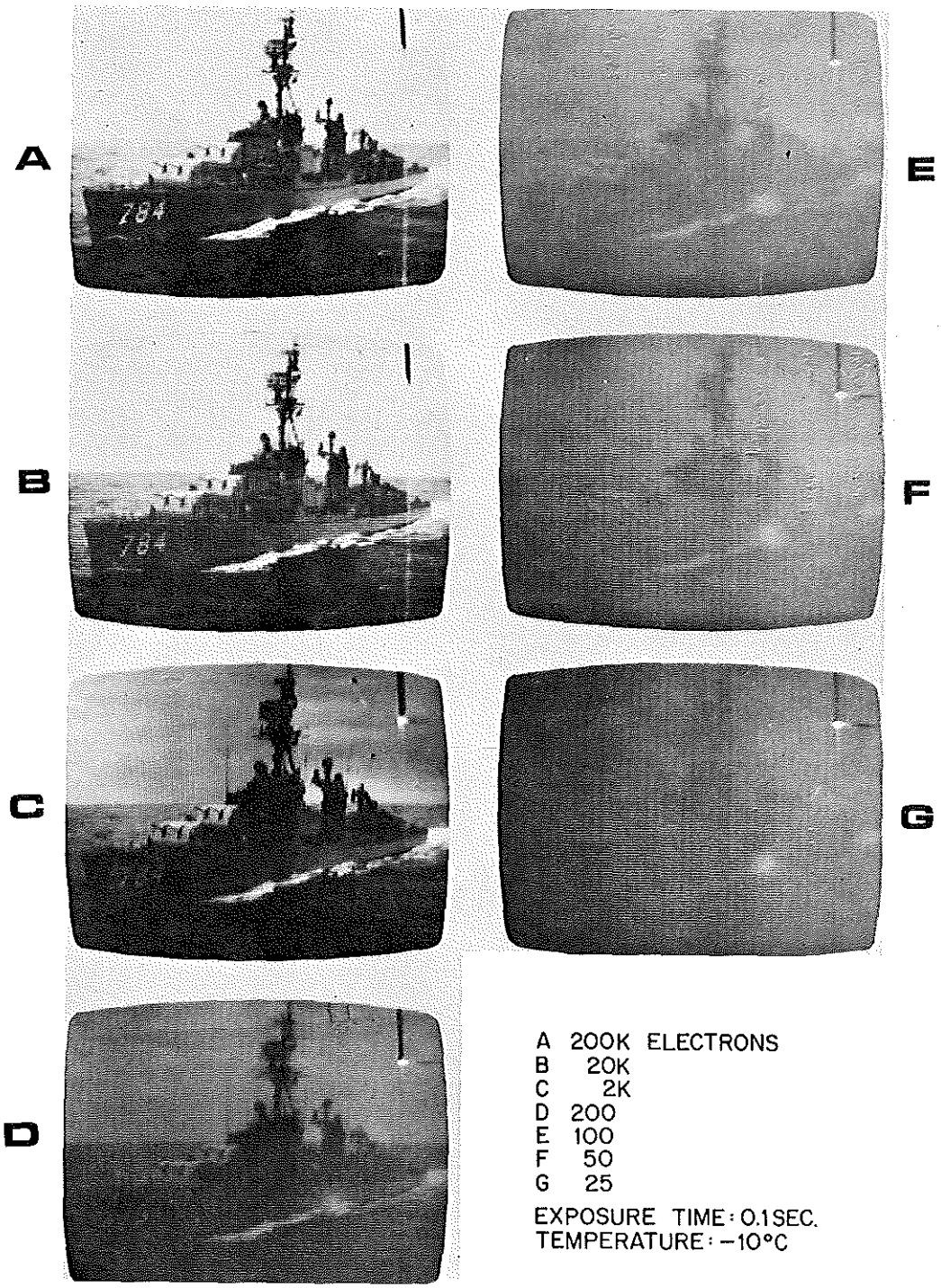

Fig. 8 Low Light Level Performance

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