SERIES-PARALLEL SCAN IR CID FOCAL PLANE ARRAY CONCEPT

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ABSTRACT

A series-parallel scan IR focal plane array concept which uses small InSb CID modules is introduced. The CID is used to premultiplex photocurrent through a preamplifier before the photosignal is introduced into a Si CCD TDI signal processor. An analysis of the expected performance of this configuration suggests that if correlated double sampling is used in the CID readout, a larger f* can be obtained (in the 3-5 μm region) than with most other focal plane array configurations (which use direct injection).

INTRODUCTION

The development of silicon CCD and CID area imaging arrays for $\lambda < 1$ μm has encouraged the infrared community to examine the application of these technologies to infrared focal planes. For terrestial applications the interest is primarily in the development of new kinds of thermal imagers for the 3-5 μm and the 8-12 μm atmospheric windows. We expect that the use of CCD's at or near focal plane will permit the use of thousands of IR detectors in a focal plane at reasonable cost. If these future focal plane arrays (F.P.A.'s) succeed in being limited by statistical fluctuation in background flux (background limited) a signal-to-noise ratio improvement proportional to the square root of the number of detectors can be expected compared to present systems assuming other design parameters remain constant. This paper will concentrate on the problems associated with obtaining background limited performance with F.P.A.'s operating in the 3-5 μm region.

CCD and CID structures can be fabricated in materials sensitive to infrared radiation however CCD and CID structures which are appropriate for the visible and very near infrared are not necessarily appropriate for thermal imaging systems. Because of the low contrast of thermal imagery a DC coupled staring sensor would have difficulty distinguishing between variations in detector responsivity and variations in image irradiance. For example net detector to detector responsivity uniformity in an unscanned array would need to be better than 0.35% in the 3.4-5.1 μm band in order not to compete with apparent target temperature differences of 0.1°C.

The use of area arrays in a mechanically scanned series-parallel configuration using time delay and integration (TDI) and an effective AC coupling of the detector with the image avoids these stringent uniformity requirements. Also TDI provides built in redundancy in that a few dead detectors can be tolerated without significantly degrading the imagery.

The technical approach to a high packing density array for series-parallel scan which to date has received the most investigation mates conventional InSb photodiodes with a Si CCD chip to form a InSb photodiode Si CCD sandwich focal plane module. (See Fig. 1).[1,2] Several modules would be used to form a focal plane of thousands of detectors. With this approach each detector is individually connected to a direct injection input circuit which inputs photocurrent into a silicon TDI CCD register. This method of inputting photocurrent into a Si CCD requires a connection for each detector and has certain signal-to-noise limitations which will be discussed

later. Preamplifiers between the detector and the CCD have not been used to date due to packing density considerations.

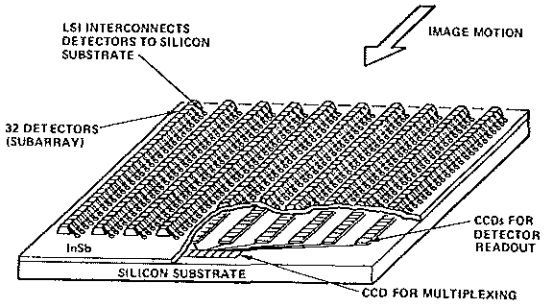

FIGURE 1 - Sandwich/direct injection IR focal plane array using IR photodiodes and Si CCD TDI registers.

As an alternative to the sandwich/direct injection F.P.A. structure discussed above we propose the approach series-parallel scan with InSb shown in Fig. 2 which is based on the CID in InSb developed by Kim.[3] The CID in effect premultiplexes the photocurrent through a preamplifier before it is demultiplexed and inserted into Si CCD TDI registers. High transfer efficiency in the InSb is not required since an x-y readout can be implemented. Connections must be made to the x-y readout lines on the CID module, but for the 400 detector module size suggested in Fig. 2 this is only 0.1 interconnect per detector. The CID modules must be read out more than once per dwell time leading to high clock frequencies, but the premultiplexing feature allows the use of a small number of high quality preamplifiers before intorudiction of the signal current into the CCD TDI signal processor. This can lead to improved signal to noise performance over direct injection as will be explained later. "Background rejection" equivalent to A.C. coupling would be provided at the TDI output as with the sandwich/direct injection structure.

OPERATION OF SERIES PARALLEL SCAN CID

Operation of the focal plane shown in Fig. 2 can be understood by reference to Fig. 3. With the arrangement shown in Fig. 3, each CID detector which integrates photogenerated charge is read out sequentially at a rate such that the entire CID module is read out in the time the image moves a distance y/2 on the focal plane where y is the detector center to center spacing.

When detector 5A is read out gate A° is closed and the amplified signal charge is fed into CCD well 1A'. When detector 5B is read out gate B° is closed and the amplified charge is fed into CCD well 1B'. Before detector 4A is read out the charge in 1A' is transferred to 2A' to make room for the charge from 4A. This process continues until the entire CID module is read out and an amplified replica of the signal from detector 1A, 2A, 1B, 2B, etc., is stored in CCD wells 1A', 2A', 1B', 2B'. At that point, the transfer gates are opened and the charge

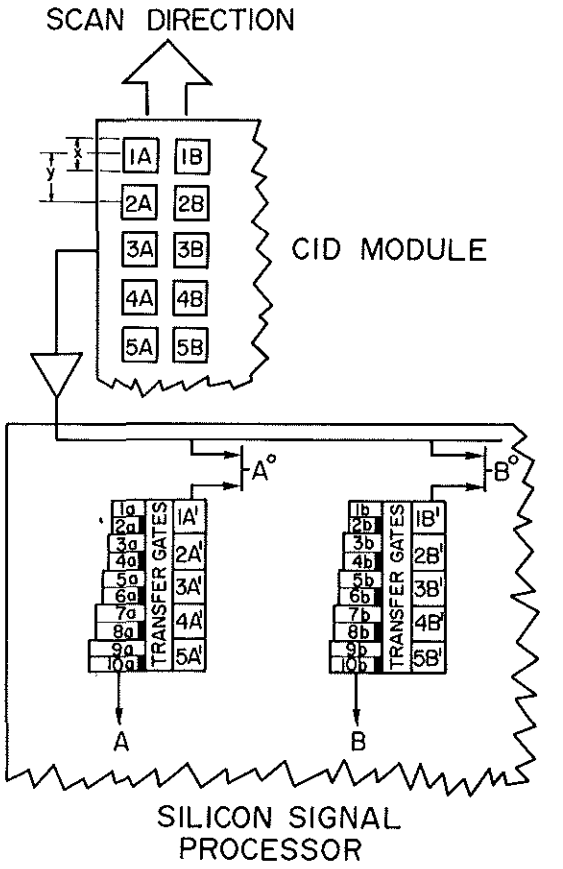

FIGURE 3 - Schematic of the CID module and the Si TDI signal processor used for series parallel scan.

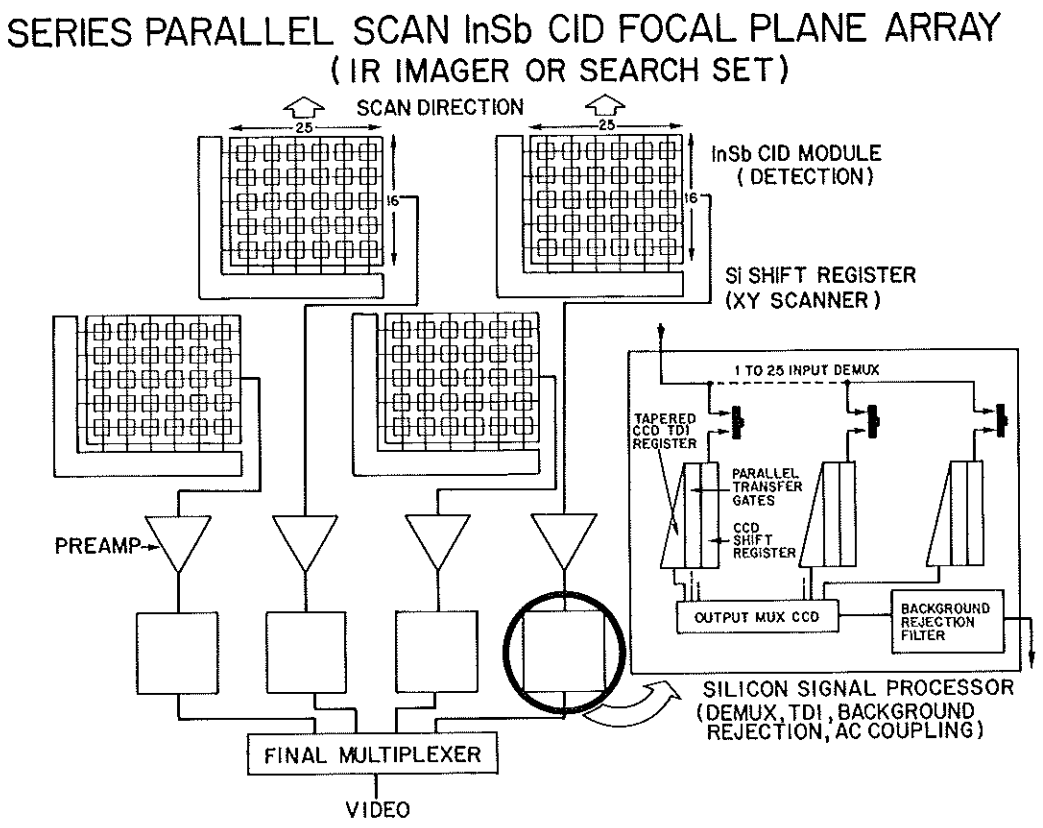

FIGURE 2 - Series-Parallel Scan CID focal plane array concept.

in 1A' is transferred to 1a at the same time thatcharge in 2A' is transferred to 3a, etc. After this parallel transfer, charge in 1a is moved to 2a, the charge in 3a to 4a, the charge in 1b to 2b, etc., and the readout process is repeated. With the design shown in Fig. 3 integration occurs after the third read out when the charge in 2A' is added to the charge in 2a which originated two read out sequences ago from detector 1A. A smaller ratio of sampling time to dwell time can be obtained by interleaving more CCD bits. The register 1a, 2a, etc. is tapered in width to be able to accomodate the integrated charge.

Since the scan rate and the clock frequency are synchronized the signals from all the detectors in a column will add coherently. The noise adds incoherently so that TDI provides a $\sqrt{n}$ improvement in signal-to-noise where n is the number of detectors in a column (16 as shown in Fig. 2). The Si signal processor chip used with the CID premultiplexer would be similar in design to that used with the sandwich approach except that since it is removed from the focal plane it can be much larger than the detector area relieving packing density and CCD well saturation limitations inherent in the sandwich approach.

EXPECTED PERFORMANCE OF SERIES PARALLEL SCAN CID

To be competitive, any IR focal plane must be able to operate background limited for IR backgrounds and scan frequencies of interest. Thus we must estimate the magnitudes of the competing noise sources for the configuration shown in Fig. 2. Sampling effects complicate the analysis. We will

consider three sources of noise: background noise arising from the statistical fluctuation of arriving photons, "kTC" noise arising from an uncertainty in charge on the preamplifier input capacitance and preamplifier noise arising from fluctuations in channel current of the input field effect transistor of the preamplifier.

The design parameters associated with any particular system are defined in Table 1.

TABLE I - DEFINITIONS

τ_s	- integration time any particular CID detector cell
τ_d	- dwell time, the time taken by an image point to cross a detector cell
f_c	- clock frequency τ_s/N_m
f_{max}	- maximum signal frequency of interest = $0.8/\tau_d$
N_m	- number of CID detectors in a module
n	- number of detectors in a column (along the scan direction)
B	- output bandwidth of the preamplifier
$\dot{N}_B$	- background photoelectrons per second into a single detector cell = $\eta A_d \dot{Q}_B$ where $\dot{Q}_B$ represents the background photon flux at the focal plane A_d is the detector area and η is the quantum efficiency

Performance of the CID IR focal plane will be analyzed with reference to Fig. 4. Signal and background photons are converted into charge in the CID. The CID detectors all integrate this charge for a time τ_s after which the integrated charge is sampled by the readout process, converted into a voltage, and amplified by the preamplifier which has an output bandwidth B. The amplified voltage is resampled before being reconverted into charge for input into the CCD signal processor. The signal processor performs TDI and outputs a number of pulse trains corresponding to the photosignal seen by each column of the CID as the image is scanned over the module.

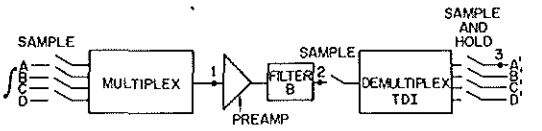

FIGURE 4 - Block diagram of the signal flow through a series-parallel scan CID focal plane array.

The input signal is reconstructed by a sample and hold process on these pulse trains. At point 3 after the sample and hold the signal will have the appearance of a staircase function, as shown in Fig. 5 for the case of uniform focal plane irradiance. The variation of signal height $\dot{N}$ shown in Fig. 5 represents noise.

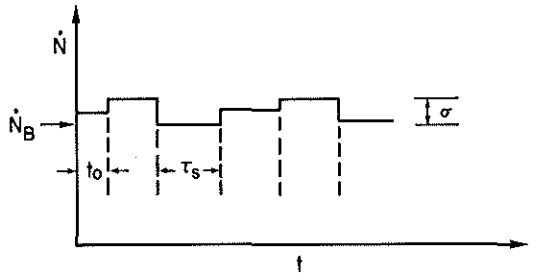

FIGURE 5 - Representative signal as a function of time after the sample and hold function shown in Fig. 4, for uniform focal plane irradiance.

As a matter of convenience, the output at point 3 will be referred back to the electrons/sec coming from an individual detector cell. σ is the standard deviation of the individual sample values at point 3 due to noise. We will assume that, after subtraction of the average value, there will be no correlation between these individual sample values as long as the input illumination is uniform. This is equivalent to assuming that before sampling the auto-correlation function of the input due to noise was zero for times larger than τ_s. This will be true for background and kTC noise and represents a reasonable approximation for preamplifier noise as long as the sampled values which are close together at point 3 did not come through the preamplifier in adjacent time slots. If the sampled values are not correlated the auto-correlation function of the signal at point 3 ignoring the DC component will be

$$\langle \dot{N}(t)\, \dot{N}(t-\tau) \rangle = \sigma^2 \ \mathrm{rect}\left[\frac{\tau-(t-t_o-(m+\frac{1}{2})\,\tau_s)}{\tau_s}\right] \qquad (1)$$

where m is the largest integer such that $m\,\tau_s < (t-t_o)$ and rect represents the rectangular function which is unity between $\pm$ 1/2 and zero elsewhere. The nonstationarity of the sampling process makes this auto-correlation function a function of both t and τ, however to calculate a power spectral density we can average this auto-correlation function over time to obtain:

$$\frac{1}{T}\int_0^T \langle \dot{N}(t)\dot{N}(t-\tau)\rangle dt = \sigma^2 \Lambda(\tau/\tau_s) \qquad (2)$$

where Λ is the triangular function (zero at $\tau/\tau_s = \pm 1$). Ignoring the DC component the power spectral density (PSD) of the output staircase waveform will thus be

$$\mathrm{PSD} = \int_{-\infty}^{\infty} \sigma^2 \Lambda(\tau/\tau_s) e^{i\omega\tau}\, d\tau = \sigma^2 \tau_s \ \mathrm{sinc}^2\, \pi\, f\, \tau_s \qquad (3)$$

The problem is one of estimating the value of σ^2 for background noise, kTC noise and preamplifier noise. If we wish to compare the variance at point 3 to the component variances associated with a single detector cell we can write:

$$\sigma^2 = \frac{\sigma_B^2}{n} + \frac{\sigma_{kTC}^2}{n} + \frac{\sigma_{pa}^2}{n} \qquad (4)$$

where all the variances are normalized to the mean. The factor of n is due to the time delay and integration process. The uncertainty in the amount of collected background photons in an integration period τ_s from a single detector cell is just $\sqrt{\dot{N}_B \tau_s}$ so that the variance in the rate of collection is just

$$\sigma_B^2 = \frac{\dot{N}_B}{\tau_s} \qquad (5)$$

kTC noise is caused by an uncertainty in the charge on the capacitor C at the input to the preamp (point 1) before the detector cell charge is shifted under this capacitor for readout. This uncertainty in electronic charge is just $\sqrt{(2/3)kTC}$ which converted to a rate and referred back to the detector as elections per second, gives a variance of

$$\sigma_{kTC}^2 = \frac{(2/3)\,kTC}{e^2\,\tau_s^2} \qquad (6)$$

where e is the electronic charge and k is Boltzman's constant.[4]

The preamplifier introduces noise which can be described by an equivalent input voltage noise with RMS value V_{rms} such that

$$V_{rms} = V_n\, B^{1/2} \qquad (7)$$

where B is the bandwidth of the preamplifier circuit. Because the preamplifier is followed by a sampling process this value of B must be minimized regardless of the final value of f_{max}. The rms noise must be

made small at the sampling point. B must not be made too small since we must pass signal pulses through the preamplifier relatively unattenuated and since crosstalk between adjacent samples should be avoided. Thus there is a genuine tradeoff in selecting a value of B. For our calculation we will use:

$$B = 1.6\, f_c = \frac{1.6\, N_m}{\tau_s} \qquad (8)$$

With this choice, we can calculate an equivalent charge uncertainty at the input to the preamplifier and relate this to an uncertainty in the rate of electrons at the detector. This leads to a variance of:

$$\sigma_{pa}^2 = \frac{C^2 V_n^2\, B}{e^2\, \tau_s^2} = \frac{1.6\, N_m C^2 V_n^2}{e^2\, \tau_s^3} \qquad (9)$$

For comaprison with a signal in electrons/sec from a single detector cell we thus have:

$$PSD = \left[\frac{2\dot{N}_B}{n} + \frac{4kTC}{3ne^2\,\tau_s} + \frac{3.2N_m C^2 V_n^2}{e^2 \tau_s^2 \eta}\right] \operatorname{sinc}^2 \pi f \tau_s \qquad (10)$$

To understand the tradeoff in the choice of τ_s relative to f_{max} we must consider the effect of the sampling process on signal as well as noise. The scanning process converts the spatial variations in the image into an AC signal which is added to the noise. Any single frequency AC signal, $\dot{N}_s \sin^2 \pi f t$, coming from a single detector cell, will be attenuated by both the input integration function and the output sample and hold function so that its peak to peak value at the output (excluding aliased terms) on the average will be

$$\text{signal} = 2\dot{N}_s \operatorname{sinc}^2 \pi f \tau_s \qquad (11)$$

From a noise point of view, a long τ_s is desirable because it makes background limited operation more likely. As $\tau_s \to 1/f$, however, the magnitude of the signal at the output will be reduced. A τ_s which is longer than optimum can thus reduce the background limited signal to noise ratio at f_{max}. For our example we will choose:

$$\tau_s = \frac{1}{3f_{max}} \qquad (12)$$

such that a signal at f_{max} would be attenuated by a factor of 0.68 if no frequency boosting were employed.

In practice frequency boosting will be employed to flatten out the signal. In that case the PSD of the noise after the boosting process will be modified to

$$PSD' = \sigma^2 \tau_s / \operatorname{sinc}^2 \pi f \tau_s \qquad (13)$$

and the RMS value of the output after passing through a frequency boosting filter and then a bandpass filter will be

$$(\text{RMS noise})^2 = \int_{f_{max}}^{f_{max}} PSD'\, df \qquad (14)$$
$$\cong 2\sigma^2 \tau_s f_{max} \left[1 + \frac{f_{max}^2 \pi^2 \tau_s^2}{9}\right]$$

so that the use of $\tau_s = 1/(3f_{max})$ with a bandpass final filter implies a decrease in the background limited signal-to-noise ratio of 6% over that which would be obtained for $\tau_s \ll 1/f_{max}$. In practice with an imaging system the bandpass of the final filter is influenced by the eye acting as a spatial filter for signals on the display.

If we desire $f_{max} = 0.8/\tau_d$ (representative for an imager design) we can achieve $\tau_s = 1/3f_{max}$ by a 3 to 1 interleave in the TDI register and a center to center spacing to detector size ratio, y/x of 1.25.

With this relationship between τ_s and f_{max} and with frequency boosting we have for the CID

$$(\text{RMS noise})^2 = \left[\frac{2\dot{N}_B}{n} + \frac{4kTC f_{max}}{e^2 n} + \frac{28.8C^2 V_n^2 N_m f_{max}^2}{e^2 n}\right] f_{max} \qquad (15)\ (1.12)$$

For background limited operation the first term should dominate the remaining two. We will define f* for the CID to be that value of f_{max} for which the first term equals the sum of the remaining two terms. Without correlated double sampling, C.D.S., kTC noise dominates and

$$f^* = \frac{\dot{N}_B e^2}{2kTC} \qquad (16)$$

whereas if kTC noise is suppressed by correlated double sampling we will have:

$$f^* = \left[\frac{\dot{N}_B e^2}{(14.4) V_n^2 C^2 N_m}\right]^{\frac{1}{2}} \qquad (17)$$

Without excess noise in the preamplifier, channel thermal noise of the input FET will dominate and V_n will be given by $V_n = (8/3\ kT/g_m)^{1/2}$ where g_m is the transconductance of the input FET. g_m can be as high as 8000 μmhos giving

$$V_n = 5.95 \times 10^{-10} \text{ volts/Hz}^{1/2} \text{ at } 77°K \qquad (18)$$

In these f* relationships for the CID, C is the total capacitance between the input to the preamplifier (at point 1) and ground. C includes stray capacitance, the input capacitance to the preamplifier (5 pf), and the capacitance of the column readout line. If nondestructuve CID readout techniques are used with two surface electrodes per detector then this latter capacitance will be limited by the capacitance of half the photoactive area associated with a column of the CID module. As the number of detectors in a column is increased to make the module size larger C will thus increase. Assuming the same module aspect ratio as shown in Fig. 2 (16/25), a stray capacitance of 1 pF, InSb photoactive area capacitance of 0.1 pF/mil^2 and a full detector cell size of 4 mil^2, we can write

$$C = (6 + .16\sqrt{N_m})\ \text{pF} \qquad (19)$$

which is 9.2 pF for N_m = 400.

Using the above relationship for C we have plotted f* as a function of $\dot{N}_B$ for several values of N_m in Fig. 6. In all cases we have adjusted the clock frequency such that $\tau_s = 1/3f^*$. With kTC noise there is a minimum number of background photons which must be collected per sample time to make the device background limited. For C = 9.2 pF this number is 2.5 x 10^5 electrons. If the limitation is kTC noise, the dependence of f* on N_m is not strong.

With a careful implementation of the non-destructive CID readout techniques introduced by Michon and Burke in their parallel injection readout scheme it should be possible to implement correlated double sampling (CDS) as shown in Fig. 7, and remove the effect of kTC noise.[6,7] The removal of kTC noise by correlated double sampling (CDS) can provide approximately an order of magnitude increase in f* for devices operating in the 3-5 μm region where considering different applications $\dot{N}_B$ can vary from 1 x 10^8/sec to 1 x 10^{10}/sec depending on the exact choice of spectral filtering and F/no.

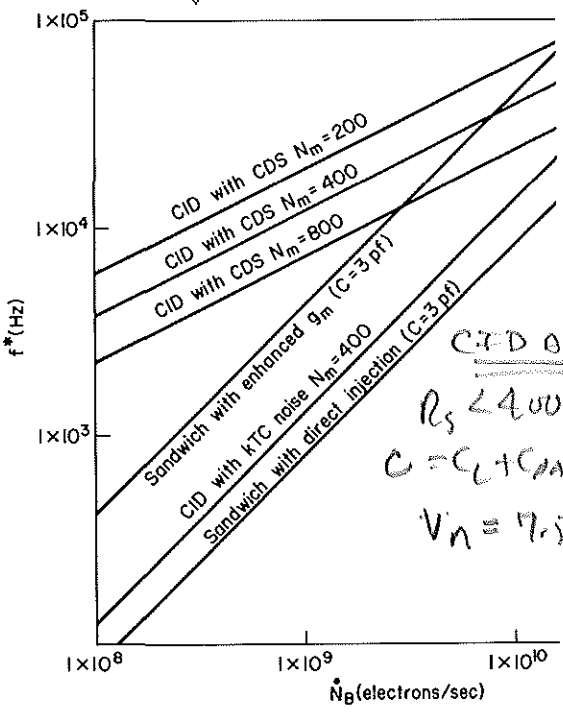

FIGURE 6 - The maximum signal frequency for which various FPA configurations will be background limited as a function of the photoelectron generation rate at a single detector in the array.

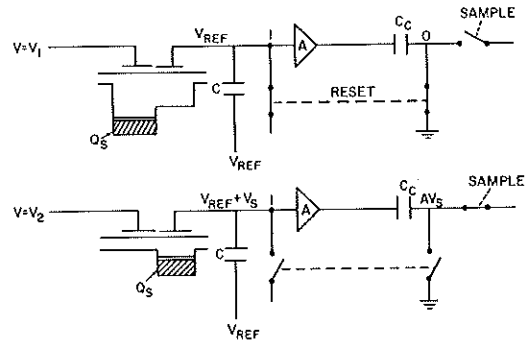

FIGURE 7 - Technique for implementing correlated double sampling with a non-destructive CID readout. The reset switch is opened, V_1 changes to V_2 transferring the signal charge, Q_S, and then the output is sampled.

kTC noise will lead to an uncertainty in the charge on the capacitor C before the read cycle, however if the resistance between the point 1 and ground is high enough after the reset switch is opened, this total charge will not have time to change before the signal charge is "sloshed" under the readout electrode and the change in voltage caused by this transfer of charge is sampled at the output. Since only the change in voltage caused by the transfer of signal charge is measured at the output, kTC noise will not be observed. As long as the capacitance of a single cell is a small portion of the total capacitance between point 1 and ground this change in voltage V_S will be Q_S/C.

Examination of Fig. 6 for the CID with CDS (N_m = 400) shows that for background currents of 10^9 electrons/sec corresponding to A_d = 4 mil^2, η = .7, and $\dot{Q}_B = 5.7 \times 10^{13}$ photons/cm^2, an f_{max} of 10 kHz should be possible while remaining background limited. Clock frequencies of 12 MHz would be needed; τ_d could be as short as 8×10^{-5} sec for background limited operation. The relationship between f_c and f_{max} is determined by eq. (12).

$$f_c = 3\ N_m\ f_{max} \qquad (20)$$

This relationship is plotted in Fig. 8 for representative values of N_m. Larger values of N_m would reduce the number of interconnects per detector. However, in general the use of a larger N_m reduces f* and for a given f_{max} may increase the required clock frequency to unobtainable values.

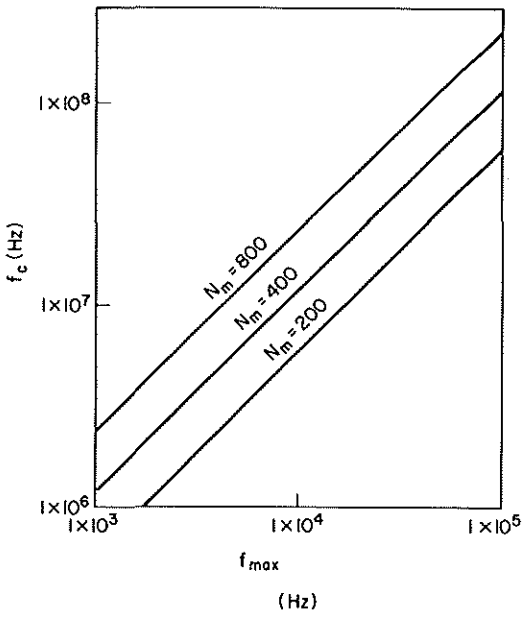

FIGURE 8 - Clock frequency, f_c, as a function of the maximum signal frequency of interest, f_{max} for various CID module sizes.

NOISE LIMITATIONS WITH DIRECT INJECTION (SANDWICH STRUCTURE)

In the previous section we have developed estimates of f* for the CID F.P.A. structure which uses premultiplexing. In this section for comparison purposes we will estimate f* for a sandwich FPA structure which uses direct injection to inject photogenerated charge into CCD TDI registers. A comprehensive treatment of signal-to-noise ratio at the output of a direct injection based FPA has been developed in refs. 1 and 2. It was determined that the direct injection input circuit itself is responsible for the most stringent limitation on f*. In the simplified treatment provided here, we will concentrate on the competion between noise arising from the input circuit and noise arising from fluctuations in the background flux. As a first approximation, the effects of sampling will be neglected. Minor correction factors due to sampling will be derived in Appendix A.

The input structure is shown in Fig. 9. The detector anode is connected to a p type diffusion. During an integration period τ_s, V_{sc} is held at a fixed bias to deplete the vicinity of the input diffusion while the screen electrode, V_{ST}, is biased more negatively to create a potential well. Photocurrent from the detector is injected from the diffusion and stored beneath V_{ST}. At the proper time by changing ϕ_T this stored charge is transferred into the CCD TDI register. Charge is then transferred down the register and the cycle is repeated.

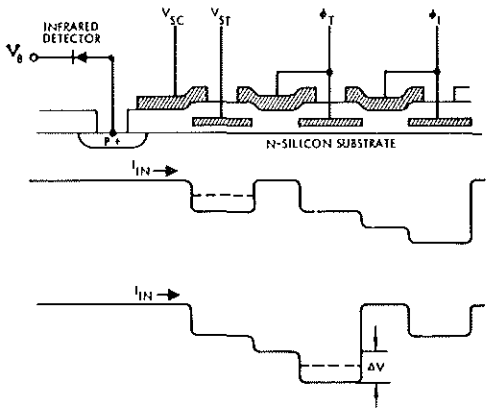

FIGURE 9 - Direct injection input circuit structure.

The AC equivalent circuit of Fig. 10 can be used to analyze the circuit operation. The input structure is treated as a grounded gate MOSFET where the input diffusion, "S", acts as a source, V_{sc} as a gate and the potential well under V_{ST} as a virtual drain. At the low photocurrents of interest this MOSFET will usually operate in the sub-threshold or weak inversion regime where

$$g_m = \frac{1}{2}\frac{e}{kT} I \qquad (21)$$

where I is the total D.C. current flowing from the source to the drain.[8,9,10] At higher currents $g_m \alpha I^{1/2}$. In Fig. 10, C is the combination of all input shunt capacitances and will be about 3 pF for a 2 mil square InSb photodiode. i_s is the shot noise of the background generated photocurrent, i_1 is the noise current due to shunt resistances and i_2 represents the MOSFET channel thermal noise. Vg_s is the voltage between the gate and the source. Note that the current generator $g_m Vg_s$ acts like a resistance in series between the detector and an ideal processor.

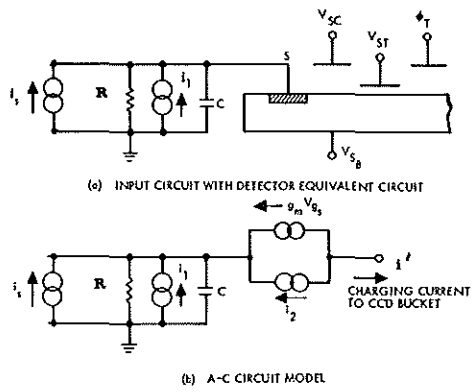

FIGURE 10 - AC equivalent circuit with direct injection.

An analysis of this equivalent circuit gives an expression for the output current power spectral density.

$$\frac{\int^{*}_{CCD}}{\int^{*}_{DT}} = \frac{C_{DT}}{C_{CCD}} \sqrt{\frac{g_{m_{CCD}}}{g_{m_{DT}}}}$$

$$PSD_i = \left|\frac{g_m R}{(1+g_m R)(1+j\omega RC(1+g_m R)^{-1})}\right|^2 (e^2 \dot{N}_B + 2kT/R) \left|\frac{1+j\omega RC}{(1+g_m R)(1+j\omega RC\ (1+g_m R)^{-1})}\right|^2 ((4/3)kTg_m) \quad (22)$$

where R is the effective resistance between S and ground. To avoid Johnson noise limitations we must assure that R is large enough. If we arrange the circuit such that $R >> 2kT/e^2\dot{N}_B$, f* will be limited by channel thermal noise. If Johnson noise can be neglected we will have $g_m R >> 1$ as long as the equivalent input MOSFET would be in the subthreshold regime (for $I = e\dot{N}_B$). Under these conditions f* can be defined as the largest value of f for which the second term in the PSD_i dominates the first term. Neglecting effects due to the sampling process f* is thus given by:

$$f^* = \frac{\sqrt{2e\dot{N}_B g_m}}{2\pi C\sqrt{8/3\ kT}} \quad (24)$$

If the value from Eq. 21 is used for g_m then:

$$f^* = \frac{\sqrt{3/2}\ e^2\ \dot{N}_B}{4\pi CkT} \left[\frac{I}{e\dot{N}_B}\right]^{1/2} \quad (25)$$

As large a value of g_m as possible is desired. Use of the subthreshold expression for g_m as a function of I could be optimistic for $I \geq 1 \times 10^9$ amps.

With the most straightforward implementation of direct injection R is the detector resistance and $I = e\dot{N}_B$. f* for this case is plotted in Fig. 6 as direct injection with C = 3pF. If I is greater than $e\dot{N}_B$, g_m enhancement can occur and f* will be increased. We estimate that I can be increased by a factor of 30. Assuming the subthreshold expression for g_m vs. I, this leads to a mixiumum improvement ratio of 5.5 for f* which is plotted in Fig. 6.

Another approach to a higher f* with direct injection is to use a photoconductor to provide D.C. gain to enhance I. The smaller capacitance of a photoconductor would by itself lead to an increase in f*. As an example we will consider an extrinsic Si photoconductor with the properties listed in Table II.[11]

TABLE II - EXTRINSIC PHOTOCONDUCTOR PROPERTIES.

$E_{max} = 2500\ V\ cm^{-1}$

$\mu = 6 \times 10^3 cm^2 V^{-1}\ sec^{-1}$

$\tau = 2 \times 10^{-8}$ sec

$L = 0.1$ cm (thickness and inter-electrode spacing)

$C = 0.5$ pF

$A_d = 2.5 \times 10^{-5}\ cm^2$

With these properties the D.C. gain $G_o = (E\mu\tau/L)$ will be 3 making $I/e\dot{N}_B = 3$.

Assuming a saturated A.C. gain of 1/2 and $R >> 8kT/e^2\dot{N}_B$ referring to Eq. 16, f* for the photoconductor will be

$$f^* = \frac{1}{2}\ \frac{\sqrt{3/2}}{4\pi CkT}\ e^2\ \dot{N}_B\ (G_o)^{1/2} \quad (26)$$

which for $G_o = 3$ and C = .5pF represents an improvement in f* over the 3pF photodiode of a factor of 5.2 (at the same T). Thus f* for a photoconductor would be similar to our estimate of f* for a photodiode with g_m enhancement. The use of an A.C. gain of 1/2 in the above expression

will be justified as long as the dielectric relaxation time, τ_ρ, is such that

$$f_\rho = \frac{1}{2\pi\tau_\rho} << f^* \qquad (27)$$

i.e., as long as

$$\frac{e\mu\tau\dot{N}_B}{2\pi A_d L\ \varepsilon} < \frac{1}{2}\ \frac{\sqrt{3/2}\ e^2\dot{N}_B\left(\frac{E_m\mu\tau}{L}\right)^{1/2}}{4\pi CkT} \qquad (28)$$

For the values in Table II at 60°K

$$f_\rho/f^* = \frac{(G_o)^{1/2}}{E_m\varepsilon}\ \frac{4CkT}{\sqrt{3/2}\ eA_d} = 0.23 \qquad (29)$$

so that the assumption of a saturated photoconductive gain of 1/2 at f = f* is justified.[12]

The 3-5 μm extrinsic photoconductor will give superior f*performance to the photodiode; however there will be a temperature of operation penalty and since absorption lengths tend to be long there will be quantum efficiency vs. crosstalk tradeoffs for a 3-5 μm FPA made with extrinsic photoconductors.

All of the above estimates for f* with direct injection ignore sampling effects and are therefore only strictly true for sampling rates such that $\tau_s << 1/f^*$. In practice since CCD bits cannot be made an order of magnitude smaller than the detector size this is unlikely to be the case if f* approaches $f_{max} = 0.8/\tau_d$. In the appendix we have considered the effects of sampling for a more realistic case where $\tau_s = 1/3f^*$ and show that the degradation in f* from the effects of sampling will be about 16%.

CONCLUSIONS

Series parallel scan with small InSb CID modules appears to be a convenient moderate cost approach to IR focal plane arrays for the 3-5 μm region. Our calculations suggests that the use of CID for premultiplexing has the potential of providing a higher f* in the 3-5 μm region than any of the focal plane array approaches that we have analyzed which use direct injection with the possible exception of direct injection with an extrinsic photoconductor including g_m enhancement. To realize this projected f* performance high speed (10-20 MHz) CID readout schemes which include correlated double sampling must be developed.

None of the FPA designs we have analyzed appear readily capable of providing f* high enough for a TV compatible IR imaging system in the 3-5 μm region (which requires an f* of ≈ 30 kHz). With the higher background fluxes of the 8-12 μm region extrinsic photoconductor FPA's using direct injection should not be seriously limited by f* problems if the imaging systems use a parallel scan.

APPENDIX A

DEGRADATION IN f* WITH DIRECT INJECTION DUE TO SAMPLING

Unless $\tau_s << 1/f$ the integration and sampling which occurs at the output of a direct injection circuit with a sandwich type FPA structure will have some effect on the signal-to-noise ratio. Due to the complex frequency dependence of the noise power spectral densities before the sampling we will take a different approach to calculating the effect of aliasing than was used with the CID.

If f_s is the sampling frequency the noise current power spectral density after integration and sampling, $\widehat{PSD_i}$, will be

$$\widehat{PSD_i}(f) = \sum_{-\infty}^{\infty} PSD_i(f+nf_s)\ \mathrm{sinc}^2\pi\ \frac{f+nf_s}{f_s} \qquad (A\text{-}1)$$

where sincx ≡ (sinx)/x and where $PSD_i(f)$ is the power spectral density before integration and sampling. In a practical case we could adjust f_s such that

$$f_{max} = f_s/3 \qquad (A\text{-}2)$$

so that

$$PSD_i'(f_{max}) = 0.68\ PSD_i(f_{max}) \left[1 + 0.25 \frac{PSD_i(2f_{max})}{PSD_i(f_{max})} + 0.06 \frac{PSD_i(4f_{max})}{PSD_i(f_{max})} \cdots \right] \quad \text{(A-3)}$$

With the expression for PSD_i from Eq. 22 the term in brackets represents an increase of about 55% in channel thermal noise power and 10% in photon noise power. With these sampling effects included, the frequency $f_{max} = f^*$ at which channel noise power exceeds photon noise power is 16% lower than that predicted by the non-sampling approximation. Further the signal-to-noise ratio at the corrected f* is approximately 5% lower than that predicted at the uncorrected f* with the non-sampling approximation. This decrease is due to increased photon noise due to noise folding.

While one would like to avoid the effects of noise folding, the geometry of the array will determine the maximum sample rate relative to the dwell time. If n_d is the maximum number of CCD bits that can be placed in a space equal to the detector width in the scan direction then:

$$\tau_d = n_d \tau_s \quad \text{(A-4)}$$

and if

$$f_{max} = \frac{0.8}{\tau_d} \quad \text{(A-5)}$$

we will have

$$f_s = \frac{1}{\tau_s} = \frac{n_d}{0.8} f_{max} \quad \text{(A-6)}$$

so that if n_d is limited to 2.4 for a 2 mil detector

$$f_s \leq 3 f_{max} \quad \text{(A-7)}$$

An acceptable yield with smaller CCD bits would allow less aliasing and noise folding. The inter-detector spacing would of course in all cases be adjusted to provide an integer number of CCD bits between inputs.

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