INTEGRATED CCD-BIPOLAR STRUCTURE FOR FOCAL PLANE PROCESSING OF IR SIGNALS

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ABSTRACT The trend in thermal imaging sensor design is toward the use of high performance, low cost, integrated focal plane arrays. The hybrid marriage on the focal plane of detector mosaic with charge coupled device processor is one concept to economically achieve greater detector densities. The IR system requirements do impose severe constraints on the design of the preamplifier/CCD processor.

A monolithic CCD processor with bipolar preamplifier array was developed for use with photoconductive HgCdTe detectors.* The designs and operation of both PNP and NPN preamplifiers with P and N type surface channel charge coupled devices are described. Preliminary test results show the preamplifier gain for a PNP device at 77°K to be above 30 with greater than 1.8 megahertz bandwidth and approximately two (2) nanovolts per root Hz noise referenced to the input. Non-uniformities among preamplifiers (base-emitter voltages and bias resistors) are responsible for variation in dc bias voltages at the CCD input gates. Large differences in dc bias among input gates may compromise the CCD gain when operating in a time delay integration mode. The measured linear dynamic range using gate modulation input is 67db.

I. INTRODUCTION

The evolution of charge coupled device technology has provided momentum to the concept of focal plane signal processing in advanced FLIR systems.(1) Speculative systems designs with CCD's predict much greater number of detectors than contemporary technology would permit. The ability to integrate detector with signal processor on the focal plane in a single hybrid or monolithic structure permits detector densities commensurate with high performance in thermal imaging. Ultimately, the detector-processor marriage will lower system cost and improve system reliability.

This paper addresses the development of a CCD Time Delay Integration (TDI) circuit monolithic with a bipolar preamplifier array.(2) The device is designed to operate at 77°K for direct coupling to 0.1 ev HgCdTe in a serial scan application. The basic system characteristics which impose constraints on the preamplifier-CCD design are listed in Table I.

TABLE I
Requirements Imposed On CCD/Preamp

System Spec	CCD/Preamp Requirement
Multi-row, Serial Scan, TV Compatible	Signal B.W.> 1.5MHz Out. Data Rate > 5MHz Taps per TDI > 8
8-12μ wavelength NETD < 0.2°K	Dynamic Range > 60db
HgCdTe at 77°K	Operate at 77°K NEI ≤ 2nV/Hz$^{1/2}$ Gain > 30
Dewar Heat Load <.75 watts (cold shield, radiation, bias, preamp, CCD)	3mW max per channel Min Silicon Area
Cost/Reliability	Bipolar compatible with CCD fabrication process

*Devices fabricated by Hughes Aircraft and supplied to NVL under contract DAAK02-74-C-0229.

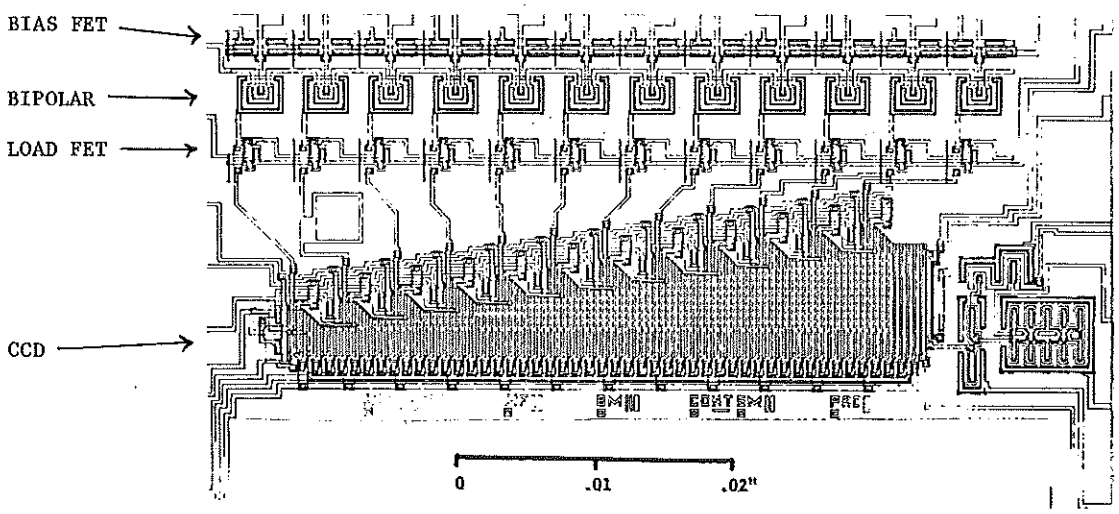

FIGURE 1
PREAMP ARRAY WITH CCD-TDI

The CCD/Preamp must interface with a mercury-cadmium-telluride detector array. Photoconductive HgCdTe, operated at background limited performance (BLIP), has a noise voltage which ranges from 4 to 8 nanovolts per root hertz. The detector bandwidth is greater than one megahertz. The impedance is normally 50 ohms but may vary from 50 ohms up to 100 ohms. A constant current detector bias is used to partially compensate for detector resistor variance.

The CCD must not limit system sensitivity, linearity, MTF, or dynamic range and must maintain detector BLIP conditions.

II. CIRCUIT DESCRIPTION

The preamplifier and CCD processor array (PAPA) is shown in Figure 1. The circuit consists of (1) a 12 input tapered CCD shift register for time-delay-integration action; (2) a MOSFET bias resistor for each detector and a MOSFET for each preamp load at the input to the CCD gates; and (3) bipolar amplifiers operating in a grounded base configuration. Devices were made using P-channel CCDs with PNP bipolars and N-channel CCDs with NPN bipolars. All CCDs were surface channel devices.

A. Charge Coupled Device: Each output of the twelve preamplifiers is directly coupled to one of the twelve input gates on the charge coupled device. Figure 2 schematically illustrates the basic building block (1 of 12) for the focal plane processor.

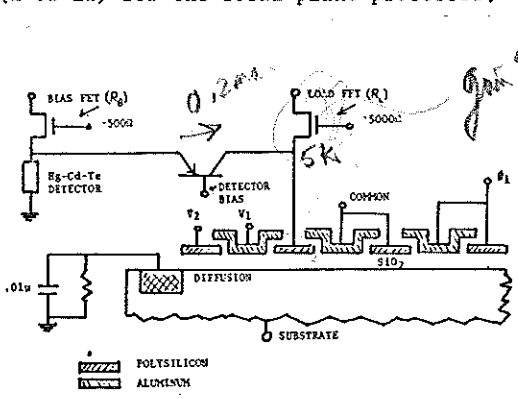

FIGURE 2
PREAMPLIFIER/CCD BUILDING BLOCK

The amplified signal voltage modulates the channel beneath a buried polysilicon electrode. The CCD register is operated with complementary two phase clocks. A "diffusion" current, entered through an RC integrating network, is introduced at the p+ diffusions adjacent to each input gate. It is this current, when modulated by gate signal voltage, which supplies charge to the CCD wells for transfer and integration. The width of the CCD registers are tapered, becoming progressively wider from the beginning to the end of the device. The

$\frac{V_n^2}{\Delta f} = 4kTR = 4(1.38\times10^{-23})(77)5\times10^{3} \simeq 20\times10^{-18}$

$\frac{V_n}{\sqrt{\Delta f}} \simeq 4.5\,nV/\sqrt{Hz}$

tapering effectively maintains a near constant percentage of fill level since well capacity becomes greater as charge is successively integrated along the line. Several gate modulated input schemes were evaluated. The integrating input, where charge is integrated on common over a clock period then shifted out at ϕ_1 rates, proved to have a lower noise equivalent input than that of the pulsed diffusion mode.(2) The voltage at the CCD output should be less than a volt in order to maintain reasonable linearity in the output charge amplifier. The on-chip output charge amplifier uses a floating diffusion with a single reset MOS transistor and a double source follower as shown in Figure 3.

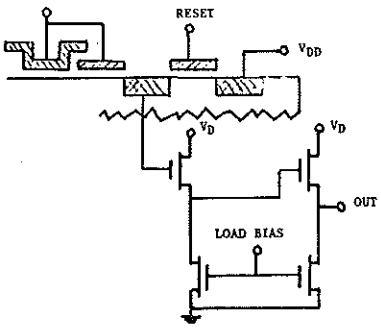

FIGURE 3
CCD OUTPUT

B. MOSFET Resistors: The MOSFET resistor used to bias the HgCdTe detector was designed to be 500 ohms at 2mA of current. This separate MOSFET supplies the detector bias current in order that only minimum current need flow through the bipolar transistor and associated load resistor. The preamplifier load FET is designed for 5K ohms when operating near 200μA quiescent current.

C. Bipolar Preamplifier: Several preamp designs were incorporated on each chip in order to determine the optimum gain-bandwidth and low noise configuration. The current gain (β) decreases substantially at lower temperatures. However, the α remains reasonable and a significant transconductance (g_m) can be obtained at 77°K. Figure 4 shows the noise model for the common base preamplifier. The preamplifier voltage gain is given by:

1) $\text{gain} = \frac{\alpha R_L}{R_D + r_e + (1-\alpha) r_b}$

where

R_L = MOSFET Load Resistance

α = current transport factor = $\frac{\beta}{\beta+1}$

r_e = emitter resistance = $\frac{kT}{qI_e}$

r_b = base spreading resistance

R_d = detector resistance

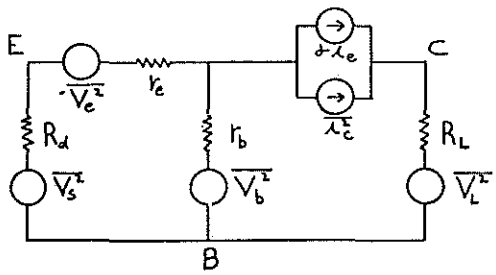

FIGURE 4
COMMON BASE AMPLIFIER NOISE MODEL

The noise equivalent input (NEI) of the preamp was designed for less than 2 nanovolts per root hertz. At midband the mean square equivalent input noise is given by:

$$\overline{V_{in}^2} = \overline{V_L^2}/G^2 + \overline{V_s^2} + \overline{V_b^2} + \overline{V_e^2} + \overline{i_c^2}\,(R_L/G + r_b)^2$$

where

G = amplifier gain

$\overline{V_s^2}$ = thermal noise of the source

$\overline{V_b^2}$ = thermal noise of the base spreading resistance

$\overline{V_e^2}$ = Voltage equivalent of emitter current noise (3)

$\overline{i_c^2}$ = Collector current noise

III. CIRCUIT FABRICATION

In order that the bipolar device fabrication be compatible with surface channel CCD processing, lateral bipolar transistors were built using a "triple diffusion" process. The basic processing steps for a triple

FLIR should use this approach!

uniformity ± 150mV at input without correction actual ± .9μV/√Hz

10nV/√Hz measured referred TDI amp of CCD input approximately √12

÷ 45 (typical gain) ≈ 2nV/√Hz

diffusion PNP-transistor P-channel CCD are:

(1) P-type collector well diffusion (or implant) and drive in

(2) N-base contact diffusion (required only for PNP devices)

(3) N-type base diffusion and drive-in (simultaneous with input diffusions in CCD)

(4) Contact holes and metallization (can be merged with CCD processing)

When comparing the triple diffusion transistor to the more standard types the parasitic collector resistance is higher (500-1500 ohms), the base to collector breakdown voltage is lower (15-30 volts), and the base to collector capacitance is higher (about 3pf).

The metallization pattern provided common ties to the same functions on each input and the fat zero (Fig 1 & Fig 2). The bias FETs (R_B) drains are common. The bipolar bases are common. The load FETs (R_L) gates and drains are each common. The integrating gates "common" for the 12 inputs and fat zero are also tied together. Fat zero level may be controlled separately by its own gate. One test pad was made available on the CCD input at the output of the amplifier on channel two. The combination of tied electrodes made separate evaluation of the effects of each component (R_B, bipolar, R_L, CCD gate) difficult without using special operating modes.

IV. EXPERIMENTAL RESULTS

A. Preamplifiers: Both NPN and PNP transistors were evaluated. The current gain betas (β) for both are tabulated in Table II for the various emitter configurations. Beta does decrease dramatically with temperature, however, at 77°K the $\frac{\beta}{\beta+1}$ appearing in the gain equation for a common base amplifier, is still reasonable. The magnitude of the base spreading resistance (r_b) is inversely proportional to temperature. At reduced temperatures the current crowding, even at 200μA, can affect beta. The multi-emitter structure minimizes r_b, reduces current crowding, and thus enhances beta at 77°K. Figure 5 shows the gain and

TABLE II
Transistor Beta
Collector Current = 200μA

	NPN		PNP	
Emitters	300°K	77°K	300°K	77°K
1	180	12.5	135	5.4
2	460	16.	110	5.6
4	500	19.5	110	5.6
8	440	23.0	130	6.2

noise over frequency for PNP amplifiers at 300°K and 77°K. Figure 6 is a similar graph for NPN amplifiers. With the reduced emitter resistance($\frac{kT}{qI_e}$) at 77°K, there is an increase in gain. With a 5K ohm load resistor the high frequency roll-off in gain is dominated by instrumentation input capacitance. Operating into a CCD gate the frequency response of the bipolar amplifier would be greater than shown. The PNP devices do have lower noise than the NPN devices. The noise for both NPN and PNP is higher at 77°K then at 300°K, probably due to increased contributions from base spreading resistance. Because the multi-emitter structure does reduce r_b, the noise associated with multi-emitter PNP and NPN devices is less than for a single emitter transistor at 77°K.

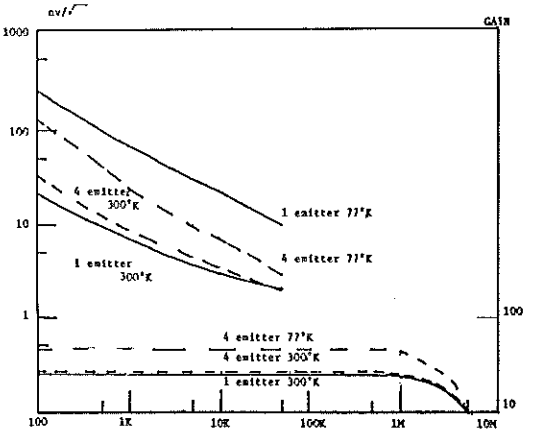

FIGURE 5
PNP GAIN/NOISE CHARACTERISTICS
(With discrete load resistor)

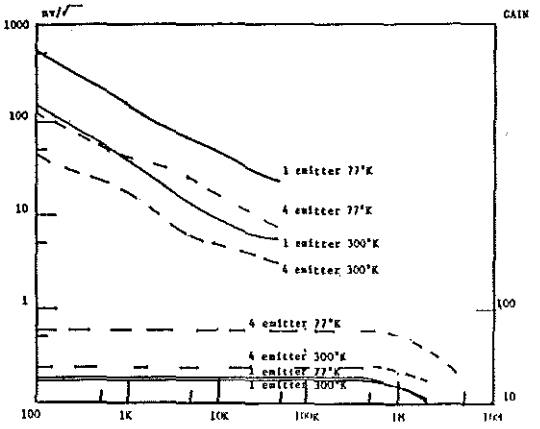

FIGURE 6
NPN GAIN/NOISE CHARACTERISTICS
(With discrete load resistor)

C. CCD & Preamp: The gain of this CCD is related to the g_m associated with the gate modulated input and the integration time. The g_m may be increased by increasing the dc current beneath the gate (channel current in the common source MOSFET analogy). With signal and bias applied to only one input the dc current can be adjusted to achieve a gain of about 1.5 in the CCD-2085 when clocked at one megahertz. In the TDI mode all inputs are on and the signals and dc bias levels add constructively. Therefore, the dc channel current must be reduced to prevent complete filling of any wells as each input adds to the main channel. The maximum signal gain achievable in the TDI mode was 0.2 at 1MHz data rate.

In order to study the effect of variations from the preamplifiers and input structures the CCD was run in both the TDI and multiplexer modes. In the TDI mode a long period (greater than 48 clock periods) pulse was entered into all inputs simultaneously to assure that TDI action would occur. The resulting output is a staircase with 12 steps. Variations in step height were noted. However, the relative amount due to gain variances, and dc variances could not easily be separated as the gain was low (0.2 as described above). In the second experiment the CCD was run as multiplexer in the higher gain mode with 200kHz clock. The "common" electrodes, which are between each input and the main channel, are normally biased to a dc level. In this case, they were held off and gated on for a short period and then the inserted signals clocked out before inserting additional inputs. This short sampling period prevented the TDI action and permitted separate observation of the samples from each input. Operating the CCD register with the bipolar amplifiers off (emitter grounded) provides a reference output level for each input. Then, applying a stable dc voltage to each emitter, the resulting output can be compared to the reference. If there were no variations among amplifiers (bipolars and FET loads) then the differences in "off" and "on" outputs should be identical for all inputs. The measured differences using this technique on one P-channel device ranged from 9 millivolts to 111 millivolts. These variations can be attributed to:

Transistor base-emitter offsets leading to different dc currents through each load FET.

Resistance tolerance of the load FET.

The metallization pattern on the CCD-2085 did not permit experimental separation of the offsets from these two sources.

The dynamic range was characterized by applying a sinusoidal signal to a single input and determining when distortion becomes excessive. The signal was capacitively coupled to the CCD gate, which was dc biased through a large resistor. The clock frequency was 1MHz and the signal frequency was 10kHz. At the CCD output the signal is filtered to suppress the main clock frequency, and the harmonic components are measured using a spectrum analyzer (HP5556). The percentage 2nd harmonic component of the fundamental is used to express the signal transfer linearity and define the upper extreme for dynamic range. The setting of quiescent current (fat zero + diffusion currents from 12 inputs) will determine where a large signal will start to distort. For a given quiescent current, the output spot noise of the CCD can be measured and the ratio of maximum signal to output noise established. At one megahertz clock and under particular bias conditions, the maximum signal for 3% second harmonic was 0.6 volts and the spot noise at 200kHz was $350nv/Hz^{1/2}$. Dynamic range is defined as the ratio of the maximum undistorted peak-to-peak signal to the RMS value of the output wideband noise voltage. The dynamic range, assuming a 500kHz flat noise bandwidth, is 67db.

V. SUMMARY

A CCD delay and integration processor with integrated preamplifiers was developed for focal plane processing of signals from HgCdTe detectors. The CCD-compatible bipolar devices operating at 77°K exhibited gains greater than 30, bandwidths above 1.8MHz, and noise commensurate with good background limited HgCdTe detectors. The success of this bipolar/CCD monolith is in itself an important contribution to charge coupled device technology.

The IR system imposes many requirements on the design of the CCD focal plane processor. Noise, gain, bandwidth, dynamic range, uniformity, and power must trade-off against one another in a manner not to degrade system performance after the detector. Of particular interest in direct coupling from detector to preamp to CCD is dynamic range and uniformity. The measured linear dynamic range of 67db should be adequate under all but the most unusual scenario. For delay-and-integration operations, because the signals from individual channels are summed together, small variations between channels are unimportant. Large variations in dc level at the CCD input gate, however, may turn-off or saturate some channels. Interchannel non-uniformity can be caused by variations in the CCD gate threshold, transistor load resistance, or the transistor emitter-base threshold voltage. The process used to fabricate the CCD-bipolar combination must provide enough uniformity to minimize the occurrence of such effects. The non-uniformities measured on the CCD-2085 were great enought to impair efficiency on certain channels. Improved bias uniformity among CCD input gates may be obtainable through optimized device processing to minimize bipolar threshold variations or through ac coupling between amplifiers and CCD.

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