10:17 — 10:39 presentation
10:39 — 10:42 questions

InSb CCDs AND OTHER MIS DEVICES FOR INFRARED APPLICATIONS*

R. D. Thom R. E. Eck J. D. Phillips J. B. Scorso

Santa Barbara Research Center
Goleta, California

ABSTRACT. Indium antimonide (InSb) CCDs and other MIS devices have been fabricated and successfully operated. The CCDs are four-phase, overlapping gate, surface channel devices fabricated on n-type, single-crystal InSb. The demonstration of charge coupling in this material offers the potential of a future generation of 1- to 5-μm charge-coupled infrared imaging devices (CCIRIDs). Fabrication of the MIS structures is discussed. Several properties of the insulator-InSb interface were evaluated from MOSFET and MIS capacitor data. Measurement of interface state density has indicated midband values of $6 \times 10^{11}/cm^2$-eV. Storage times of up to 0.5 sec have been measured at 77°K; the dark current at this temperature is shown to be due to bulk, rather than surface, generation. Effective inversion layer mobility of 250 to 500 cm^2/volt-sec has been determined from the MOSFETs. Results are given for a four-bit InSb CCD with 200-μm bit length. An efficiency per transfer of 0.90 was measured for this device, limited by the gate length of the CCD and the interface state density. Efficiencies of 0.99 or better are projected for InSb CCDs with shorter gate lengths. Other devices for infrared applications utilizing InSb MIS structures have also been fabricated; results are given for single- and multi-element MIS detectors utilizing substrate injection readout.

I. INTRODUCTION

Since the advent of charge-coupled devices, several new concepts for the fabrication of high-density infrared detector arrays have been developed or proposed. The application of CCD readout and signal processing techniques to infrared arrays promises a new generation of infrared focal plane assemblies with significantly improved performance and reduced power and weight requirements. Several approaches for the integration of CCDs and infrared detectors are currently under development, including: 1) hybrid assemblies of conventional silicon CCDs and infrared detectors; 2) sandwich structure configurations, where silicon CCDs and infrared detectors are bonded together in a planar "sandwich" configuration and interconnected using advanced lead fabrication techniques; 3) monolithic silicon devices where CCDs are fabricated on appropriately doped silicon substrates, and extrinsic photoconductivity is employed for the detection mechanism; and 4) monolithic devices fabricated on a narrow-band semiconductor material, such as InSb, where both detectors and CCDs or related devices for readout are integrated in the same material and intrinsic photodetection is utilized. This fourth concept is the objective of the development reported in this paper.

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A monolithic infrared imaging device fabricated in the appropriate narrow-band semiconductor represents in many ways the ultimate solution for realizing an infrared imaging device. The absorption coefficient of the intrinsic material is high; therefore, high quantum efficiencies can be realized. Further, the high absorption coefficient eliminates crosstalk effects that can occur in extrinsic silicon structures. Higher permissible operating temperatures are also an advantage of the intrinsic material approach, which can be critically important in many space and tactical applications where cooling to lower temperatures is impractical.

InSb was selected for development based on the relative maturity of InSb technology compared with that of other infrared detector materials, favorable material parameters, and a spectral response suitable for a wide range of potential applications below 5.4 μm. Two such applications are infrared imaging for earth resources and planetary missions. A configuration particularly suited to these applications is the charge-coupled infrared imaging device (CCIRID), which would combine InSb metal-insulator-semiconductor (MIS) detectors and CCD readout registers in a two-dimensional array. One method of achieving significant performance improvements is to use time delay and integration (TDI) of the infrared signals on the focal plane,[1] utilizing InSb CCDs for the delay-and-add function. The possibility of achieving TDI in real time, within the imaging device itself, is an important feature of this InSb technology development and could lower future spacecraft signal processing complexity. In TDI, the signal-to-noise ratio is increased by the factor $\sqrt{N}$, with no increase in bandwidth, over that of an individual detector element, where N is the number of detector elements in the TDI subarray. Since the performance improvement is proportional to the square root of subarray length, relatively small gains are achieved by using numbers of detectors greater than about 30. Therefore, the requirements for an InSb CCD to perform TDI on the focal plane are not severe, in that the number of required bits is small; consequently, transfer efficiency need not be exceptionally high.

To successfully produce a monolithic InSb infrared imaging device, development of a high yield MIS technology in this material is required. Current status of InSb MIS development is discussed in this paper. A process technology for producing multilayer metal-insulator structures on InSb is described in Section II. Section III describes several relevant interface properties that have been determined from the fabrication of InSb MOSFETs and MIS capacitors. An InSb CCD has been designed and fabricated, with results reported in Section IV. Other devices for infrared applications utilizing MIS structures in InSb are described in Section V.

II. DEVICE FABRICATION

A process technology has been demonstrated for fabricating multilayer metal-insulator structures on InSb. This technology has enabled InSb CCDs, multielement MIS detector arrays, MOSFETs, and other MIS devices to be fabricated on this infrared semiconductor material. Starting material for device fabrication is single-crystal, tellurium-doped InSb[2] with donor concentration of $4 \times 10^{14}/cm^3$ to $1 \times 10^{15}/cm^3$. All the devices reported in this paper are wafer-processed using standard photolithographic techniques. The wafers are 2.5 to 3.8 cm in diameter, yielding approximately 80 to 120 chips per wafer for a typical die size.

Figure 1 shows an overall view of one of the InSb test chips processed in this work. This chip, which is 2.4 mm square, contains a number of exploratory devices including: MIS capacitors; MOSFETs of various geometries; test devices utilizing substrate injection readout, including a linear and an area array; and a four-phase (4φ), overlapping-gate CCD.

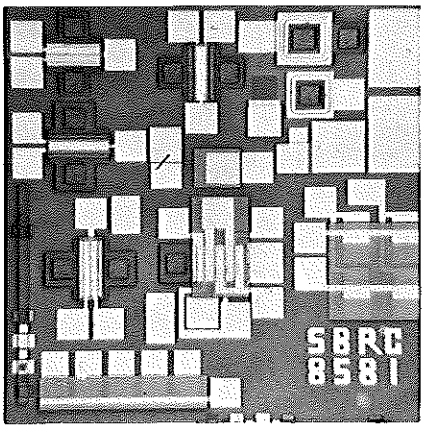


Figure 1. InSb MIS Device Chip

The fabrication sequences for a MOSFET and a four-phase CCD are useful to illustrate the materials that have been used. A photomicrograph of an InSb MOSFET on another test chip is shown in Figure 2. This MOSFET is a closed-geometry device with a channel length L = 20 μm and W/L = 50. W/L on other devices fabricated has ranged from 0.3 to 100. The MOSFET source and drain regions are formed by cadmium diffusion, followed by deposition of a gate insulator approximately 1500 Å thick. Both alumina (Al_2O_3) and silicon monoxide (SiO) have been used successfully as gate insulators in the InSb MIS devices processed in this laboratory. The higher dielectric constant (K = 8) of the former is advantageous for charge storage devices such as CCDs, since storage capacity for a given oxide thickness is increased. The Al_2O_3 is deposited by electron-beam evaporation, while the SiO is thermally-evaporated. Evaporation and delineation of the gate metal and subsequent formation of contacts to the source and drain regions complete the structure. Aluminum is used for the metal layers on Al_2O_3 devices. Titanium or titanium-gold metallizations are used on the SiO devices.

A photomicrograph of a four-bit, four-phase InSb CCD is shown in Figure 3. Test results for this device are given in Section IV. The InSb CCD makes use of an overlapping-gate, stepped-oxide structure. SiO was used for all the dielectric layers in the structure. Titanium was used for the channel stop and buried gate metallizations, and titanium-gold for the surface metal layer. Three insulator levels and three metallizations are used in this InSb CCD design. A four-phase clock layout was used to provide maximum flexibility in clocking the device. Due to the present unavailability of a proven process to either implant or diffuse n^+ layers into n-type InSb, a "channel stop" metallization was used on this device to confine the charge to the channel region. This channel stop metallization consists of a buried gate which bounds the CCD channel, deposited on top of the gate insulator (thin oxide). This metallization is in turn insulated with a thick oxide, which supports the bonding pads for the CCD gates. By appropriately dc-biasing the channel stop metallization with respect to substrate, the surface potential in the region surrounding the channel may be independently controlled.

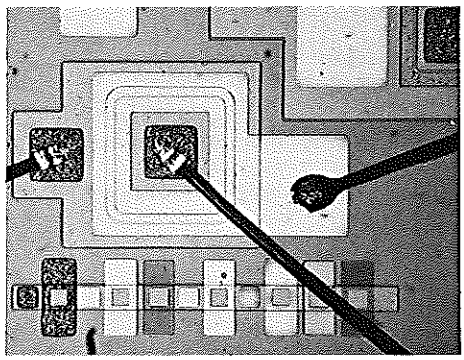


Figure 2. InSb MOSFET (W/L = 50)

The CCD of Figure 3 has a channel 0.94 mm long by 0.20 mm wide, with an input and output diffusion at either end of the channel. The device has an overlapping pair of input gates to provide flexibility for various electrical input schemes. The CCD bit length is 200 μm. The gate lengths and other dimensions on this device are consequently larger than those found in typical

silicon CCDs. The combination of dimensions, tolerances, and multilayer requirements of the CCD was, however, heretofore unproven on InSb, thereby motivating this conservative first mask design. A new mask set currently being processed incorporates 25-μm gate lengths; future designs will incorporate 13-μm or less gate lengths. Fabrication of a nine-bit linear imager with lateral transfer from MIS detectors into a CCD readout register is also underway at the present time.

Figure 4 shows a scanning electron micrograph of one section of the four-bit InSb CCD. This photograph clearly illustrates the delineation capability that has been achieved on these devices.

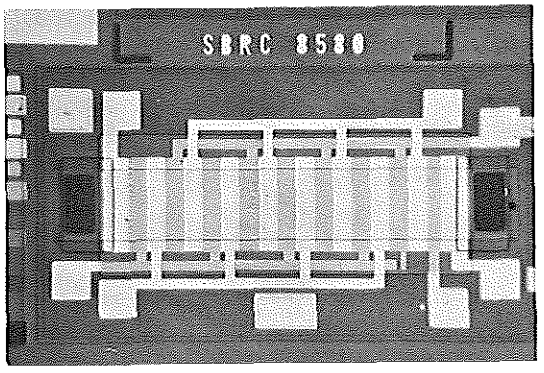


Figure 3. Four-Bit, Four-Phase InSb CCD

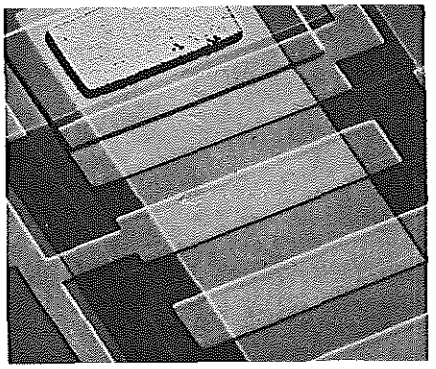


Figure 4. Detail of Four-Phase InSb CCD (200× SEM, Backscatter Mode)

Bit Length ≈ 200 μm
Separate Gate of Stepper
with Metal Electrode

III. InSb MOSFETs AND MIS CAPACITOR MEASUREMENTS

The principal test structures that have been used for process evaluation and measurement of MIS characteristics are InSb MOSFETs and MIS capacitor structures. These devices have been included on each CCD chip design that has been produced.

The MOSFETs generally follow ideal FET behavior, with square-law and linear characteristics in the saturation and low-drain-voltage regions, respectively. An output characteristic for an InSb MOSFET with Al_2O_3 insulator is shown in Figure 5. These characteristics and all other data presented in this paper were obtained at 77°K. The Al_2O_3-InSb FETs operate as p-channel, enhancement-mode devices with a threshold voltage of about -5 volts. Threshold voltages of the SiO devices are similar.

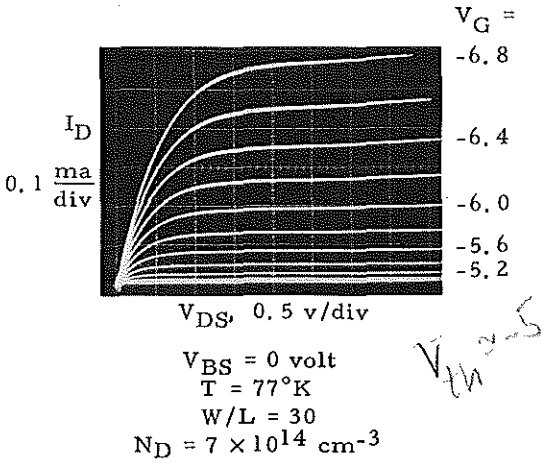
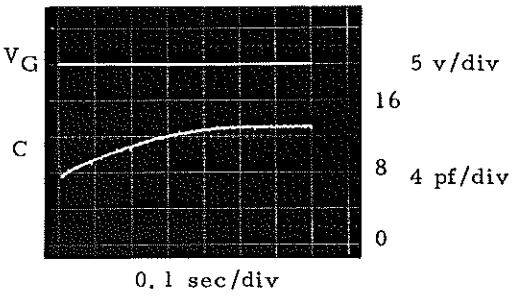


Figure 5. InSb MOSFET Output Characteristics

The effective inversion layer mobility of holes may be determined from a measurement of the channel conductance $g_D = \delta I_D / \delta V_D$ in the linear region. A plot of g_D versus $(V_G - V_T)$ should be linear in the ideal case with slope $\beta = (W/L)\, C_o \mu^*_p$ where C_o is the insulator capacitance per unit area and μ^*_p is the effective hole mobility.

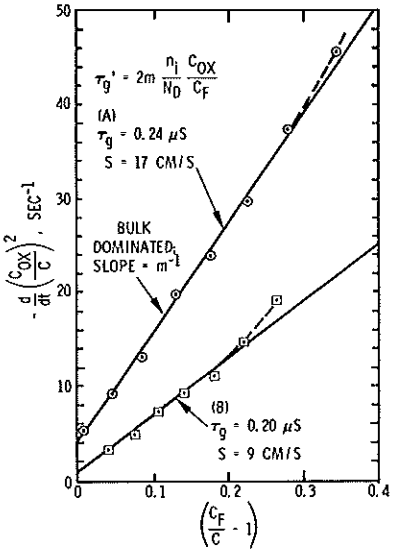
Experimentally, InSb MIS storage times of up to 0.5 sec have been measured at 77°K. Figure 7 shows the measured small-signal capacitance of an InSb MIS sample in response to a -5V step on the gate. The observed storage time for this sample is about 0.4 to 0.5 sec. By the above calculation, this magnitude of storage time indicates that the dark current is dominated by bulk rather than surface generation centers. To investigate this further, a modified Zerbst model[4, 5] was used to analyze the C-t data for several samples. A Zerbst plot tests the relationship between the inversion layer formation rate and the depletion region width. A linear region on the plot corresponds to bulk generation, where the time rate of change of the inversion layer density is given by $dp_s/dt = n_i (W_d - W_{df})/\tau_g'$. In this expression, W_d is the depletion region width at a given time, W_{df} its final value, and τ_g' the effective generation lifetime. τ_g' is obtained from the slope of the linear region and τ_g, the bulk generation lifetime, is extracted from the result. When the C-t response is primarily surface-dominated, the Zerbst plot is markedly nonlinear over its entirety. Figure 8 shows such plots for two InSb MIS samples. Curve A is for the C-t trace of Figure 7; Curve B is a plot for another sample with twice the substrate impurity concentration. The linearity of the plots corroborates the conclusion drawn from the storage time magnitude that the C-t response is bulk dominated. From the slopes of the curves, a bulk generation lifetime of about 0.2 μsec is obtained for both samples. Relating this result to hole lifetime requires more detailed knowledge of the generation centers; for the case of equal electron and hole lifetimes and generation centers at midgap, $\tau_p \simeq \tau_g/2 \simeq 0.1$ μsec. From the intercept of the Zerbst plot, the surface generation velocity s may also be calculated; the result is typically 20 cm/sec or lower.

The bulk limited dark current observed in InSb at 77°K contrasts to the room temperature silicon case, where surface generation normally dominates. This is due to the longer lifetimes in the latter material. The measured InSb storage times are, however, more than adequate for moderate clock frequencies and the CCD applications considered for these devices.



T = 77°K, 0° FOV
Signal Frequency = 10 kHz
Pulse Voltage = -5V

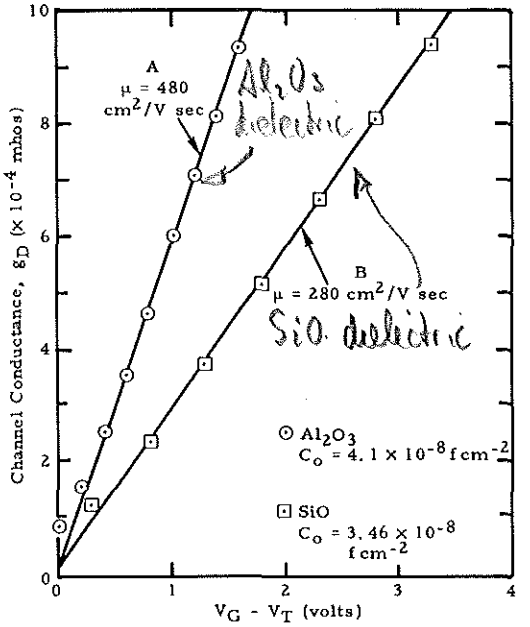
Figure 7. Storage Time of InSb MIS Sample



T = 77°K, 0° FOV
(A): $N_D = 5 \times 10^{14}$ cm^{-3}
Pulse Voltage = -5V
(B): $N_D = 1 \times 10^{15}$ cm^{-3}
Pulse Voltage = -4V

Figure 8. Thermal Generation Parameters from Pulsed InSb MIS Device Transients

Curve A in Figure 6 shows a plot of this type for the device of Figure 5. An effective mobility of about 500 cm^2/volt-sec is obtained. Curve B in Figure 6 shows a similar plot for an SiO-insulator InSb MOSFET, with a typical value of mobility observed with this dielectric material. The observed effective mobilities are comparable to silicon MOS devices; consequently, these InSb transistors display the same transconductances as silicon MOSFETs of the same geometry. As a result, charge transfer in an InSb CCD will be comparable to that of a silicon CCD, of similar geometry, if other factors such as interface state density are also comparable.



T = 77°K
W/L = 30

Figure 6. InSb MOSFET Channel Conductance in Linear Region Versus Gate Voltage

Pulsed MIS capacitor (C-t) measurements have been used to investigate the non-equilibrium characteristics of the InSb MIS samples. The storage time is a particularly important parameter for charge transfer devices. Since the pulsed MIS capacitor measurement is sensitive to minority carrier generation from all sources, a 0° FOV (dark) storage time test is an effective measure of overall device quality. The dark current is given approximately by[3]

$$J_G = qn_i \left(\frac{n_i L_p}{N_D \tau_p} + \frac{W_d}{2\tau_p} + \frac{s}{2} \right)$$

where the first term is the leakage current due to minority carriers generated in the neutral bulk which diffuse to the surface depletion region, the second due to carriers generated in the depletion region of width W_d, and the third due to generation at the surface with surface generation velocity s. n_i is the intrinsic carrier concentration, N_D the impurity concentration, L_p the diffusion length, and τ_p the minority carrier lifetime. The storage time T_s is proportional to the charge capacity and inversely related to the average dark current; i. e., $T_s \simeq C_o \Delta\phi_s / J_G$ where $\Delta\phi_s$ is the difference in full and empty well surface potentials. Using the representative 77°K values:

$N_D = 10^{15}/cm^3$

$n_i = 2.7 \times 10^9/cm^3$

$\tau_p = 0.1$ μsec

$\mu_p = 9 \times 10^3$ cm^2/volt-sec

$L_p = 25$ μm

$\epsilon_s = 1.5$ pf/cm

$C_o = 3 \times 10^{-8}$ f/cm^2

$\Delta\phi_s = 2.5$ volts

the estimated dark current components at 77°K are:

J (diffusion)	0.03 na/cm^2
J (depletion region)	300 na/cm^2, average
J (surface)	(0.2) (s) na/cm^2

where s is in units of cm/sec. The generation in the depletion region clearly dominates the diffusion component at this temperature, similar to the InSb p^+-n photodiode case. For sufficiently low s, the expected bulk-limited storage time is on the order of 0.25 sec.

The MIS conductance technique[6] has been used to determine interface state density using InSb MIS capacitors. Representative curves of equivalent parallel conductance G_p/ω versus frequency obtained by this technique are shown in Figure 9, for two values of gate bias. For both curves (A) and (B), the sample is biased such that the surface is depleted. The data were fitted reasonably well by the equivalent parallel conductance for an interface state continuum (broken curves in Figure 9). A deviation from the theoretical curve is observed at low frequencies due to the influence of minority carrier transitions, in addition to the majority carrier transitions on which this model is based. The minority carrier response, usually negligible in silicon devices, appears at low frequencies in InSb due to higher generation-recombination rates. Using $N_{ss} = 2.5\ (G_p/\omega)_M/q$, the interface state density was calculated from the peak value $(G_p/\omega)_M$ of the equivalent parallel conductance curve. From curve (A), an $N_{ss} = 1.4 \times 10^{12}/cm^2\text{-eV}$ is obtained, while curve (B) yields, for N_{ss} near midband, a value $6.2 \times 10^{11}/cm^2\text{-eV}$. The results of conductance measurements agree with densities as determined by a high-frequency capacitance-voltage technique.

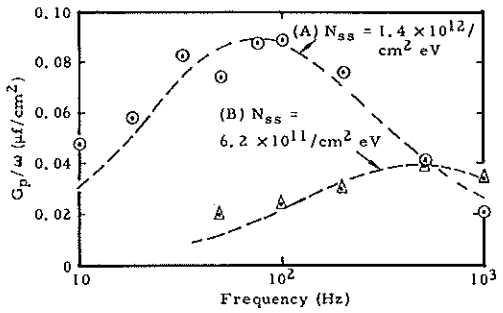


Figure 9. Equivalent Parallel Conductance Versus Frequency for InSb MIS Sample

IV. InSb CCDs

The 4φ overlapping-gate InSb CCD (Figure 3) has been successfully operated with three different clocking modes. These modes are: (a) conventional 4φ clocking; (b) 4φ clocking with storage only under the buried gates; and (c) simulated 2φ clocking. Mode (a) results in four transfers per bit while both modes (b) and (c) produce two transfers per bit. Electrical input was achieved by several techniques: the signal was applied to one of the input gates or input diffusion, with the other two input terminals appropriately biased. The device output was obtained through use of the conventional precharge (or reset) circuit, except that the output circuit elements, with exception of the output diode, were not integrated on-chip as is the case in most silicon CCD structures. The circuit was built up in discrete form using silicon FETs and interconnected to the InSb output diode by means of wire bonding. This resulted in a functioning circuit sufficient to observe device operation, but the large output circuit capacitances resulted in a low output responsivity (15 mv/pC) and increased reset clock feedthrough.

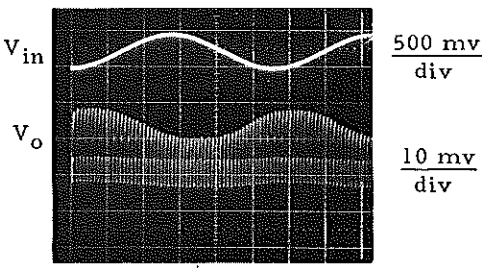
Figure 10 shows input and output waveforms for the four-bit CCD clocked at 5 kHz, with a sine wave input signal. The simulated 2φ clock mode (c) was used in this case, and the signal was applied to the buried input gate. Input and output waveforms using clock mode (a) and a square-wave input are shown in Figure 11. (Note that the output waveform is inverted with respect to the input waveform on all oscilloscope photographs.)

Measurement of the transfer efficiency for the device was carried out in all three clocking modes. The results for the efficiency per transfer η, at a clock frequency of 5 kHz, ranged from $\eta = 0.82$ to 0.92 depending on the clock mode, fat zero level, and measurement technique used. The best measured efficiencies were obtained for those devices operated in mode (a), but the results for the other modes were not significantly different. For simplicity, only

the 4ϕ clock results are discussed here. Two principal methods were used in computing the transfer efficiency from the output data. In method (1), the magnitudes (B) of the first output pulse and the maximum value (A) of the signal output were measured. η was then computed from $\eta = (B/A)^{1/N}$, where N is the number of transfers. For mode (a), four transfers per bit result in N = 16. Method (2) utilized the sum of the charge deficits in the leading signal outputs (S_L) or the sum of the trailing signals (S_T) to estimate the efficiency. In this approach, the sums are related to the inefficiency ϵ by:

$$S_L = S_T \simeq \frac{N\epsilon}{1 - \epsilon}$$

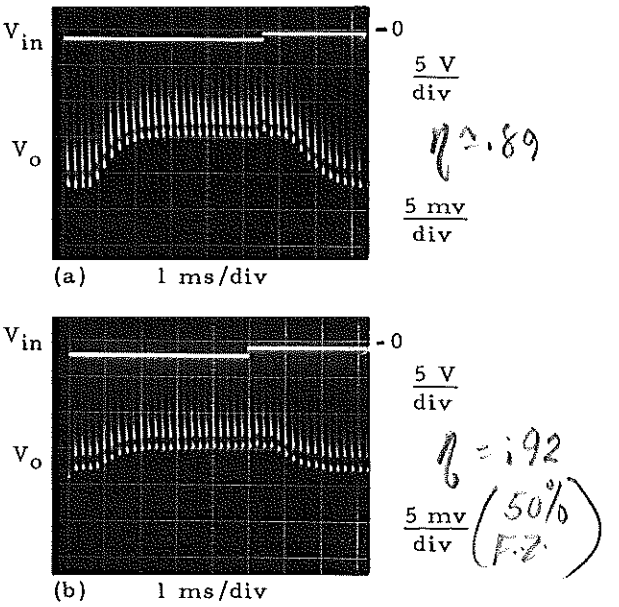
By measuring either S_L or S_T and inverting, the inefficiency ϵ ($\eta = 1 - \epsilon$) may be readily computed.



f_c = 5 kHz
Clock Mode (c)
ϕ_{INB} Input
T = 77°K, 0° FOV

Figure 10. InSb CCD Output Waveform

In Figure 11(a), the device was operated without a fat zero while in Figure 11(b) a fat zero of approximately 50% of saturation was used. From the output signal of Figure 11(a), the efficiency per transfer is computed as $\eta \simeq 0.886 \pm 0.006$ using method (1), while application of method (2) yields $\eta \simeq 0.854 \pm 0.01$. Similarly, the results with fat zero [Figure 11(b)] are $\eta \simeq 0.919 \pm 0.009$ as determined by method (1) and $\eta \simeq 0.880 \pm 0.01$ using the leading and trailing sum approach. Although the alternate methods yield slightly different results, an average of several measurements showed that $\eta \simeq 0.90$ was typical of the device when operating in the conventional 4ϕ clock mode.



f_c = 5 kHz
ϕ_{INB} Input

Figure 11. Output Waveform, Clock Mode (a)

The two principal mechanisms which limit the transfer efficiency of the InSb device are the lengths of the CCD gates and the interface state density. As mentioned in Section II, long gates were used on these devices because of processing uncertainties on this first mask set. Computer calculations, based on a two-dimensional model with 50-μm gates, predict a negligible tangential field in the gate centers and a field of approximately 1000 v/cm at the gate edges. For this gate length, therefore, the fringe field coupling between the gates is small. As a result of these small fields, the transfer through the device relies principally on diffusion.

The gate length also increases the impact of interface states on the device efficiency. To examine this dependence, the effects of interface states were treated using the model proposed by Lee and Heller.[7] The basic assumptions of this model are instantaneous charge redistribution during the transfer period and the use of an effective time constant (τ_s) to describe the effects of interface states. Using the Lee and Heller model, the constant τ_s was determined by fitting the model predictions of transfer efficiency to $\eta \simeq 0.90$, the measured value for the present InSb structure at 5 kHz. Assuming the same clock rate and conventional 4ϕ operation, the efficiencies predicted for future devices with various gate lengths were calculated. The results are shown in Table 1. The well depth used in the calculation is also shown in Table 1. It represents the ratio of the charge stored to the capacitance of the storage well. The well depth observed in operating the present device was $\simeq 0.5$ volt, so this value was used in fitting the measured efficiency. For the remaining cases of 25-μm, 13-μm and 7.5-μm gate lengths, a well depth of 2 volts was assumed, since this value has been observed on InSb discrete devices and is expected to be realized on future CCD structures. A significant decrease in interface state loss with decreasing gate length is evident in the Table.

Table 1. Calculated Transfer Efficiency Versus Gate Length for InSb CCD

GATE LENGTH (μm)	WELL DEPTH (volts)	INTERFACE STATE LOSS	EFFICIENCY (η)
50	0.5	9.36×10^{-2}	0.90
25	2.0	9.64×10^{-3}	0.990
13	2.0	2.51×10^{-3}	0.997
7.5	2.0	9.11×10^{-4}	0.999
f_C = 5 kHz; $\tau_S = 5 \times 10^{-6}$ sec; NO FRINGE FIELD; 4ϕ CLOCK MODE (a)			

Used Heller's model to fit data and obtain $\tau_S = 5 \times 10^{-6}$ sec.

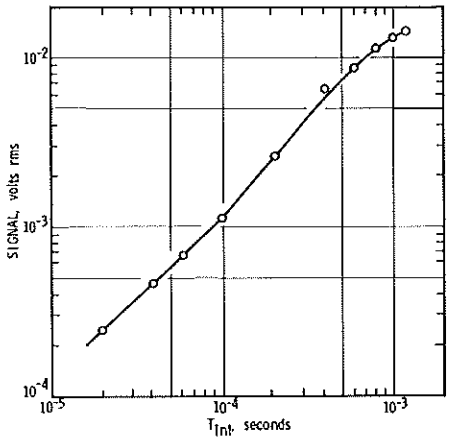
In summary, CCD operation has been achieved on an InSb substrate. Analysis of the device structure indicates that the transfer efficiency is limited by the gate length as well as by interface state trapping. From Table 1, an efficiency of $\eta = 0.99$ or better is predicted, even with the present interface state density, for InSb CCDs with gate lengths of 25 μm or less. Although these predictions are necessarily qualitative, they represent reasonable extrapolations from the performance of the first devices reported here. Further, fringe field coupling will also enhance transfer in future devices with decreased gate lengths, an effect which has not been included in the calculations leading to Table 1. The efficiency values projected in the Table will be more than adequate for a number of system applications of these InSb CCDs. Investigation of processing variations to reduce interface state densities is also continuing, and future improvements are anticipated.

V. InSb MIS DETECTOR ARRAYS

Other devices for infrared applications utilizing MIS structures in InSb have been fabricated. The interface properties and multilevel structure capabilities demonstrated in the InSb CCDs are also applicable to the fabrication of MIS detector arrays using approaches other than CCDs for readout. Two such techniques are the detection of signal charge by sensing voltage change on an element or line capacitance, or the injection of signal charge into the substrate and detection of the displacement current by various circuit approaches.

Single-element InSb MIS detectors utilizing substrate injection readout were fabricated and tested prior to processing of multielement arrays. The single-element device has a 125-μm square active area defined by a semitransparent titanium gate approximately 50 Å thick. Infrared testing was accomplished using chopped blackbody radiation input and a cold FOV restriction to reduce background photon flux to 2×10^{14} photons/sec-cm^2, a typical level for a 3- to 5-μm infrared system. Figure 12 shows

the dependence of output signal on integration time for a representative device, for a constant incident blackbody irradiance. The output signal is approximately linear with integration time as expected for an integrating detector, until a saturation point is reached which is dependent on the total incident photon flux and the storage capacity of the device. For the example shown in Figure 12, saturation occurs at about 1 msec, consistent with the background flux and clock level used. The MIS detector shows the typical InSb spectral response, identical to that of a photovoltaic InSb detector. Relative response per photon is nearly flat over the spectral band characteristic of an ideal quantum detector, with the intrinsic InSb cutoff at 5.4 μm.



$T_{BB} = 500°K$
H_{BB} (rms) $= 7.1 \times 10^{-6}$ watts/cm^2
$T = 77°K$
$Q_B = 2 \times 10^{14}$ phot/sec cm^2
$A_D = 1.6 \times 10^{-4}$ cm^2

Figure 12. Output Signal Versus Integration Time for InSb MIS Detector

Five-element MIS detector arrays also have been designed and fabricated; one such array is shown in Figure 13. Device processing techniques are similar to those used in the InSb CCDs: insulator layers are SiO; all metal levels, including the transparent gates, are titanium. Each element (or unit cell) of the array consists of a pair of overlapping transparent gates: an X gate on the buried metal level, and a Y gate of equal area on the surface metal level. Each gate is 125 × 125 μm. The X gates are interconnected with a buried metal clock line, terminating in a bonding pad which is positioned over a channel stop or ground plane metallization and its associated thick oxide. This latter metallization level ensures that no infrared sensitivity or other spurious effects are obtained in the bonding pad region. In a full two-dimensional array of these devices, the Y gates would be similarly interconnected by a pattern of clock lines (on the surface metal level) at right angles to the X clock lines. On this linear array, the Y lines were eliminated and contact was made directly to the Y gates by wire bonding.

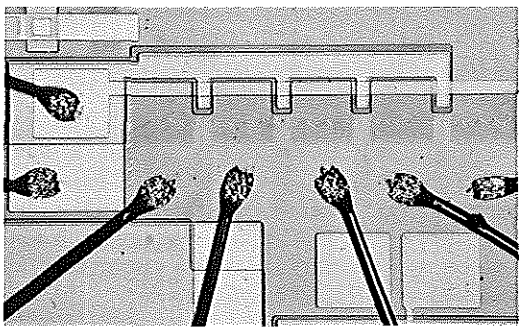
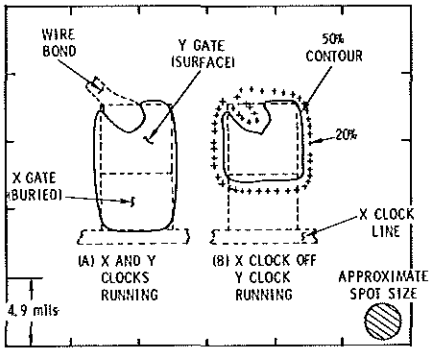


Figure 13. 5-Element InSb MIS Detector Array

The correct mode of operation of the unit cells in the linear arrays has been observed; i.e., the transfer of stored charge from the X gates to the Y gates and subsequent charge injection readout has been obtained. A clear demonstration of unit cell operation was obtained by infrared spot scanning of the device. Figure 14 shows a contour plot of one unit cell of a five-element array. In Figure 14, both X and Y clocks are running, and the full 125 × 125 μm area is photosensitive as shown. In Figure 14(B), the X gate is grounded, disabling this half of the cell, as confirmed by

the resulting spot scan. Spectral response and other characteristics of the arrays are similar to those of the single-element devices.



T_{int} = 200 μsec
T = 77°K
$Q_B = 2 \times 10^{14}$ phot/sec cm^2
f/6 Objective

Figure 14. Spot Scan of InSb MIS Array Unit Cell

VI. CONCLUSIONS

An InSb MIS technology for the fabrication of monolithic InSb infrared imaging devices is under development. The insulator-InSb interface properties as determined from MOSFET and MIS capacitor structures have been found to be favorable for the fabrication of CCDs and other charge storage devices in this material. A process technology for producing the required multilayer metal-insulator structures on InSb also has been demonstrated, a second requirement for realization of the monolithic infrared imaging device. Third, the principal component of a CCIRID, an InSb charge-coupled device, has been fabricated and successfully operated. Finally, InSb MIS detectors have been produced which are suitable for fabrication of two-dimensional arrays using other approaches for readout. The demonstration of charge coupling in InSb offers the potential of a future generation of 1- to 5-μm monolithic infrared imaging devices with significant reduction in focal plane assembly complexity, reduced sensor power and weight requirements, and improved performance.

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